

A Time Difference Amplifier

A.M.Abas, A.Bystrov, D.J.Kinniment, O.V.Maevsky, G.Russell, and A.V.Yakovlev

Dept of Electrical and Electronic Engineering, University of Newcastle, NE1 7RU, UK

Abstract—Accurate measurement of edge time differences down to 10ps or less is required for tests of timing in digital systems. We describe a circuit aimed at reliably amplifying these time differences by a factor between 3 and 10 before measurement to enable greater accuracy.

I. INTRODUCTION

With the reduction in dimensions and consequent increasing speed of digital circuits, sub-micron devices show increasing variability of delays. Parametric changes, as well as spot defects, may cause the dynamic behavior of a circuit to change, resulting in timing problems. While systems can be fully tested functionally by adding test structures on chip, timing issues remain a problem, particularly the timing margins available when working at full speed. Measurement of the relative timing of two signals is central to any timing test, for example the test of set up and hold input timing requires the test data and clock timing to be adjusted to very accurate absolute timing margins, perhaps as low as 10ps. Techniques which are useful in this context, are timing adjustment methods, such as adjustable delay lines made of inverter chains [1][2], and specialised circuits for indicating which of two signals appears first. Digitally adjustable delay lines can be made from a network of inverters that are switched to produce delay paths alterable in increments of two inverters, or less, and comparison of the timing between two signals can be done by means of a MUTEX circuit which indicates which of two requests arrive first [2][3]. By delaying the earlier signal with a digitally adjustable delay line in a succession of stages, each with a factor of two smaller

delay, it is possible to produce a digital representation of the initial time difference [4]. The problem is that because variations in individual inverter pair delays may be up to 10ps, very accurate time measurements difficult.

II. TIME MEASUREMENT

A MUTEX circuit is shown in

Figure 1 in which the assertion of an input signal is compared with a reference, after resolution of any metastability, the circuit indicates which was the first input to occur. Provided the MUTEX is symmetrical with respect to signal and reference, the accuracy of the result with respect to the time difference $\Delta_t = t_s - t_r$ between signal and reference is limited only by noise. Consequently, resolution to an accuracy of 0.1ps in a circuit with a MUTEX time constant, τ , of 100ps should be possible [5]. In other words, if the value of Δ_t is greater than this accuracy limit, the output “Signal first” (or “Reference first”) will respond after a finite metastability resolution time T_m . If, however, Δ_t is too small, then it can only be measured with some error E_Δ (affected by noise). In practice imperfections in fabrication may affect the transistor sizes, and power supply variations will also reduce the overall circuit accuracy. Results from simulations of MUTEX circuits in AMS 0.6 μ CMOS technology with up to 10% variation in transistor nominal size are shown in Table 1. If only one of the eight transistors has a size of 10% above nominal, the time offset is no more than 6.7ps, but the worst case distribution of sizes within the range 0-10% gives a maximum offset of 12.5ps. The probability of this worst-case situation occurring in a circuit with eight closely spaced transistors is fairly low.

Potentially more accurate time measurements can be made by using the response time of two MUTEXs to effectively amplify the input time difference. The difference in the output voltages for a bistable in metastability is approximately given by: $\Delta_V = q \cdot \Delta_t \cdot e^{t/\tau}$, where τ is the device time constant, q is the conversion factor from time to initial voltage at the metastable nodes, and Δ_t , is the input time overlap between the two inputs [5]. This formula is correct for the interval $|\Delta_t| \in \left(0, \frac{|\Delta_V|}{q}\right)$, and provides a practically acceptable approximation for $|\Delta_t| \ll \frac{V_{dd}}{q}$. In a typical MUTEX fabricated in 0.6 μ technology, the output time has a log relation to the input time difference. For these devices, previous work has shown that $q = 3 \text{ mV/ps}$, and $\tau = 125 \text{ ps}$ [5], and the threshold value at which the output changes is determined by the filter transistors at about 1V difference between the outputs. In this case, the theoretical curve given by $t = -\tau \ln(q \cdot \Delta_t / \Delta_V)$ is close to those obtained by simulation of a MUTEX circuit for time differences below 50ps. The corresponding output times are greater than 300ps.

This relationship can be used in a circuit which compares two rising inputs, and produces two outputs differing in time by a multiple of the input time difference. Reference to rows 4 and 5 of Table 1 shows that increasing the width of both B input transistors by 10% on the signal side of the MUTEX will give an offset of 6.7-1.6 = 5.1ps, and decreasing their width on the reference side will produce a total offset of about 10ps. Simulations show that a repeatable 45ps offset is produced by width ratios of 2:1 (+ and - 33%) in the width of the B inputs. By using two MUTEX circuits, as shown in Figure 2, one with an offset of +45ps, and one with -45ps, over the range + or -30ps input time difference, Δ_{in} , the time difference of the

two outputs, Δ_{out} , will be given by $\Delta_{out} = \mathbf{t} \cdot \ln(45 + \Delta_{in}) - \mathbf{t} \cdot \ln(45 - \Delta_{in})$. A SPICE simulation confirming this relationship is shown in Figure 3. At the point where $\Delta_{in} = 0$, the gain of the circuit is given by $\frac{d\Delta_{out}}{d\Delta_{in}} = \frac{2\mathbf{t}}{t_{offset}}$, thus the gain in this case is about 5. By adjusting the offset value gains of between 3 and 10 can easily be produced. Note that the gain depends only on transistor ratios, since the values of \mathbf{t} and t_{offset} are both related to the technology time constants in the same way, and as a result the gain at 10ps input varies by less than 2% for a 10% change in Vdd. The zero accuracy of this circuit also depends on variations in the geometry of the MUTEX, but with careful layout it should be possible to achieve better than 5ps.accuracy at the input.

III. CONCLUSIONS

The accuracy of time measurements between two rising edges can be improved by using a time amplifier circuit to increase the size of the time difference by a reliable amount before the measurement, thus if a measurement accuracy of 30ps is obtainable, the effect of a factor of 5 time amplification would be to improve that accuracy to $30/5 + 5 = 11$ ps, making on chip time measurement a practical proposition.

IV. REFERENCES

- [1]S.W.Moore, G.S.Taylor, P.A.Cunningham, R.D.Mullins and P.Robinson. "Using Stoppable Clocks to Safely Interface Asynchronous and Synchronous sub-systems". Proceedings AINT2000, Delft, 19-20 July 2000 pp.129-132.
- [2]R.Ginosar and R.Kol. "Adaptive Synchronization". Proceedings AINT2000, Delft, 19-20 July 2000 pp.93-101.
- [3]C.Molnar, I.Jones. "Simple Circuits that Work for Complicated Reasons". Proceedings Sixth International Symposium on Asynchronous Circuits and Systems, Eilat, April 4-6: 2000.

- [4] O.V. Maevsky and E.A. Edel. "Converter of time intervals to code". USSR Patent Certificate 1591183, Class H03M1/50, Bulletin No. 33, 070990.
- [5] D.J. Kinniment, A. Bystrov, and A.V. Yakovlev. "Synchronization Circuit Performance". IEEE JSSC, Vol. 37, No. 2, pp202-209, Feb 2002.

Signal Gate transistor widths, μ				Reference gate transistor widths μ				Time error
Input A		Input B		Input A		Input B		E_{Δ}
p	n	p	n	p	n	p	n	ps
6.7	7.5	6.7	7.5	6.7	7.5	6.7	7.5	0
7.37	7.5	6.7	7.5	6.7	7.5	6.7	7.5	-2.9
6.7	8.25	6.7	7.5	6.7	7.5	6.7	7.5	+1.2
6.7	7.5	7.37	7.5	6.7	7.5	6.7	7.5	-1.6
6.7	7.5	6.7	8.25	6.7	7.5	6.7	7.5	+6.7
7.37	7.5	7.37	7.5	6.7	8.25	6.7	8.25	-12.5

Table 1 MUTEX time errors

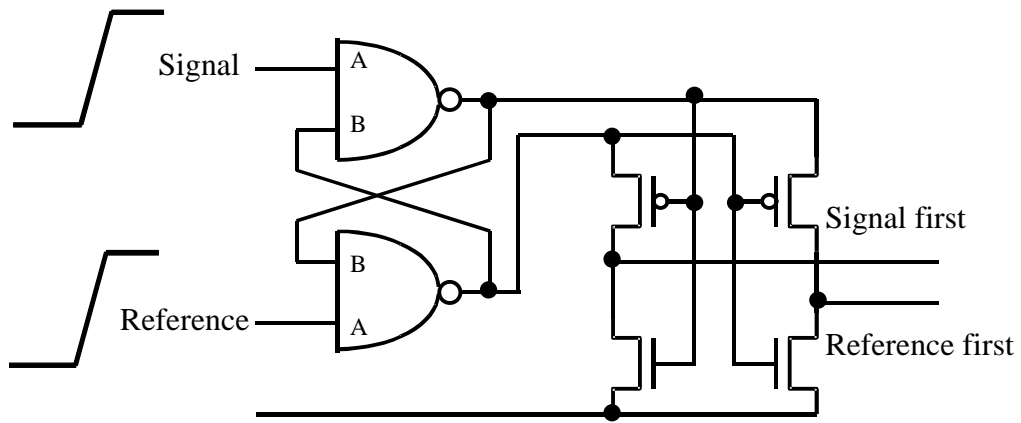


Figure 1 MUTEX time measurement

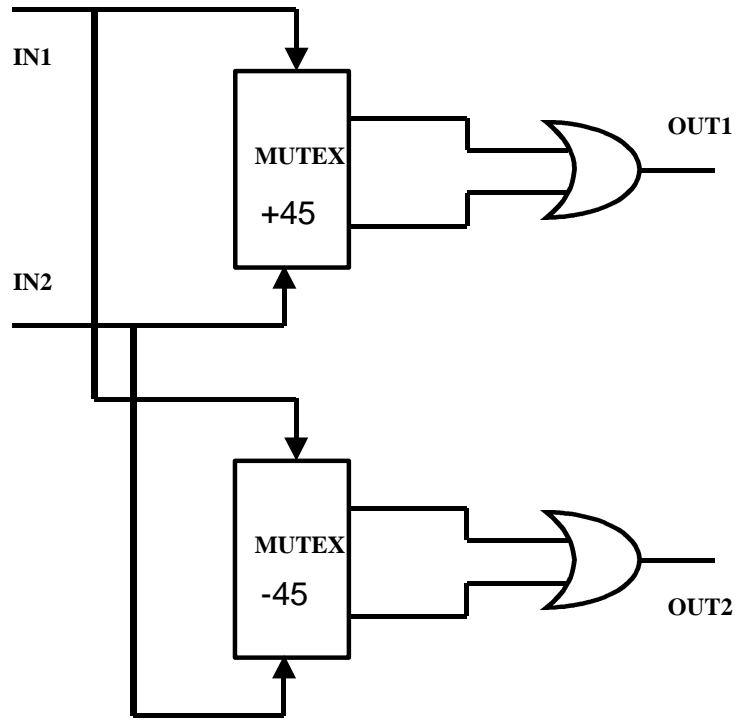


Figure 2 Time amplifier

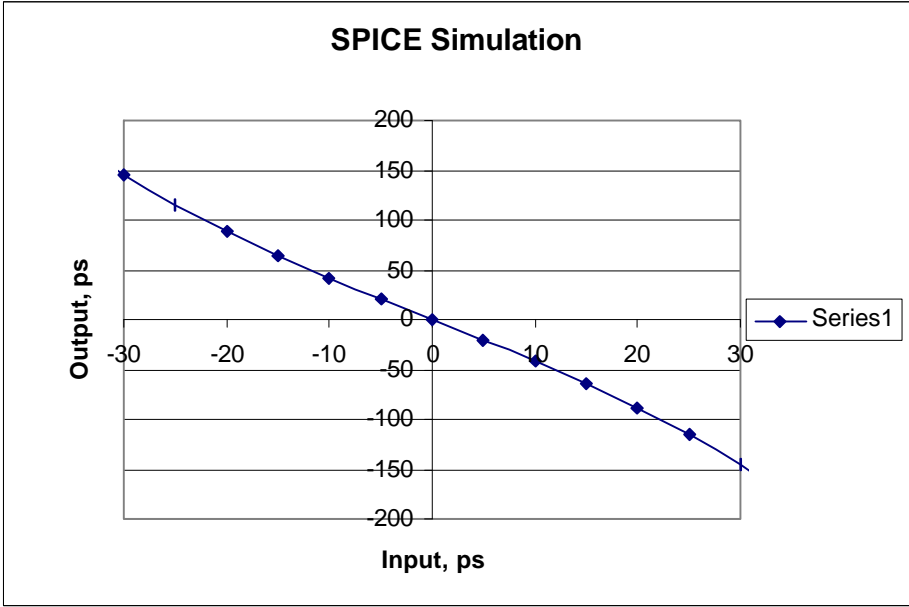


Figure 3 Amplifier Characteristic