Synchronization Circuit Performance

D. J. Kinniment A Bystrov, and A.V. Yakovlev, University of Newcastle, UK

Abstract—Synchronizer circuits are usually characterized by their rate of failure in transmitting data between two independently timed regions. The mean time between failures is assumed to be $MTBF = \frac{e^{t/t}}{T_w . f_1 . f_2}$, where f_1, and f_2 are the clock frequencies on either side of the interface, t and T_w are constants. Here t is the time allowed for the synchronizer circuit to reach a stable value after clocking. Previous experimental work has shown that the slope of the histogram relating the logarithm of failure probability to t, is not always constant. We show that these effects, which include an apparent reduction in the value of t in the early part of the histogram to as much as 60% of the final value can be explained by extending the existing theory to take account of initial offsets, and propose a new, more accurate, formula:

$MTBF = \frac{e^{t/t_b}}{\left[\frac{V_e}{V_{t-v}} - \frac{V_s}{V_{t-v}} e^{\frac{-t}{t_a}}\right] . f_1 . f_2}$ where V_s, V_e, $V_{t\text{-}v}$, t_a and t_b are circuit constants.

Synchronizer performance depends on achieving a high reliability of synchronization together with a short time. We show that commonly used circuits such as the jamb latch, do not produce the best compromise for very high reliability applications, and that a circuit with a lower value of t can be designed.

In order to confirm that thermal noise does not influence the MTBF against synchronization time relationship, we have devised an experiment to measure noise in an integrated CMOS bistable circuit. We show that the noise exhibits a Gaussian distribution, and is close to the value expected from thermal agitation.

Index terms-- analysis, design, digital, large-scale integration

I. INTRODUCTION

Synchronization of digital data paths in sub-micron technology is of interest, because system failure may result from metastability in the synchronizer circuits, [1][2][3]. One aspect of this problem that is becoming increasingly important is the design of synchronization circuits for multiply clocked systems, or for globally asynchronous locally synchronous systems. The frequency of failure in synchronizers using bistable devices is determined by the probability of marginal input triggering conditions, and the resulting mean time between failures (MTBF) of the system is dependent on the clock frequencies on either side of independently timed interfaces, f_1, and f_2, the number of synchronizers, and the response time of the circuit, t. The MTBF, for an individual synchronizer, is represented by:

$MTBF = \frac{e^{t/t}}{T_w . f_1 . f_2}$, [1][2] and includes a parameter T_w, which may not be constant. Future systems will have clock rates of over 1GHz, and the number of interfaces between separately timed zones, and therefore synchronizers, is likely to be high because of the difficulty of clock distribution. The time, *t*, allowed for synchronization must be kept as short as possible to maintain system performance, but in order to keep system failures to less than 1 in 10^8 s (2 years) *t* may need to be over $30t$. Control of failure rates therefore depends on a good understanding of the synchronizer MTBF formula. Previous theory assumes a constant value t and T_w for all conditions, but recent results suggest that this is not the case [2], differing values of slope having been observed for different inputs. It is apparent that large inputs can drive the circuit away from the metastable point and while it settles, the value of t may be apparently higher or lower than normal.

Our aim is to analyze typical synchronizer and arbiter circuits and show how the results can be accounted for within accepted theory, and consequently how synchronizer circuits can be designed for optimum performance. In this paper, Section II will develop the basic theory to account for different output thresholds and initial conditions, Section III will compare this theory with simulations of practical circuits and present results of measurements on the circuits themselves. In section IV noise measurements are given, and section V will discuss the results, and the implications for system designers.

II. MODEL

Most models of bistable circuits operating as synchronizers assume that the cross coupled gate circuits operate as two linear amplifiers [4][5][6]. Each gate is represented by an amplifier of gain $-A$ and time constant RC, as shown in Figure 1. Differing time constants due to different loading conditions may also be taken into account [6]. The model for each gate is linear with a gain A and has an output time constant determined by CR. In a synchronizer, both the data and clock timing may change within a very short time, but no further changes will occur for a full clock period, so we can assume that the input is monotonic, and the response is unaffected by input changes.

For the two time constants we can put: $t_1 = \frac{C_1.R_1}{A}, t_2 = \frac{C_2.R_2}{A}$, and this leads to

$0 = t_1.t_2.\frac{d^2V_1}{dt^2} + \frac{(t_1 + t_2)}{A}.\frac{dV_1}{dt} + (\frac{1}{A^2} - 1).V_1$. This has a solution of the form:

$V_1 = K_a.e^{\frac{-t}{t_a}} + K_b.e^{\frac{t}{t_b}}$

K_a and K_b are determined by the initial conditions; t_a and t_b by t_1, t_2, and A. We assume typical values of t_1, t_2, and A for a 3.3V, 0.6μ, process, of 100ps for t_1 and t_2 (depending on the loading of the inverters) and 30 for A.

This model is valid within the linear region of about 50mV either side of the metastable point. Outside this region the gain falls to less than 1 at about 400mV, but the output resistance of the inverter and the load capacitance also drop significantly, R by a factor of more than 10, and C by a factor of about 2. Thus, even well away from the metastable point the values of t_1 and t_2, are still about 70ps. We measured the values of t_1, t_2, and A, over a range of inputs (corresponding to different values of K_a and K_b), and from these estimated the time constants t_a, and t_b, in our technology for different values of offset as in Table 1.

Offset Voltage	***A***	t_a	t_b
0	30	96.3	102.9
50mV	5	82.8	124.5
100mV	3	74.5	149.5
200mV	2	66.2	199.5
400mV	1	49.5	∞

Table 1 Inverter measurements

For most metastable events of interest, the initial conditions are such that K_b, which is the voltage difference between output nodes at the start, is less than 10mV, and while K_a, the common offset at the start, may be as much as 0.5V. However operation always reaches the linear region quickly because t_a is small outside this region. Thus a metastable event will have a trajectory that spends most of its time in the linear region and we believe we are justified in using the model above to predict qualitatively the performance of our circuits.

Figure 2 shows the response of the output against time predicted by this model when both outputs start from a point higher than the metastable level and from a point lower. This initial offset of both outputs is given by K_a = + 450mV and – 450 mV from the metastable level of 1.65V. For both these trajectories K_b = 12 mV, representing the initial difference between the two outputs. We use t_a = 75 ps and t_b =125 ps to represent a typical situation where A is about 5-10.

It is common for exit from metastability to be detected by an inverter with a slightly different threshold from the metastability level of the bistable . Thus when V_{out} exceeds that level the inverter output changes. The metastability level of the bistable here is 1.65V, and the threshold level is 1.75V. V_{out} exceeds 1.75V at 240ps for the high start of 2.1V or 280ps for the low start of 1.2V. Note that the time difference depends upon the threshold level, and that if the high start trajectory never goes below 1.75V, that is if K_b > 14 mV, no events are detectable for output time delays between 0 and 200ps. It is clear from this that the number of metastable events recorded between 0 and 300ps output time will depend strongly on the starting point and the output threshold.

Figure 3 shows how this affects the measurement of metastability. Typical characterisation measurements use oscillators to supply independent asynchronous inputs for data and clock, so that a large number of different input time overlaps occur over the time of the measurement. We plot the number of output events lying within a small interval, say 1pS, of a particular metastability time t_m, [2]. If the distribution of data and clock overlaps in time is uniform, then we would expect the number of events per second to follow the relationship: $N \approx e^{-t/t}$. In Figure 3 , K_a = + 450mV for the high start curve, and – 450 mV for the low start, both with t_a = t_b =100 ps. For all of the histograms of output events presented in this

paper, 10^{10} experiments with time differences distributed uniformly between 0 and 1ns are assumed. The events scale is the probability of a trajectory reaching the high output level within 1ps of the time given by the X axis. In order to calculate the model responses in Figure 3 and Figure 4 a uniform distribution of voltage offsets, K_b, have been derived from these time differences by using $K_b = V_{t-v}.T_{c-d}$ where $V_{t-v} = 10\,\text{mV/ps}$ in this case, and $T_{c\text{-}d}$ is the input time overlap between clock and data.

The two curves deviate from the expected straight-line relationship, the high start curve recording no events before 200ps because trajectories with large enough initial conditions do not intersect the output threshold of 1.75V, and then events are recorded earlier than expected. In the low start curve, events are delayed rather than accelerated by the effects of the $K_a.e^{\frac{-t}{t_a}}$ term.

The formula $V_1 = K_a.e^{\frac{-t}{t_a}} + K_b.e^{\frac{t}{t_b}}$ provides a better model than $V_1 = K.e^{\frac{t}{t}}$, for calculating MTBF, since, if we put V_s for the initial common mode offset, voltage, V_e, for the final voltage where the trajectory leaves the linear region, we have: $V_e = V_s.e^{\frac{-t}{t_a}} + V_{t-v}.T_{c-d}.e^{\frac{t}{t_b}}$.

Further, since the probability of one occurrence of an overlap time of $T_{c\text{-}d}$ or less is given by: $T_{c-d}.MTBF.f_1.f_2$, we can show: $MTBF = \dfrac{e^{t/t_b}}{\left[\dfrac{V_e}{V_{t-v}} - \dfrac{V_s}{V_{t-v}}e^{\frac{-t}{t_a}}\right].f_1.f_2}$, in which all the parameters are constant. This also shows the initial value of T_w can be different from its final value if the start point is anything other than zero.

It is also possible for coherent external influences, such as a late change on an input to affect the event histogram. If there is no external input, and there are N trajectories evenly

distributed within the linear region at time t = 0, the number, of those that exit to give a high output in the time between t and $t + dt$, is given by: $dn = \frac{1}{2t} N.e^{\frac{-t}{t}} dt$

If all of these trajectories are affected by some external influence at time t such that they are shifted up by a small amount, dV_{ext}. then $n\frac{dV_{ext}}{V_h}$ more will exit through the upper boundary of the linear region V_h, and $n\frac{dV_{ext}}{V_h}$ less will exit towards 0V. Thus if the original histogram was given by $dn = \frac{1}{2t} N.e^{\frac{-t}{t}} dt$, it will now be modified by the additional input to

$$\frac{dn}{dt} = \left[\frac{1}{V_h}\frac{dV_{ext}}{dt} + \frac{1}{2t}\right] N.e^{\frac{-t}{t}}$$

Figure 4 shows the effect on a histogram with no initial offset if an input V_{ext} goes from 0 at 50ps to 0.2V at 100 ps, then down to 0.15V at 200 ps

III. PRACTICAL CIRCUITS

Synchronizer circuits can be made from cross-coupled gates, together with a filter circuit, which prevents metastable levels reaching the following circuits. This arrangement is shown in Figure 5. Here when the clock goes low, one of R1 and R2 may go high just before the other. In our simulation the gate outputs both start high, but the filter outputs are low because the two p-type transistors are non-conducting. If both gate outputs go to a metastable level, the filter outputs remain low, and only when there is a difference of at least 1V between the gate outputs can the filter output start to rise, so that the filter output reaches 1.65V only when the high output gate is at about 2.4V, and the low output gate at about 0.7V. We used

PSPICE to find the output times for a range of input time differences between R1, and R2, and from these results plotted the event histograms of Figure 6 and Figure 7.

These measurements involve circuit simulations with time differences of 0.1ps or less, and the results become unreliable for differences below 0.0001ps because of the limited accuracy of the simulator, but down to this level they can be made accurately enough. Figure 6 shows the effect of the circuit with a filter, where the gate outputs both start high, and one of them must go below 0.7V to give a result. Output times are measured as the elapsed time after the last input goes high. In Figure 6 the initial slope is only slightly faster than the final slope, but the effect is more pronounced in Figure 7 where the outputs are taken from low threshold inverters with transistors sized the same as those in the filter. This threshold is about 0.1V below the metastable level. Here the final slope is slower because the loading on the bistable is greater, and the effect of the low threshold inverter on the early part of the slope of Figure 7 can be compared with that of Figure 3.

To confirm this result we made measurements using two oscillators on a MUTEX bistable with a circuit similar to Figure 5. This circuit was part of a 5 wire arbiter designed by Sun Microsystems, Inc. on 0.6μ silicon and the results are shown in Table 2. The slope of the events histogram was measured for input time differences between 30 ps and 1 ps, (the initial slope), and also below 0.01 ps where it should be close to t. In Figure 6 and Figure 7 these regions are 0.03 to 0.001 events, and below 0.00001. With a low threshold output inverter, both the theory and the simulations gave an initial slope of about 60% of the final value, but the high effective value of the filter threshold gave an initial slope much closer to the final slope both in the simulation and in the silicon.

	τ between 30-1ps	τ below 0.01ps	Initial slope
Theoretical low threshold	59	96	61%
Simulated low threshold	78	131	60%
Simulated with filter	122	127	96%
Measured with filter	99	106	93%

Table 2 Initial and final slopes

In most applications it is necessary to reduce the failure rate to a very low value, and therefore the value of t should be reduced to a minimum. Circuits called Jamb latches, based on inverters rather than gates have been proposed [2][8], because inverters have a higher gain, and less capacitance, than gates. These circuits are of two types as shown in Figure 8. Here, the bistable is reset by pulling node B to ground, and then set if both data and clock inputs are high, by pulling node A to ground. For correct operation, reset, data and clock transistors must all be made wide enough, when compared to the inverter devices, to ensure that the nodes are pulled down. Typically, that means that the reset transistor has the same width as the p-type transistors in the bistable, and the data transistor is wider.

Metastability occurs if the overlap of data and clock is at a critical value which causes node A to be pulled down below the metastability level, but node B has not yet risen to that level. This can be seen in Figure 9, where the data goes high at about 2.55 ns while the clock is high, then node A falls to about 1.1V, while node B rises to about 0.8 V. When the clock input goes low at 3 ns both node A and node B become metastable at about 1.5V, and the output taken from node B with an inverter whose threshold is 0.1V higher than the metastable level.

If the output is from node B, the response starts low, and is detected with a high threshold because it is going high, whereas if it is taken from node A, we have a low start and must use a low threshold inverter because the node is going low. Only one output inverter is connected to avoid loading the bistable, and the transistor widths are minimised. In the first circuit (node B) the events histogram should correspond to the low start, high threshold curve of Figure 3, and in the second (node A), to the high start, low threshold curve.

There are two ways in which the data and clock can be driven. If the data goes high first and then the clock low later, feedthrough from the later input has a lesser effect because it is connected to the lower transistor. We simulated both node A and node B circuits, and histograms produced from simulations are shown in Figure 10. Table 3 shows that the Node A circuit has both start and threshold on the same side of the metastable level, and is therefore equivalent to the high start high threshold case of Figure 3, whereas for Node B the start and threshold are on opposite sides, and so are equivalent to the low start case.

	Output gate threshold	Node A start level	Initial Slope	Final Slope
Node A output	Metastable -0.1V	-0.45V	200ps	95ps
Node B output	Metastable +0.1V	-0.45V	70ps	95ps

Table 3 Jamb latch results

The effect of feedthrough from the gate to the drain of the setting transistor connected to node A can be seen in Figure 11, where the clock goes high at 3 ns, and then later the data goes low. Here time is measured from the first input (the clock), and the output is taken from node B. This curve show significant differences to Figure 10, because we are measuring time from

the first (clock) edge rather than the last, and there is a pronounced peak at 3.79 ns caused by the negative going data edge at about 3.6 ns. Coupling through Miller capacitance forces node A lower and the peak is the result of this external input causing high outputs to be brought forward, as explained in section II. Similar effects have been reported in recent measurements on Jamb latch circuits [2]

The value of τ in these circuits is determined by the drive capability of the inverters, and the capacitive loading on the nodes. To reduce this loading, the output inverters should have small geometry, but the set and reset drive transistors in the Jamb latch cannot be reduced below a certain size, or the circuit will not function correctly. It is possible to overcome this problem by switching the bistable between an inactive (no gain) and an active (high gain) state. As the device moves between the two states, only a small drive is necessary to cause the output to switch one way or the other, and if this drive is small, it can be maintained in the fully active state without switching the output further. Figure 12 shows a circuit based on this principle, in which the latch is activated by the low to high transition of the clock, and one of the B_1 and B_0 nodes goes low, giving a high output on V_1 if data is high before the clock. This is similar to the Q-Flop proposed by Rosenberger et al, [9]. The p-type data drive transistors are less than ¼ the size of those in the Jamb latch, and so load the bistable much less.

The simulated performance of this circuit is shown in Figure 13. The output always takes at least 440 ps from the clock, because of the low drive from the data input, and the data must be present before the clock, but the slope of curve was measured at less than t = 75 ps. One event on the scale in this histogram represents a probability of 1 of recording exit from metastability within a 1 ps interval if there are 10^{10} synchronisations. To achieve an MTBF

of 10^8s in a system with 1000 synchronizers operating at 1GHz we would require less than 10^{-11} events in a 1ns interval. At a time 2 ns later than the clock, the number of metastable events expected from both circuits are similar at 10^{-9}, but 10^{-12} reliability is achieved at 2.5 ns after the clock in the fast synchronizer compared to 2.6 ns for the Jamb latches. From that point onwards the Q-Flop always has the advantage because the value of τ is significantly lower, since for similar transistor geometries in the bistable, loading effects from the set and reset mechanism is always less.

	Min time from clock for 10^{-9} reliability	**Min time from clock for 10^{-12} reliability**
Node A	**2.04**	**2.66**
Node B	**1.97**	**2.59**
Q-Flop	**1.98**	**2.5**

Table 4 Reliabilty comparison

IV. NOISE

The effect of noise is that the output of a synchronizer becomes non-deterministic, and an individual output time no longer depends primarily on the inputs. This only occurs at very small inputs, and by measuring the initial voltage difference between node A and node B in a Jamb latch produced by very small changes in the overlap of clock and data, we deduced that 1.04 mV was produced by a 0.1 ps timing change. To accurately predict the effects of noise in the linear region, this measurement must be done with small voltages, and if the measurement were done in technology smaller than 0.6μ we believe that the timing change required would be correspondingly smaller.

In order to measure the internal noise we designed the comparator circuit of Figure 12. This circuit has an analog input stage that drives the bistable with a small current difference. The device was fabricated using an AMS 0.6μ two layer metal CMOS process, and we measured the noise in the bistable when it was metastable by continuously clocking the device, while observing the proportion of outputs with V_1 high as the input voltage from a variable power supply was slowly varied. A digital voltmeter was used to measure the input voltage between *V*- and *V*+, and the average level of the digital output was measured with an analog oscilloscope. Using a very low bandwidth analog voltage to give very small inputs to the latch avoids the jitter problems of maintaining the very precise timing between data and clock required if time differences are used to measure noise effects. Our comparator circuit has a differential preamplifier input, followed by a bistable latch, and is shown in Figure 14. When *V*+ is very close to *V*- the bistable output is determined mainly by thermal noise on the B nodes, since the RMS noise voltage on these nodes is greater than the offset due to the input. Under these circumstances the random nature of the output can be clearly observed, and as the input voltage changes from negative through zero to positive the proportion of V_1 high outputs goes from zero to 100%. Plotting the change in this proportion for a given input change against the actual input for one sample of the fabricated devices gives the graph of Figure 15, where the points measured are compared with a Gaussian curve with an equivalent RMS noise value of 3.3mV at the input. Mesaurements over a number of samples gave noise values at the input between 1.5 and 3.5mV.

Thermal fluctuations in an FET give rise to drain current noise and gate noise. Van der Ziel [10], gives drain current noise as $i_{nd}^{\ 2} = 4kTgg_{d0}\Delta f$, where g_{d0} is the drain-source conductance, and the parameter γ has a value typically between 2 and 3. The equivalent gate

noise voltage is approximately $e_{ng}{}^2 = \frac{4kTd\Delta f}{5g_{d0}}$ where δ is typically 5-6. Noise at nodes B_1 and B_0 has a bandwidth limited by the capacitance, C, to $\frac{g_d}{4C}$, and is in the range 0.4 mV to 0.5 mV for our process, depending on the values of γ and δ. Between nodes B_1 and B_0 this is $\sqrt{2}$ greater, or between 0.55 mV and 0.7 mV. Similarly the noise between A_1 and A_0 is about 1 mV, but this only makes a small contribution towards the noise at B, because the gain from A to B is 1/(4.55). Total thermal noise should be therefore equivalent to between 1.65mV and 2.31mVat the input. Our measurement of approximately 2.5mV RMS corresponds to about 0.8mV total between B_1 and B_0. A voltage of 1 mV is given by a time difference of about 0.1ps at the inputs of a Jamb latch, which corresponds to an event level of 10^{-4} on our histograms, and is not far from the point where the slope becomes constant, sometimes termed 'deep metastability'.

We believe that this is not necessarily connected with the dominance of noise in deep metastability. Couranz and Wann [7], have demonstrated both theoretically and experimentally that for a uniform distribution of initial condition voltages, as would be the case for the histograms presented here, the probability of escape from metastability with time is given by: $P_e(t) = 1 - e^{\frac{-t}{t}}$ This function does not change with the addition of noise because of the uniform distribution of initial conditions. For each noise contribution that moves a trajectory away from metastability, there will, on average, be another compensating noise contribution that moves a trajectory towards metastability. The result, in a statistical measurement, is that the event histogram will be unchanged

V. CONCLUSIONS

Synchronizer circuits have been shown to produce event histograms which do not exhibit a constant value of t. Initially, this may be higher, or lower than the final value, depending on the circuit used. We have shown that these effects, which include a reduction in the value of t in the early part of the histogram to as much as 60% of the final value can be explained by a careful application of the existing theory. These variations in t are accounted for by the size of the initial offset from the metastability level, and the point on the trajectory at which the exit from metastability is defined.

Measurements on a range of circuits have demonstrated that simple Jamb latches perform better in synchronizers than bistables made from NAND gates, but a further reduction in total synchronization time can be achieved by a bistable that is switched between inactive and active by the clock, because the set and reset transistor sizes can be reduced.

We have measured the thermal noise in a bistable circuit, and shown that it is similar to the value expected, and exhibits a Gaussian distribution. If this is the case, and the measurement of circuit characteristics is done using a uniform distribution of input conditions, we would not expect to see any modification of the histogram with noise, but noise does affect the behavior of synchronizers with equivalent inputs less than the noise level. For metastability times of $8t$ or more, well within the normal operating range of a synchronizer, the output becomes non-deterministic, and neither the final value nor the individual output time depend primarily on the inputs. This may, in fact, be useful, since it means that inputs that are always close in time, do not always produce long metastability times.

VI. REFERENCES

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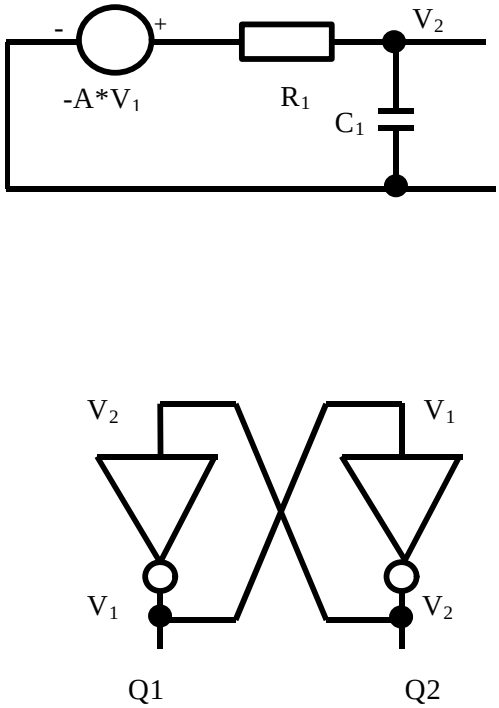

Figure 1 Gate small signal model and bistable

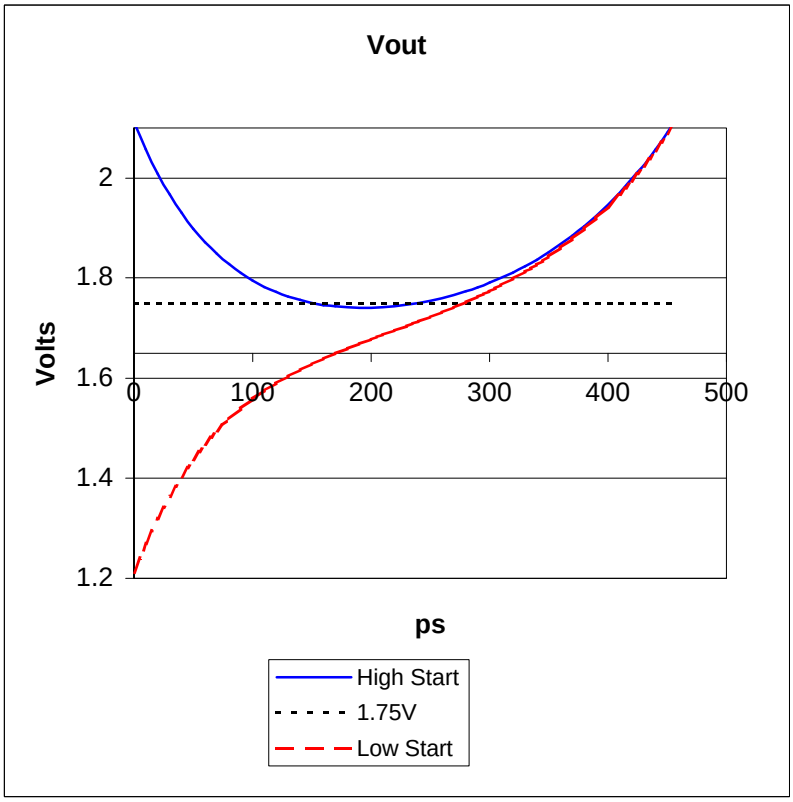

Figure 2 Model response

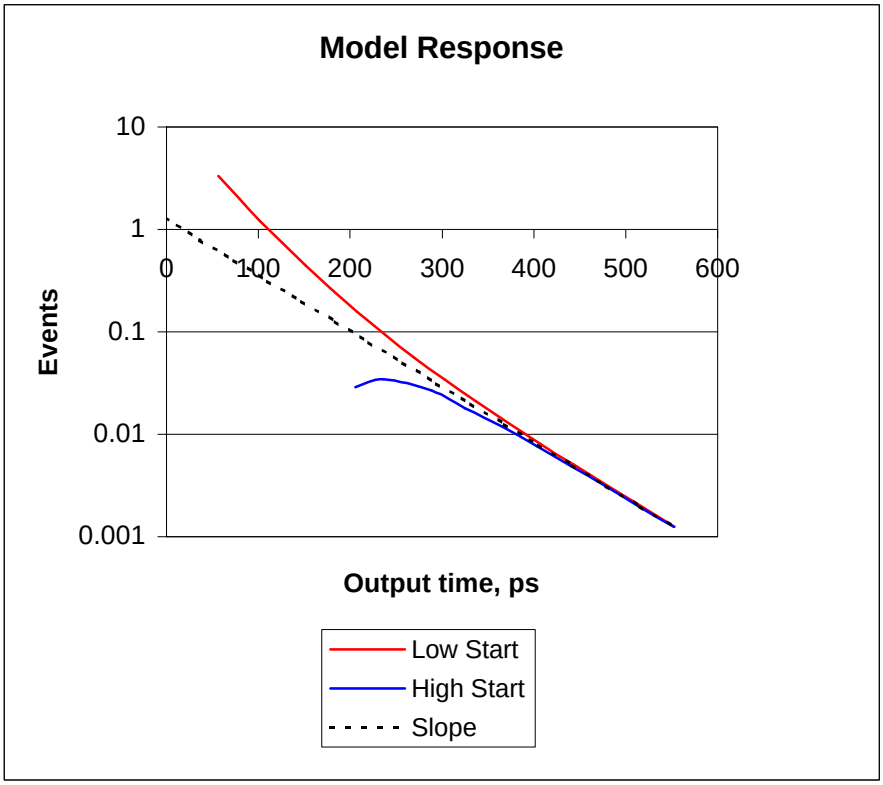

Figure 3 Events per unit time as a function of metastability time

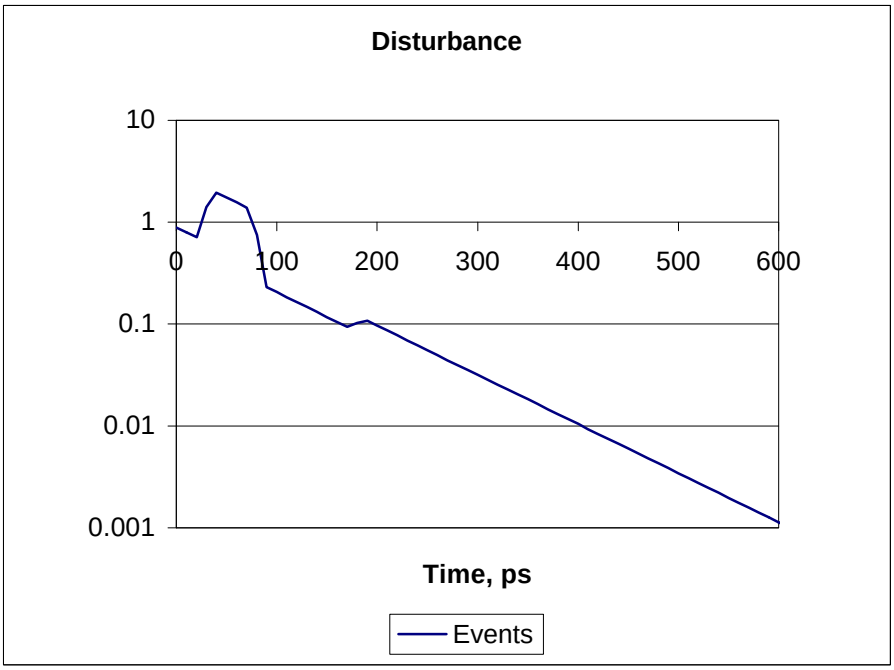

Figure 4 Effect of external input

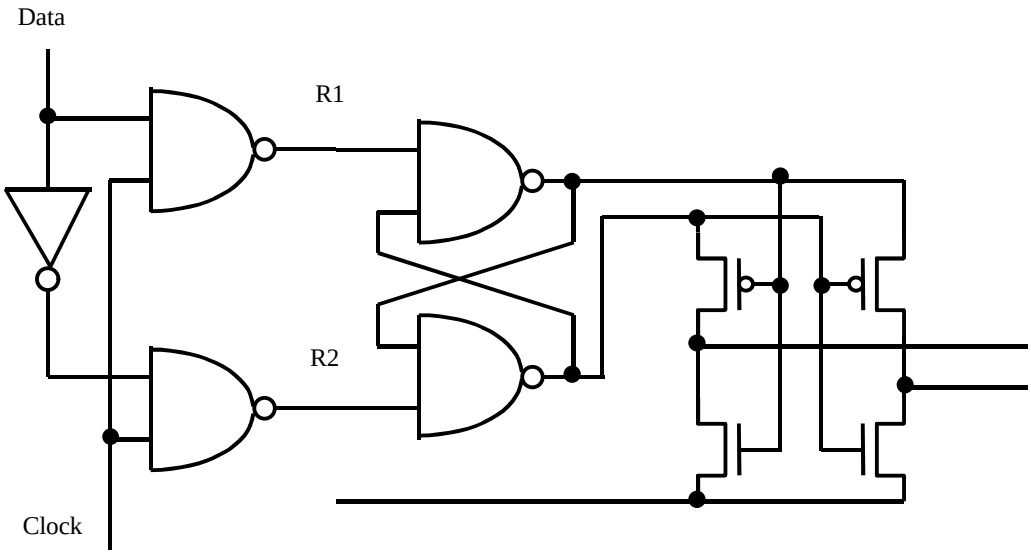

Figure 5 Cross-coupled gates with filter

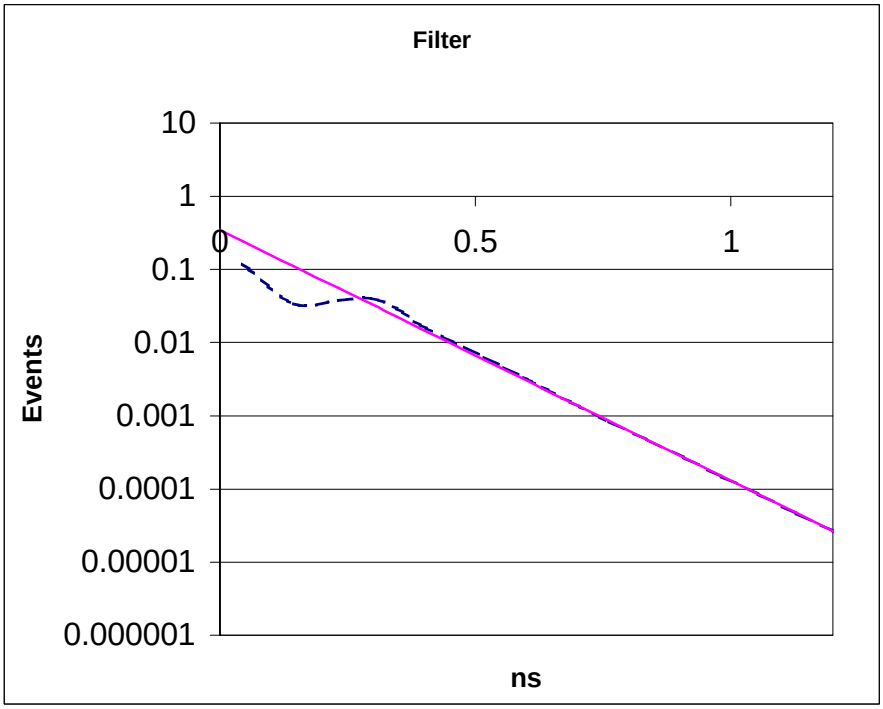

Figure 6 Gates with filter

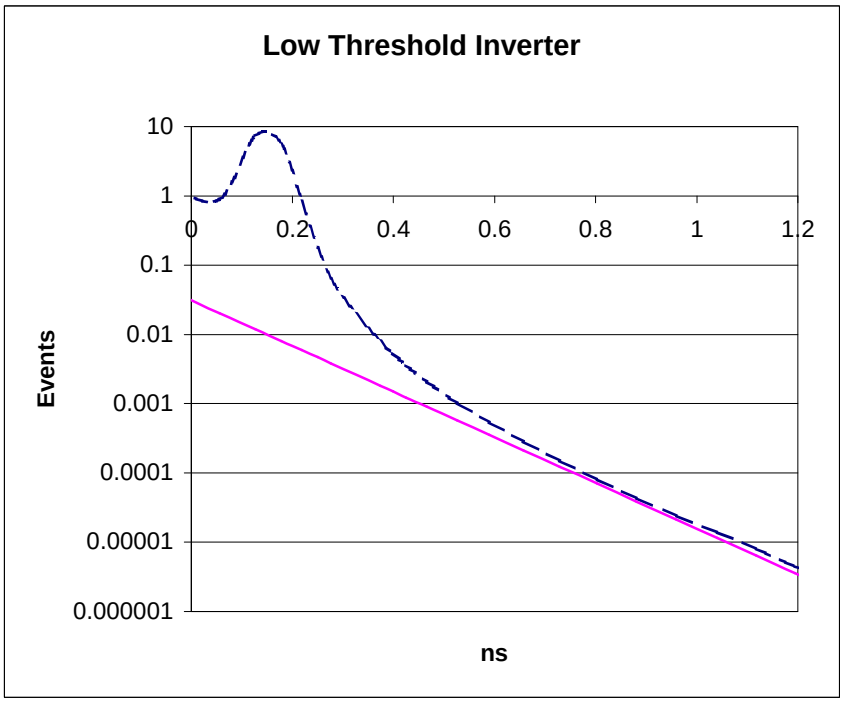

Figure 7 Gates with low threshold output inverters

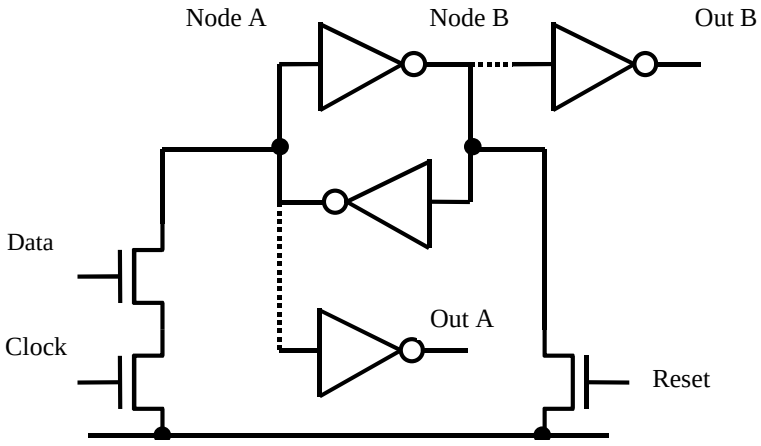

Figure 8 Jamb latch

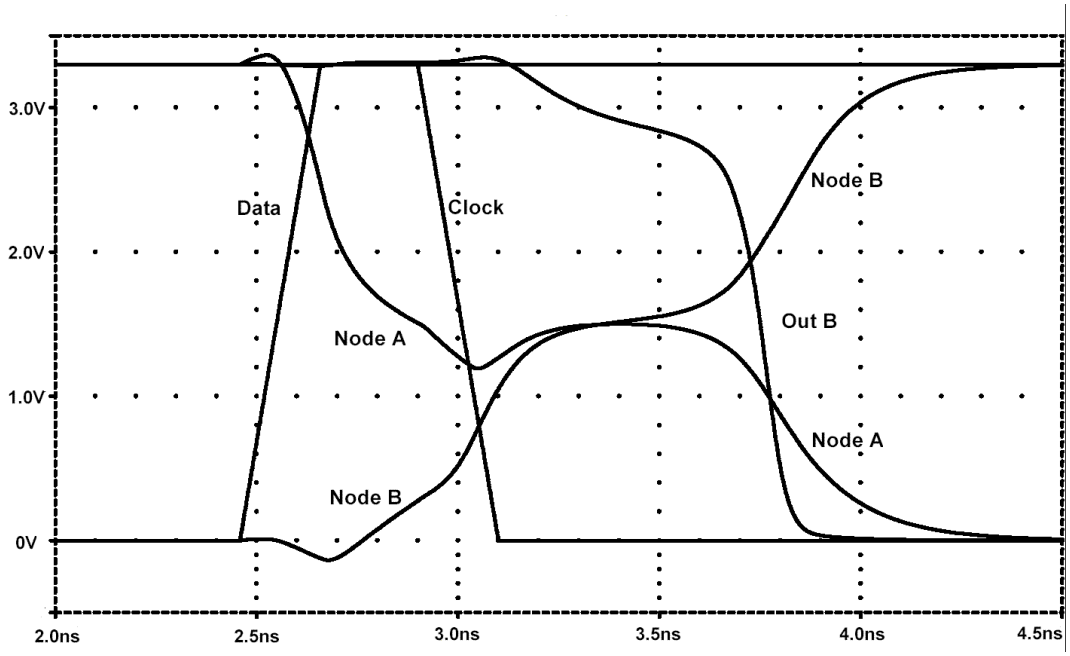

Figure 9 Jamb latch waveforms

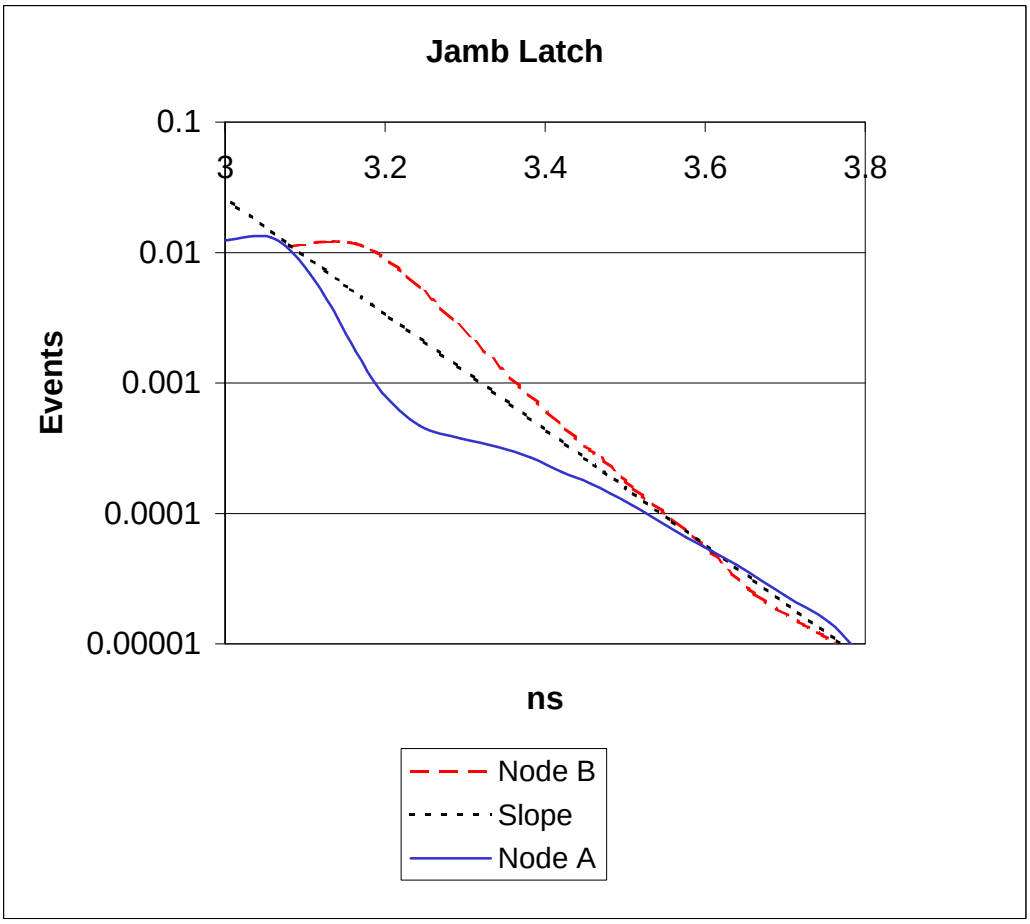

Figure 10 Jamb latch histograms

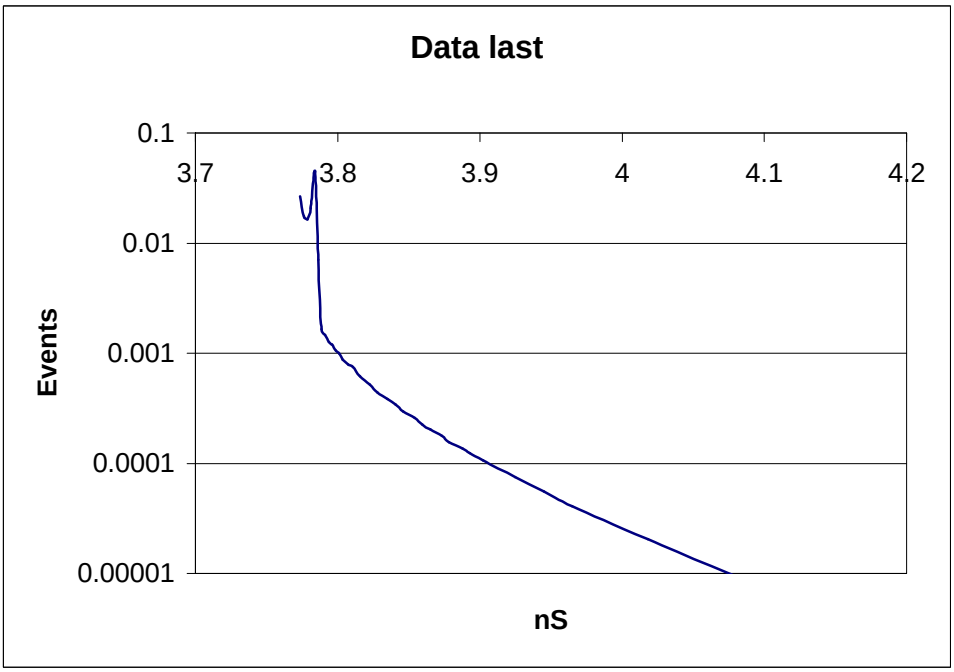

Figure 11 Clock first, Data last, Node B

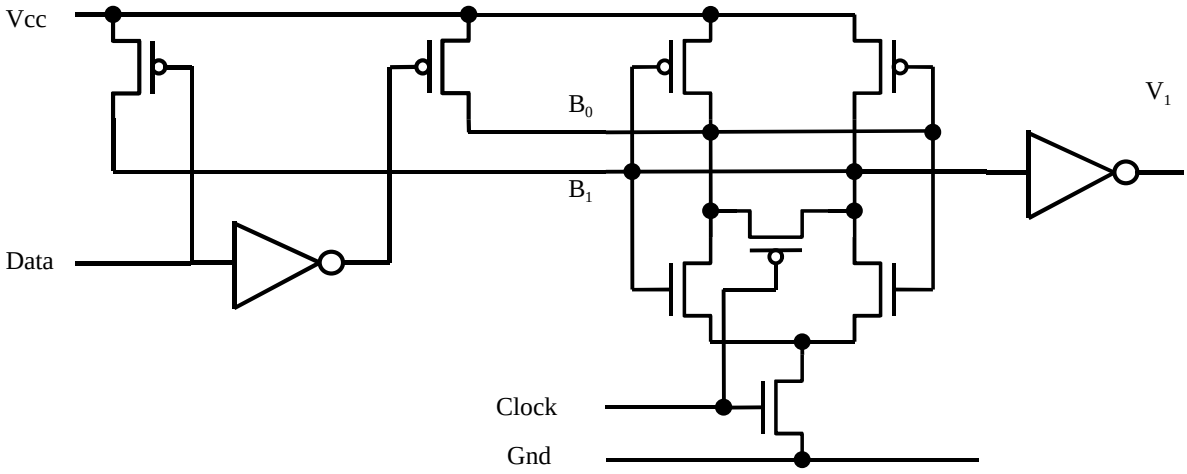

Figure 12 Fast synchronizer

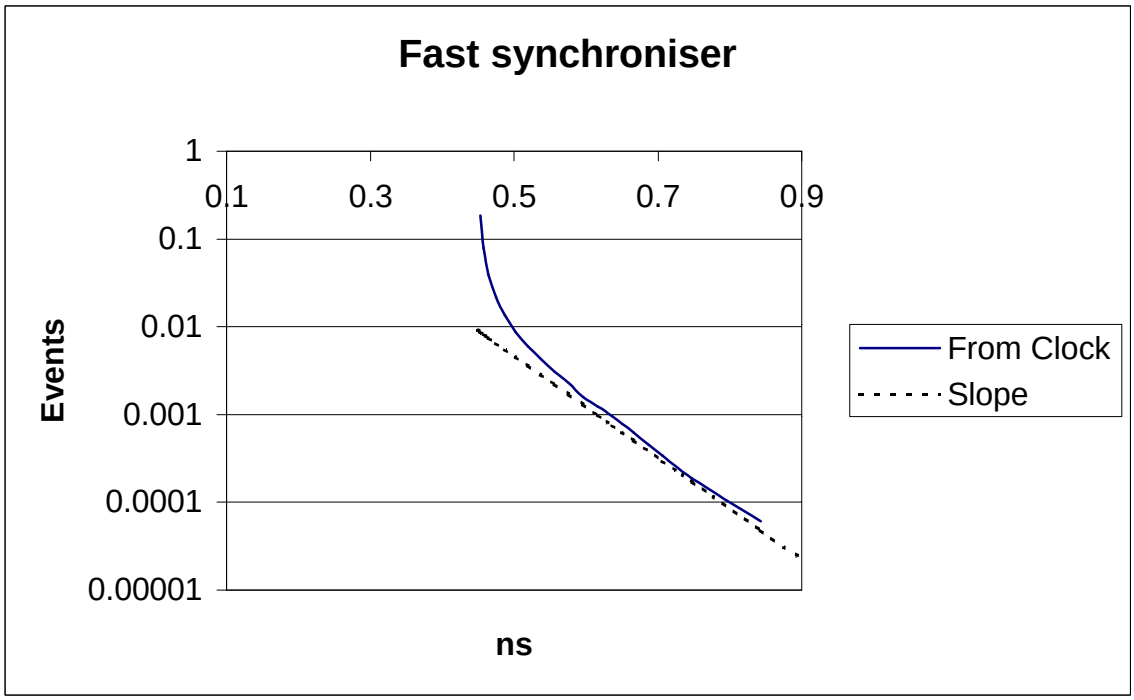

Figure 13 Fast synchronizer characteristics

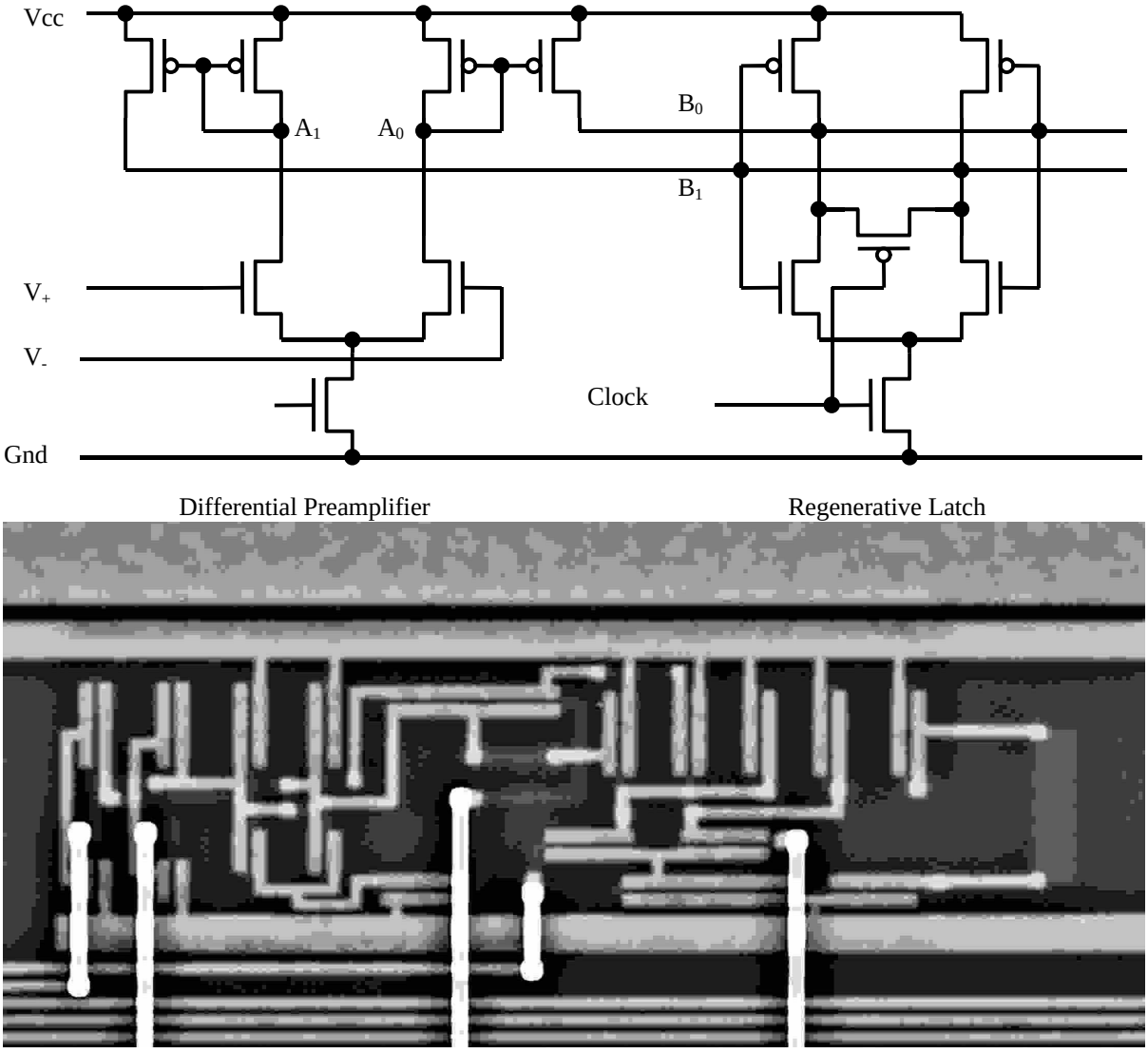

Figure 14 Noise measurement circuit and SEM

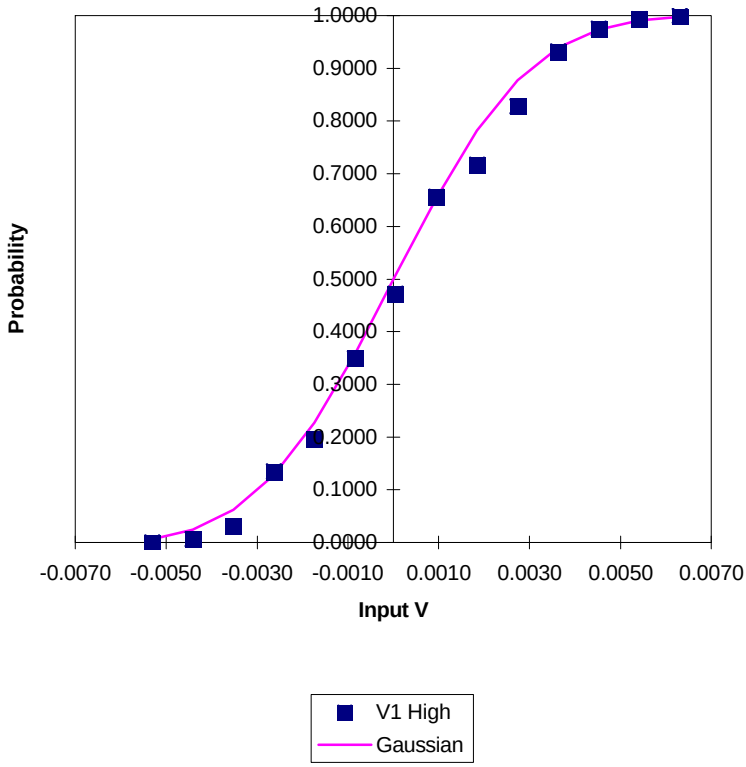

Figure 15 Probability of V_1 high