CALL FOR PAPERS

IEEE Transactions on VLSI Systems Special Section on

Asynchronous Circuits and Systems

The number of gates on a chip is quickly growing toward and beyond the one billion mark. Keeping all the gates running at the beat of a single or a few rationally related clocks is becoming difficult. In static timing analysis, process variations and signal integrity issues stretch the timing margins to the point where they become too conservative and result in significant overdesign. The importance and difficulty of such problems push some developers to once again turn to asynchronous alternatives.
This special section will report on recent advances in the development of asynchronous, unclocked and latency-tolerant circuits and systems. Topics of interest include, but are not limited to:

- Mixed synchronous/asynchronous architectures, interfaces, and circuits
- Design, synthesis and verification techniques for GALS systems
- High-speed/low-power asynchronous logic, memories, and interconnects
- High-level design and synthesis of self-timed circuits
- Physical design of unclocked logic and pipelines
- Test, reliability, security, and radiation tolerance
- CAD for asynchronous design and validation
- Asynchronous system-on-a-chip (SoC)
- Asynchrony and latency tolerance in system-level design
- Asynchronous design for manufacturing

Authors are encouraged to submit high-quality research contributions that will not require major revisions. Extensions of papers presented at ASYNC'08 – International Symposium on Asynchronous Circuits and Systems, April 7-10, 2008, Newcastle upon Tyne, United Kingdom (http://async.org.uk/async2008) are especially encouraged. Please identify clearly the additional material from the original symposium paper in your submitted manuscript (about 30% new technical content is required). Submissions of relevant original work not presented at ASYNC'08 are also welcome. All manuscripts are subject to standard IEEE Transactions on VLSI Systems review process. Prospective authors should submit their manuscripts electronically on the TVLSI Web site: http://tvlsi-ieee.manuscriptcentral.com/
Authors should clearly identify their papers as submissions for the "Special Section on Asynchronous Circuits and Systems" on their manuscript and in the Note to Editor field of the web submission form. Instructions on how to submit a paper can be found at http://tvlsi-ieee.manuscriptcentral.com/ and authors can contact Ms. Stacey Weber sweber@princeton.edu for further assistance.

Important Dates:

Submission Deadline: July 1, 2008
Notification Date: October 1, 2008
Final Version Due: November 3, 2008
Target Publication Date: 3rd Quarter, 2009

Guest Editors:

Jordi Cortadella *(Universitat Politècnica de Catalunya, Spain)* jordi.cortadella@upc.edu
Alexander Taubin *(Boston University, USA)* taubin@bu.edu