Dual-channel access mechanism for cost-effective NoC design

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Outline

- Background
- Single-channel access mechanism
- Dual-channel access mechanism
- Experimental results
- Conclusions

Background

- Network-on-Chip (NoC) paradigm is emerging as a new design methodology when entering the billion-transistor era.

- NoC design is different from traditional network design because of the following three characteristics:
  - Resource-limited;
  - Latency-sensitive;
  - Traffic predictability.

- NoC design must be a trade-off between performance and cost!
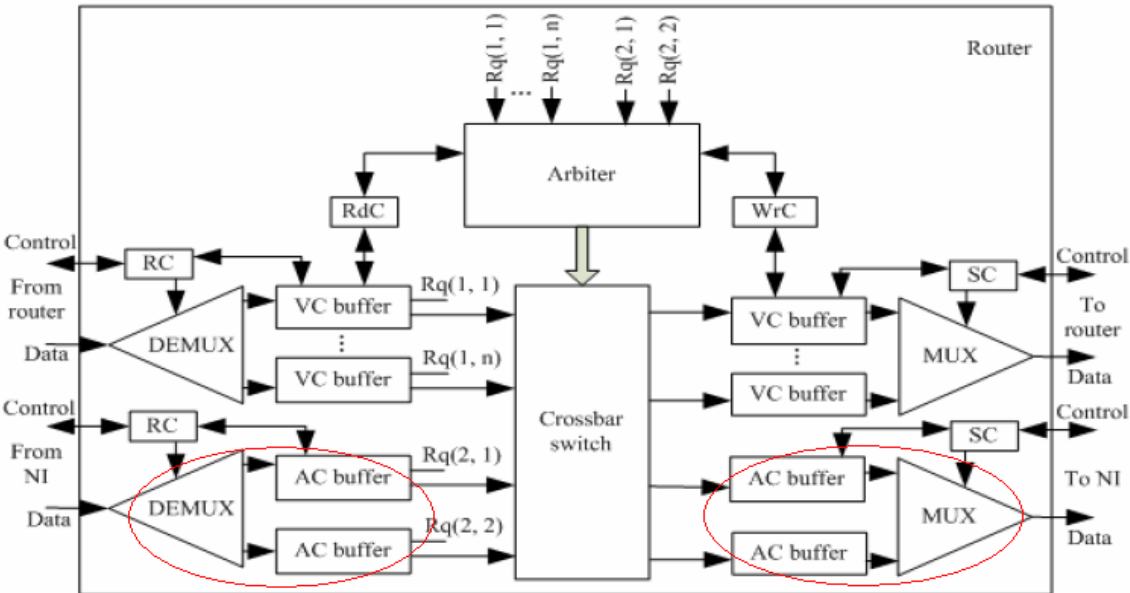
Single-channel access mechanism
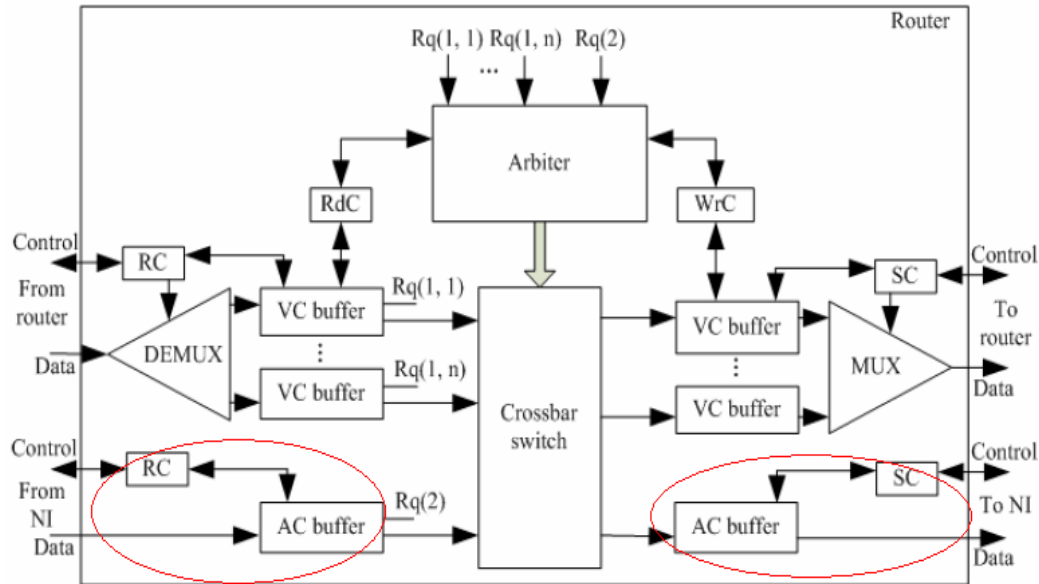
(1) Router design in single-channel access mechanism

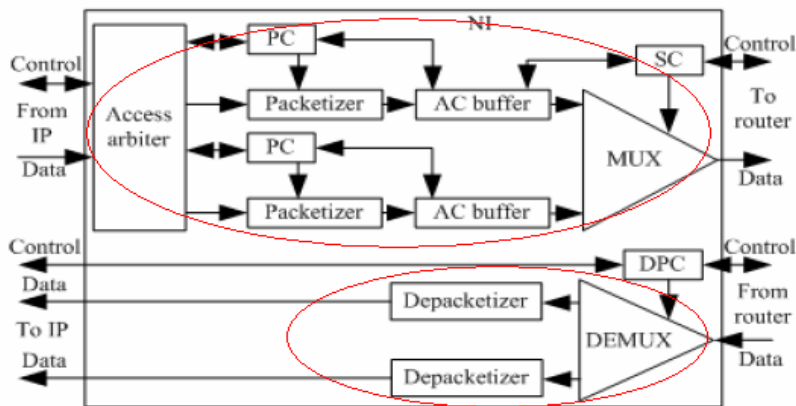(2) NI design in single-channel access mechanism
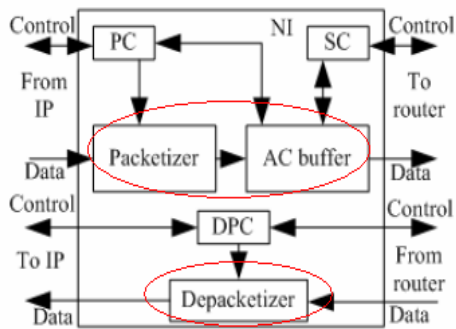
Figure 1. Router and NI design in single-channel access mechanism.

- In this mechanism, every IP only has one channel to enter the network even when more than one virtual channel is available.

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Dual-channel access mechanism

(1) Router design in dual-channel access mechanism

(2) NI design in dual-channel access mechanism

Figure 2.   Router and NI design in dual-channel access mechanism.

- Two access channels are provided for every IP.

- Make sure that NoC works at the state of "light-congestion" all the time, thus this mechanism make good use of network capacity and improve the performance.

Dual-channel access mechanism

- Static allocation method is used in the access arbiter since the traffic of NoC is predictable.

- Detailed description:
  - We pre-allocate the access channels for data of different destination IPs according to their average traffic load.
  - The principles of the pre-allocation process:
    - Data of the same destination IP is allocated to the same access channel; therefore, the transmission order is guaranteed.
    - Make sure that the average traffic loads of both access channels are as close as possible so as to increase the utilization of access channels.

Experimental results

- Parameters in our simulation platform

Table 1

Parameter	Value
Packet length	16 flits
Topology	2D-mesh
Number of IPs	16
Buffer size of every virtual channel	3 flits
Buffer size of every access channel	3 flits
Number of bits in every flit	32
Total flit number for simulation	120000

- Comparison of Area

Table 2

	Single-channel access	Dual-channel access	
	Area (NAND gates)	Area (NAND gates)	Increase
router	95242	100709	
NI	2323	4703	
Total	97565	105412	8.04%

Experimental results

- ## Comparison of Performance

Table 3

Configuration parameters			Single-channel access	Dual-channel access	
				value	improvement
TL= 0.4050 flits/ IP / routing clock cycle	F2:F1=2:1; 3 virtual channels	Th	0.4046	0.4045	-0.02%
		La	11.3	11.1	1.77%
	F2:F1=2:1; 6 virtual channels	Th	0.4046	0.4045	-0.02%
		La	11.2	9.1	18.75%
	F2:F1=4:1; 3 virtual channels	Th	0.4047	0.4046	-0.02%
		La	9.8	9.9	-1.02%
	F2:F1=4:1; 6 virtual channels	Th	0.4047	0.4046	-0.02%
		La	9.6	7.7	19.79%
TL =0.9735 flits/ IP / routing clock cycle	F2:F1=2:1; 3 virtual channels	Th	0.7078	0.9699	37.03%
		La	621.4	30.1	95.16%
	F2:F1=2:1; 6 virtual channels	Th	0.7089	0.9699	36.82%
		La	618.1	24.5	96.04%
	F2:F1=4:1; 3 virtual channels	Th	0.7528	0.9703	28.89%
		La	509.3	15.3	97.00%
	F2:F1=4:1; 6 virtual channels	Th	0.7701	0.9703	26.00%
		La	480.1	11.4	97.63%

Note: "F2" is the frequency of all the clocks used among routers, NI and IP; "F1" is the frequency of all the clock used inside routers; routing clock cycle is the reciprocal of "F1"; "Th" and "La" represents throughput and latency respectively.

Conclusions

- Dual-channel access mechanism increases the throughput and cuts down average latency greatly with reasonable implementation cost, especially when the traffic load is high.

- Thus, dual-channel access mechanism is more cost-effective than single-channel access mechanism.

- Thank you for your attentions!