Coping with Soft Errors in Asynchronous Burst-Mode Machines

Sobeeh Almukhaizim
Computer Engineering Dept.
Kuwait University, Kuwait

Feng Shi & Yiorgos Makris
Electrical Engineering Dept.
Yale University, USA

4/11/2008
Sources of Soft Errors

“Solar Particles”
Affect satellites; may also penetrate to Earth

“Galactic Particles”
Are high-energy particles that penetrate to Earth’s surface, through buildings and walls

- High-energy particles collide with silicon atoms
- Collision generates a voltage pulse at impact site
- Under certain conditions, it may produce a soft error
• Integrated circuits (synchronous & asynchronous) will require methods to tolerate / mitigate soft errors and ensure reliability
Soft Error Tolerance & Mitigation in ASYNC

- Previous studies targeted Quasi Delay-Insensitive (QDI) circuits
- SEU-tolerant QDI circuits (W. Jang & A. Martin, ASYNC, 156-165, 2005):
  - Gate-level fine-grain duplication and double-checking
  - Fine granularity results in high overhead
  - Susceptibility or sensitivity is defined with respect to the number of errors at the inputs of the C-element that are necessary to flip its state
  - Several soft error mitigation (or hardening) methods are presented
Asynchronous Burst-Mode Machines

- Interaction between the circuit and its environment happens in Bursts:
- Input Burst: a set of bit changes in any order and at any time
- Outputs and state do not change during an input burst
- Once the input burst is complete, the circuit responds with a hazard-free output burst

Particle strikes may cause logic errors or hazards
Coping with Soft Errors in ABMMs

Methods to Cope with Soft Errors in ABMMs

Tolerance Techniques
- TMR-Based

Mitigation Techniques
- Duplication-Based

ASYNC’08
TMR-based Soft Error Tolerance in ABMMs

- C-element used as majority voter
- Strikes at state-line C-elements not tolerated
Duplication-based Soft Error Tolerance

- Observation: 2-input C-elements are sufficient to tolerate one failing module (i.e., only one replica is needed)

- Strikes at state-line C-elements still not tolerated
Tolerating Errors on State-Line C-Elements

• Proposed Solution: cross-coupled structure of C-elements

• All strikes at state-line C-elements are now tolerated
Example

1. Insert original circuit
2. Insert duplicate circuit
3. Insert state-line C-elements
4. Insert output C-elements

ASYNC’08
### Experimental Results

**Duplication-based Soft Error Tolerance**

<table>
<thead>
<tr>
<th>Circuit Name</th>
<th>I/S/O</th>
<th>Original</th>
<th>Duplicate</th>
<th>C-elements</th>
<th>Total</th>
<th>Overhead</th>
</tr>
</thead>
<tbody>
<tr>
<td>hp-ir</td>
<td>3/1/2</td>
<td>8</td>
<td>8</td>
<td>18</td>
<td>34</td>
<td>325.00%</td>
</tr>
<tr>
<td>concur-mixer</td>
<td>3/2/3</td>
<td>16</td>
<td>16</td>
<td>33</td>
<td>65</td>
<td>306.25%</td>
</tr>
<tr>
<td>tangram-mixer</td>
<td>3/1/2</td>
<td>10</td>
<td>10</td>
<td>18</td>
<td>38</td>
<td>280.00%</td>
</tr>
<tr>
<td>rf-control</td>
<td>6/3/5</td>
<td>37</td>
<td>37</td>
<td>51</td>
<td>125</td>
<td>237.84%</td>
</tr>
<tr>
<td>while_concur</td>
<td>4/2/3</td>
<td>24</td>
<td>24</td>
<td>33</td>
<td>81</td>
<td>237.50%</td>
</tr>
<tr>
<td>barcode</td>
<td>13/4/17</td>
<td>172</td>
<td>172</td>
<td>99</td>
<td>443</td>
<td>157.56%</td>
</tr>
<tr>
<td>p2</td>
<td>8/4/16</td>
<td>192</td>
<td>192</td>
<td>96</td>
<td>480</td>
<td>150.00%</td>
</tr>
<tr>
<td>p1</td>
<td>13/4/14</td>
<td>238</td>
<td>238</td>
<td>90</td>
<td>566</td>
<td>137.82%</td>
</tr>
</tbody>
</table>

Area overhead seems excessive for small circuits: cost inflated due to proportionately large number of C-elements over logic gates, and the rather expensive C-element implementation used.

4/11/2008
Coping with Soft Errors in ABMMs

Methods to Cope with Soft Errors in ABMMs

Tolerance Techniques

Mitigation Techniques

- Soft error susceptibility estimation
- Sensitive gates
- Sensitive complete logic cones
- Sensitive partial logic cones
Soft Error Susceptibility Estimation

- A hazard-aware asynchronous fault simulator is needed (SPIN-SIM: F. Shi and Y. Makris, ITC, 597-606 (2004))
- Fault simulate & construct a *soft error susceptibility table* \( (\text{sest}) \)
- Asymmetric soft error susceptibility of gates in different levels
- Enables judicious selection and replication in a partial duplicate

<table>
<thead>
<tr>
<th>State &amp; Input Burst Pair</th>
<th>Potential SETs</th>
<th>( f_i )</th>
<th>( f_j )</th>
<th>( f_k )</th>
</tr>
</thead>
<tbody>
<tr>
<td>SIB1</td>
<td>11000</td>
<td>00000</td>
<td>00001</td>
<td></td>
</tr>
<tr>
<td>SIB2</td>
<td>01001</td>
<td>11001</td>
<td>..</td>
<td>11001</td>
</tr>
<tr>
<td>SIB_m</td>
<td>11001</td>
<td>00010</td>
<td>..</td>
<td>00000</td>
</tr>
</tbody>
</table>

\[
\text{susc}(G_q) = \frac{\sum_{s}^{m} \sum_{j=s+1}^{s+k_q} E(\text{sest}[i,j])}{m \cdot k_q} \quad \text{, where } s = \sum_{l=1}^{q-1} k_l \\
\text{SER(ABMM)} = \sum_{q=1}^{n} \text{sest}(G_q)
\]

4/11/2008
Duplication of Sensitive Gates

- Using a duplication-based soft error tolerant ABMM:
  1. Gates are removed from the first level of the duplicate in an increasing order of their soft error susceptibility.
  2. Fan-outs are driven by the corresponding gate in the original ABMM.
  3. Area and soft error tolerance are updated accordingly.

Cost: 87%
Tolerance: 68%

4/11/2008
Duplication of Complete Sensitive Logic Cones

• Output/State logic cones also have an asymmetric susceptibility:
  • Select a subset that meets an area target & whose replication maximizes the number of tolerated pairs of SIBs & SETs

• Modeled as an ILP:

\[
Tol(Y_k, i, j) = \begin{cases} 
1, & \text{if } Y_k.VT(sest[i, j]) = 0 \\
0, & \text{if } Y_k.VT(sest[i, j]) > 0 
\end{cases}
\]

Maximize \[\sum\sum Tol(Y_k, i, j), \text{ subject to:} \]

(i) \[C_k < \text{Cost} \]

(ii) \[X_s \in \{0, 1\}, \text{ for } 1 \leq r \leq s\]

Cost: 60%
Tolerance: 47%

Y0 & \(w\) not protected

\(w\) & \(w\) not protected

\(Y_0\) & \(Y_1\) have complete protection

4/11/2008

ASYNC’08
Duplication of Partial Sensitive Logic Cones

- Combines the previous two approaches:
  - Explores the asymmetric susceptibility of gates and output/state lines

Cost: 50%
Tolerance: 24%

Drives fan-out of removed gate not protected partial protection
Experimental Results

2-level ABMMs

- Achieved tolerance is commensurate with the area overhead
- The partial logic cones mitigation method is consistently better
Experimental Results

Multi-level ABMMs (new release by Columbia Univ.)

Cost: 70%

Tolerance: 84%

Multi-level implementation significantly improves the tradeoff between area overhead & achieved soft error tolerance
Summary

• Soft error tolerance in ABMMs
  ➔ Duplication-based solution that improves upon TMR
  ➔ Cross-coupled C-element structure for state-line protection

• Soft error mitigation in ABMMs
  ➔ Enables exploration of the trade-off between the achieved soft error tolerance and the incurred area overhead
  ➔ Driven by soft error susceptibility estimation via hazard-aware asynchronous fault simulator (SPIN-SIM)
  ➔ Yields 3 progressively more powerful partial duplication options