

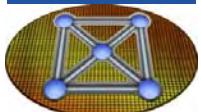


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Statistical Device Variability and its Impact on Design

Asen Asenov

Device Modelling Group
University of Glasgow





Summary

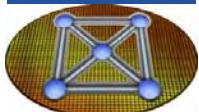
- Motivation
- Deterministic variability
- Statistical variability
- Impact on circuits
- EU variability projects
- Conclusions





Summary

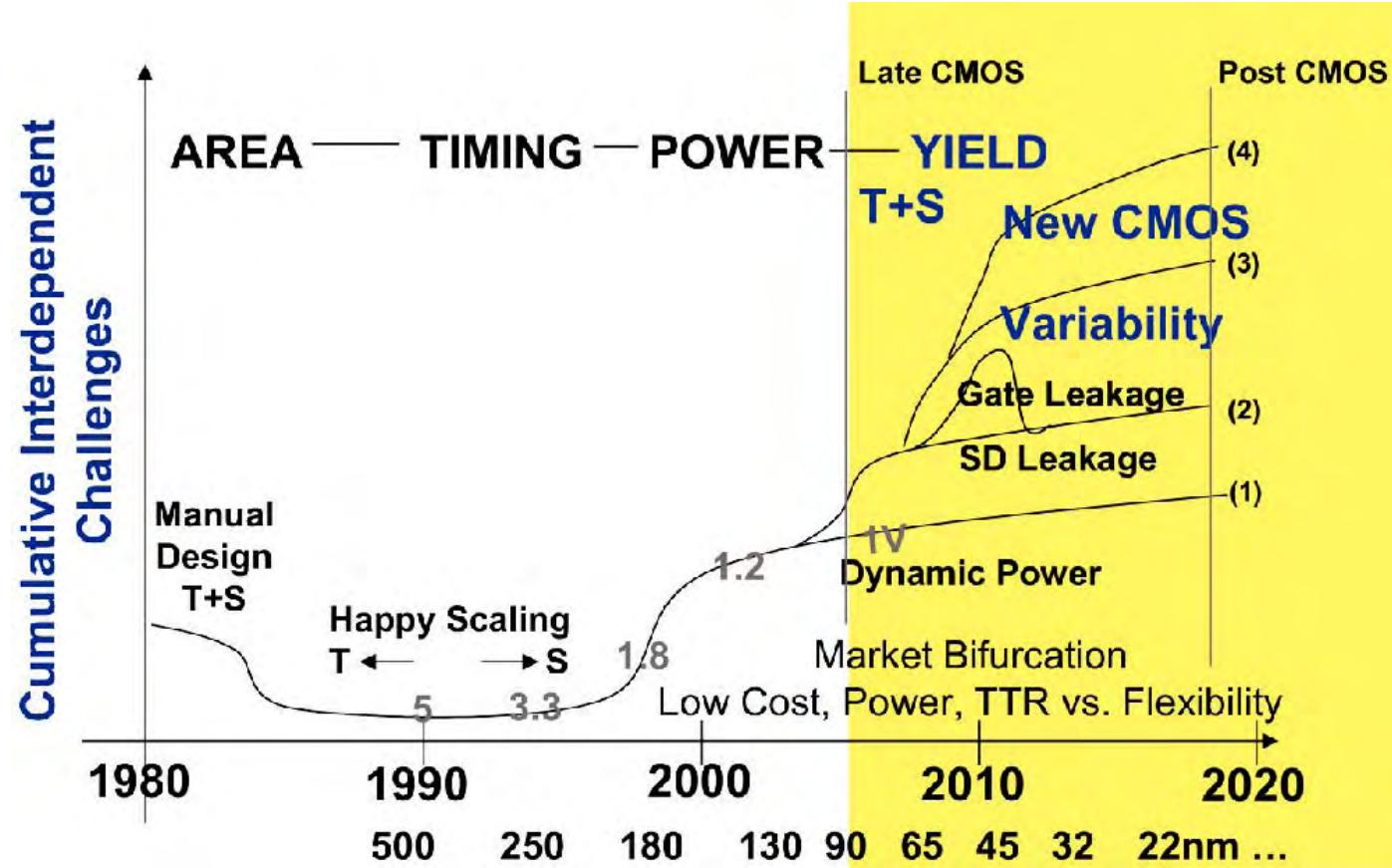
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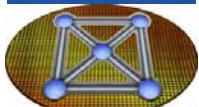
The variability is becoming a major headache



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G. Declarck, Keynote talk, VLSI Technol. Symp. 2005



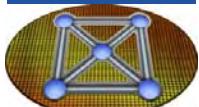
The local stochastic variability becomes a major source of concern



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| | | Process | Environment | Temporal |
|-------------|---------------|---|--|---|
| Global | Deterministic | $\langle L_o \rangle$ and $\langle W \rangle$ $\langle \text{layer thicknesses} \rangle$ $\langle R \rangle$'s $\langle \text{doping} \rangle$ $\langle V_{\text{body}} \rangle$ | T environment range V_{dd} range | $\langle \text{NBTI} \rangle$ Hot electron shifts |
| Local | Deterministic | OPC Phase shift Layout mediated strain Well proximity | Self-heating IR drops | Distribution of NBTI Voltage noise SOI V_{body} history Oxide breakdown history |
| Across-chip | Stochastic | Random dopants Line Edge Roughness Poly Si granularity Interface roughness High-k morphology | | |
| Across-chip | | Line width due to pattern density effects | Thermal hot spots due to non-uniform power dissipation | Computational load dependent hot spots |

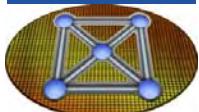
After D. J. Frank, IBM





Summary

- Motivation
- **Deterministic variability**
- Statistical variability
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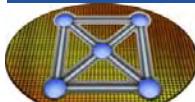


OPC and strain related variability

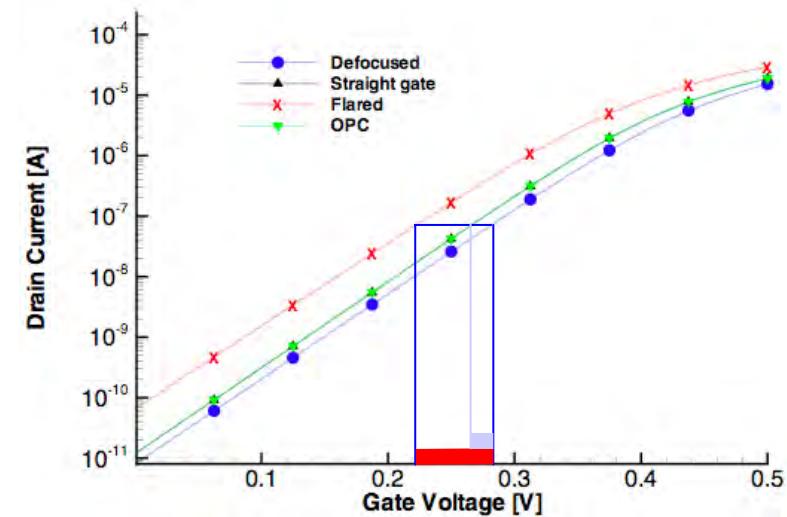
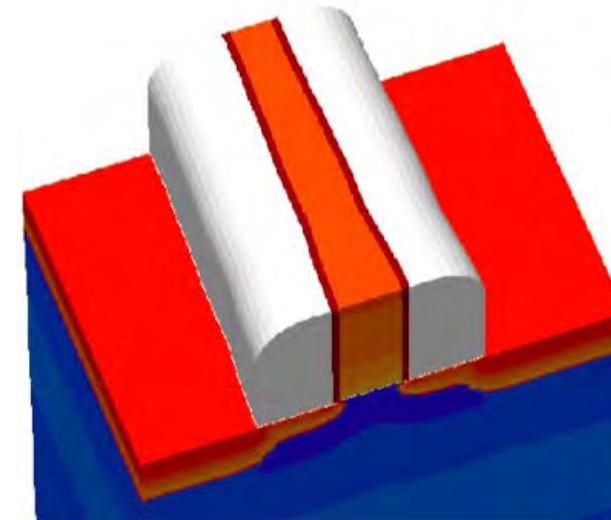
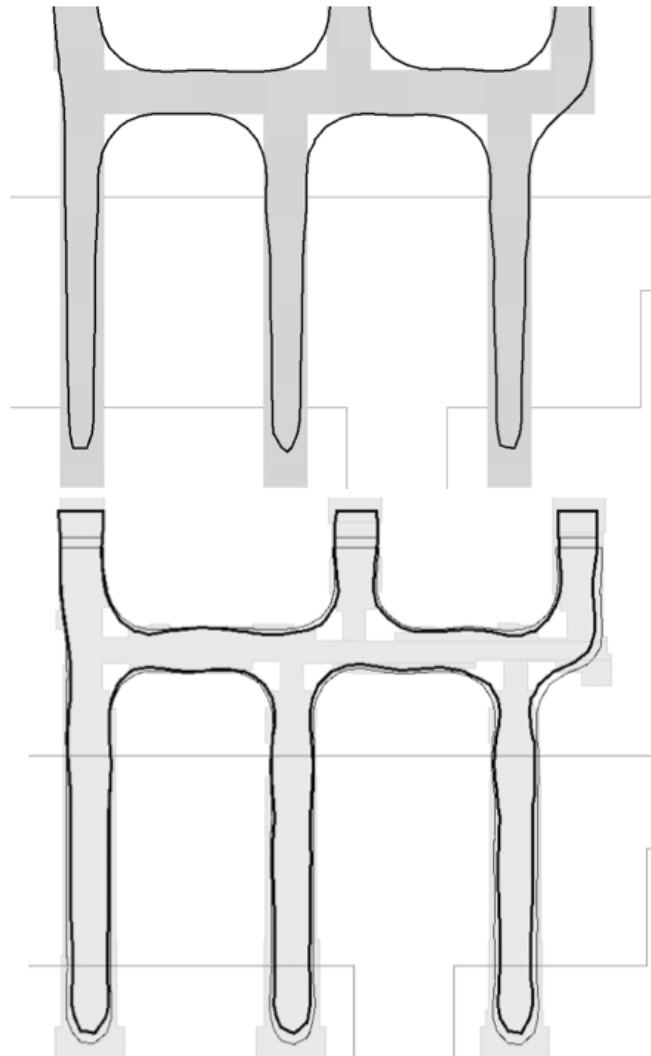
65 nm example Synopsys (SISPAD 06)



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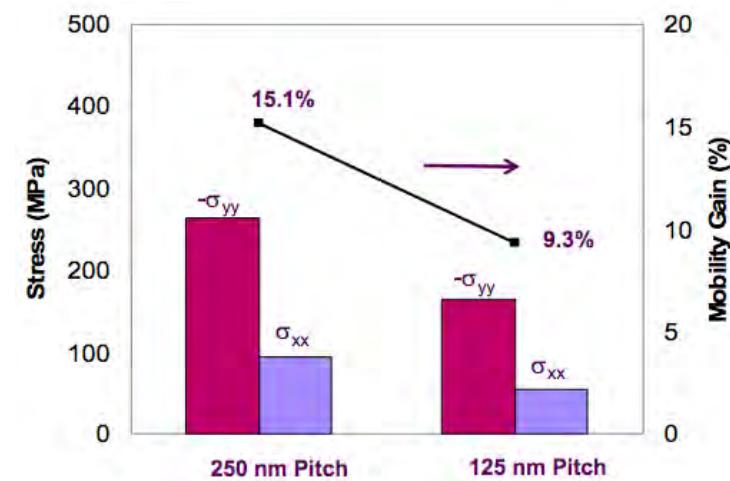
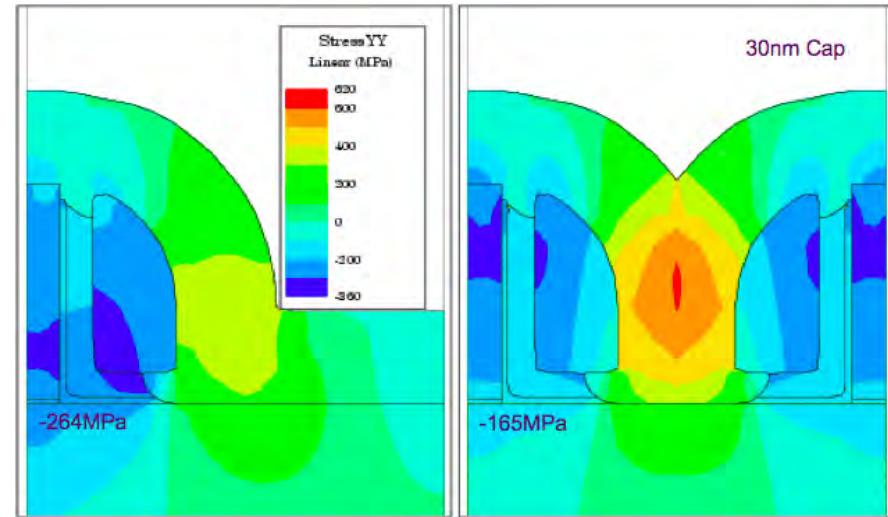
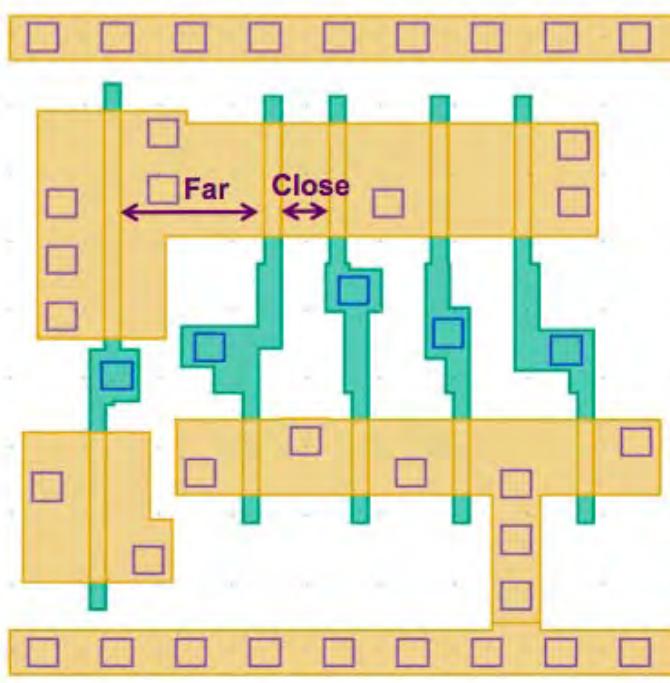
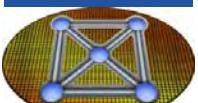


Strain induced variability



After W. Fichtner

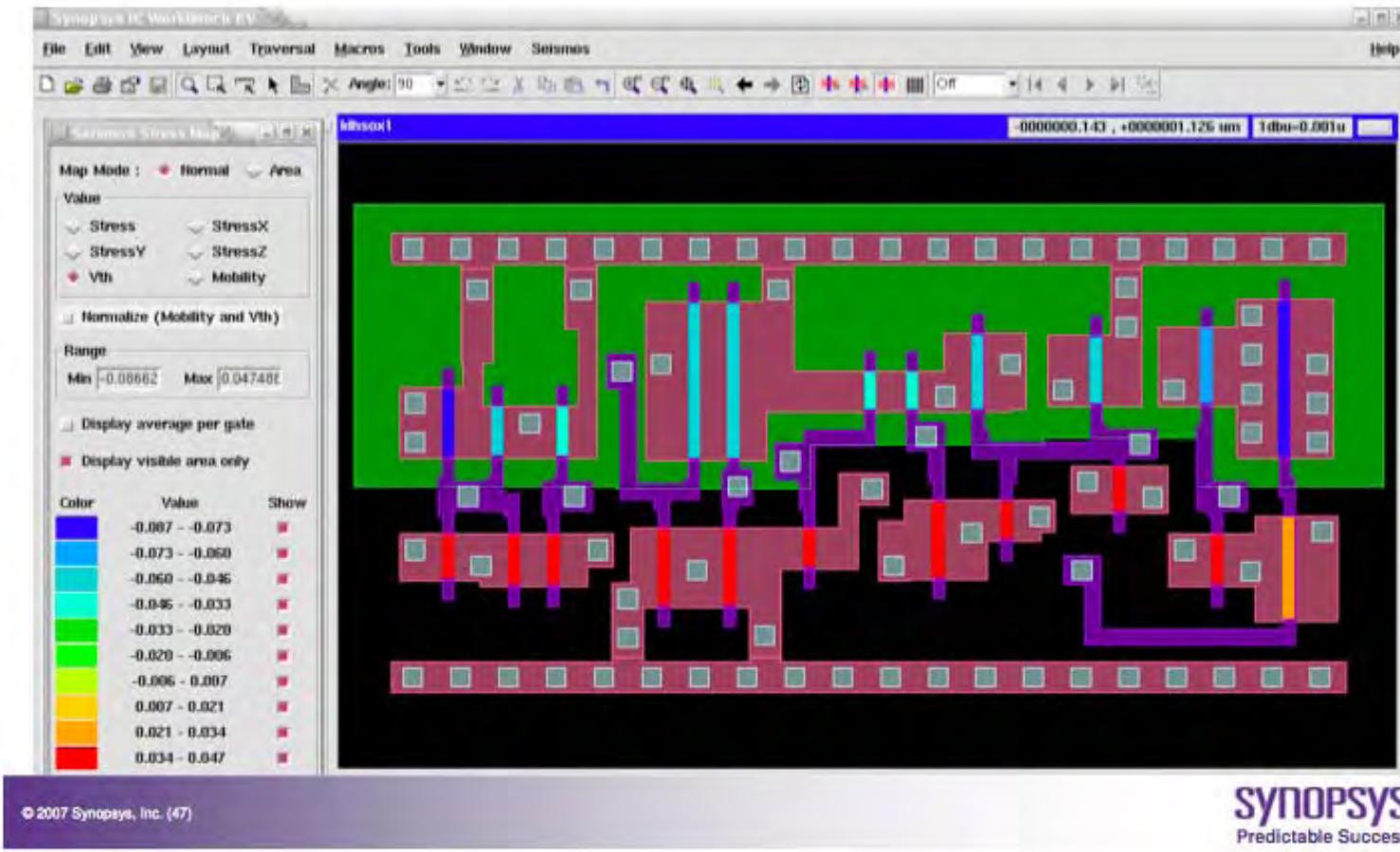
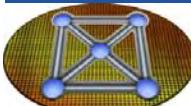
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ECAD tools can deal reasonably well With deterministic variability



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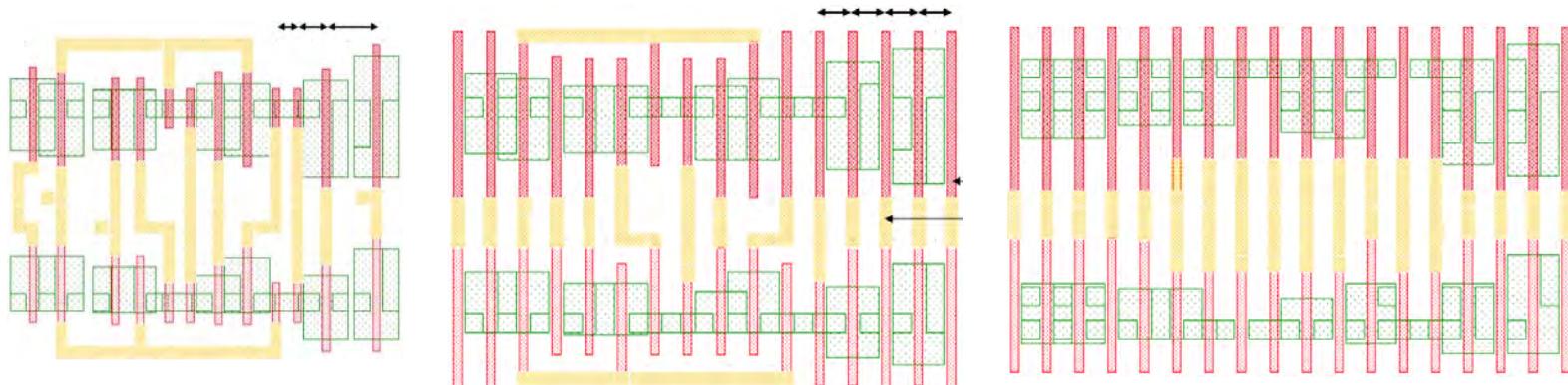


Restricted design rules and uniformity

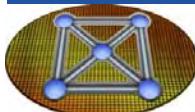
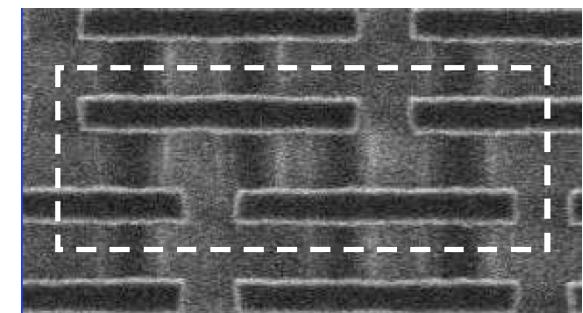


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After H. Onodera



- Irregular gate-poly pitch
- Horizontal poly wires
- Constant pitch with dummy poly insertions
- Dummy poly patterns
- Stretched gate-poly extensions
- Constant pitch with dummy poly insertions
- Stretched gate-poly extensions
- Single orientation





Summary

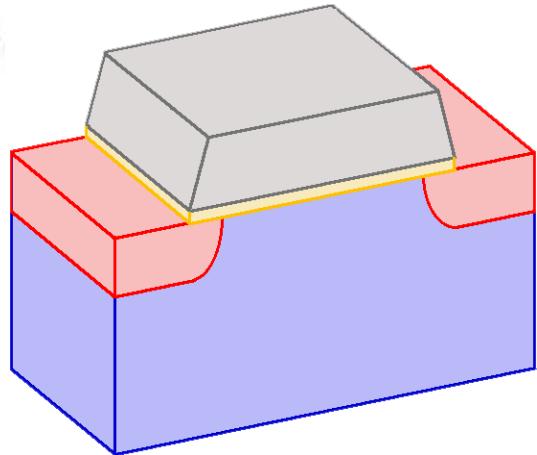
- Motivation
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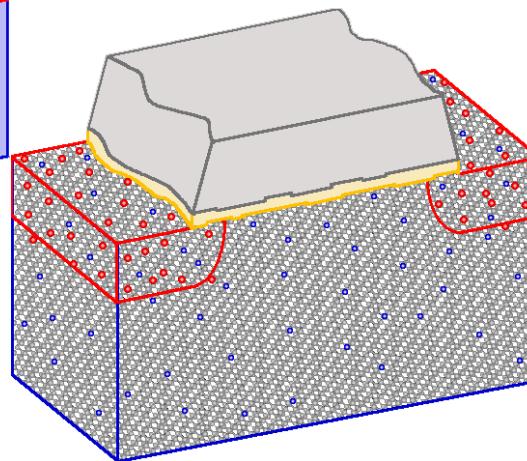
Statistical variability



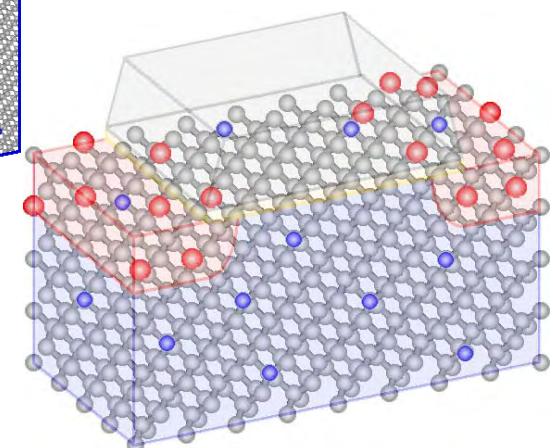
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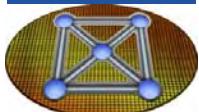
The simulation
Paradigm now



A 22 nm MOSFET
In production 2008



A 4.2 nm MOSFET
In production 2023

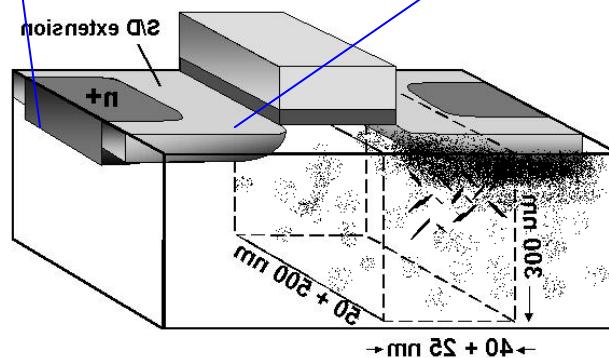
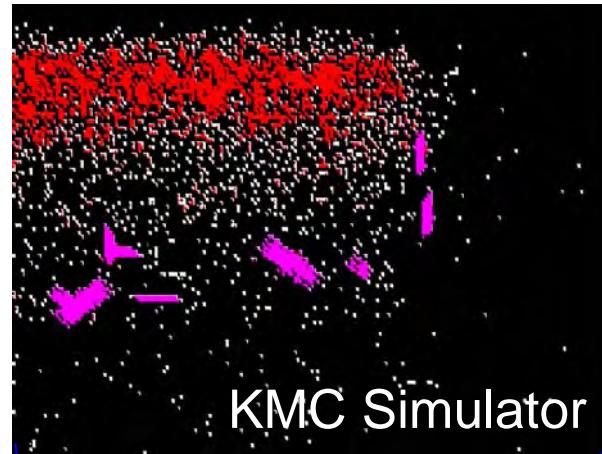


Random discrete dopants

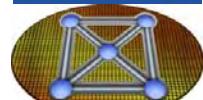
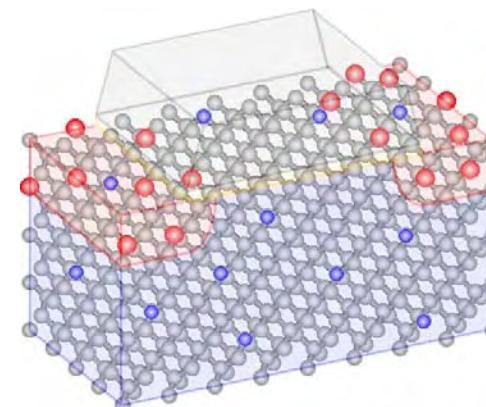
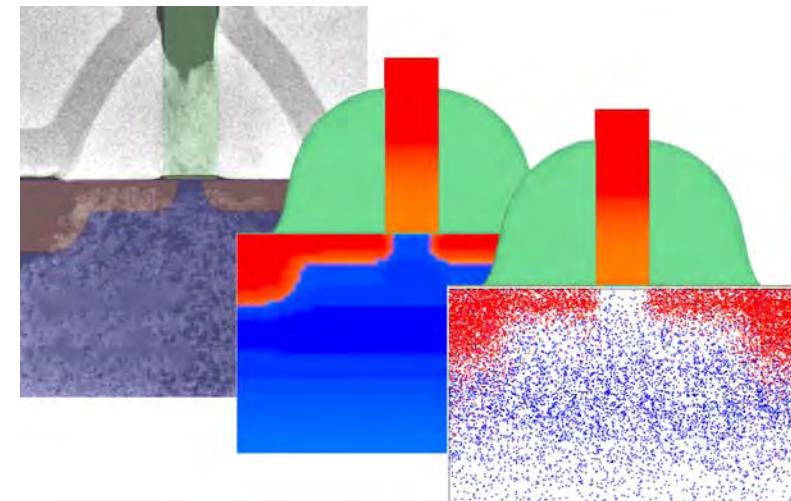


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Atomistic process simulation
M. Jaraiz



Continuous process simulation
Synopsys

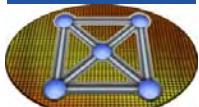
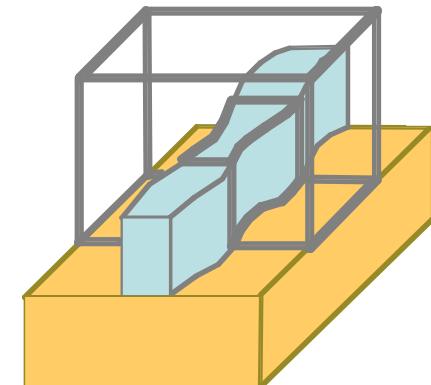
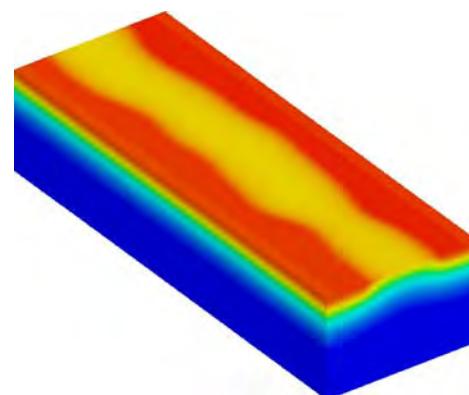
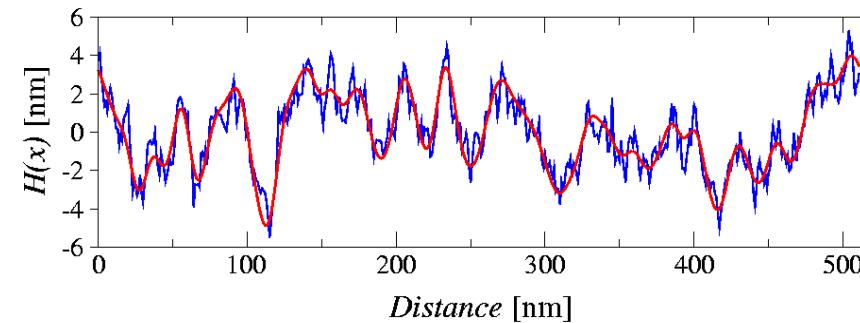
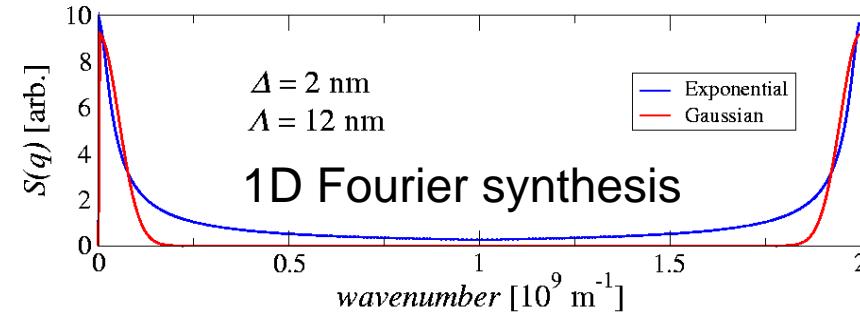
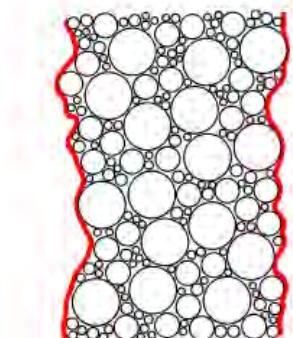
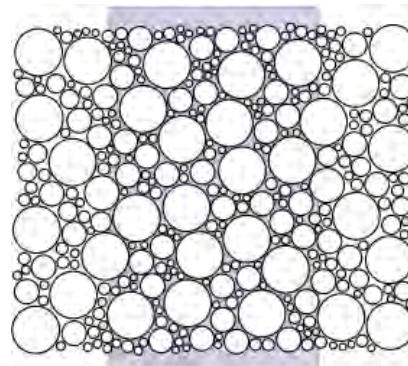
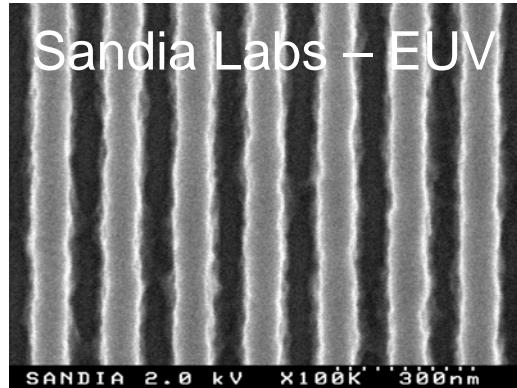


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Line edge roughness (LER)



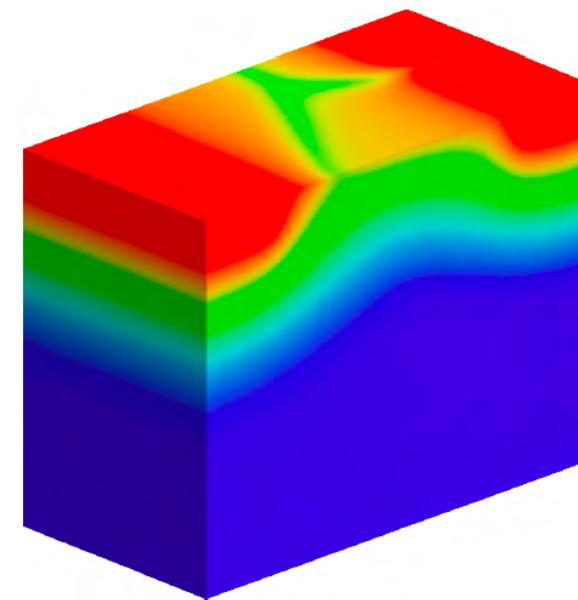
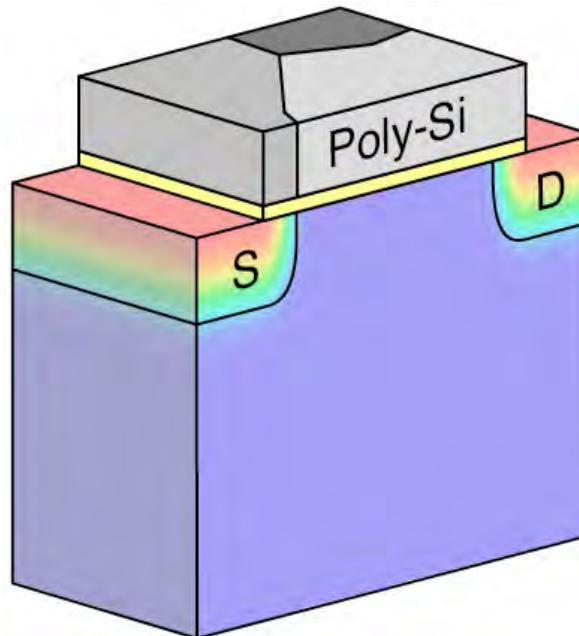
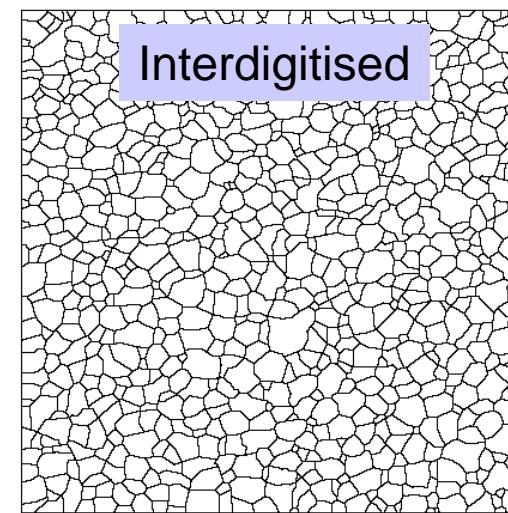
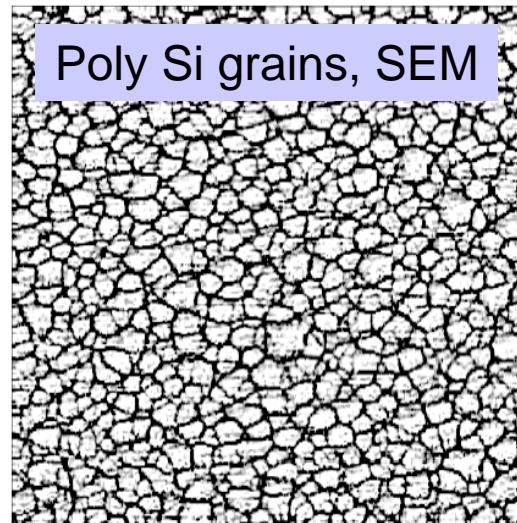
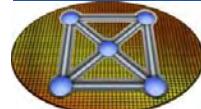
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Poly silicon grain boundaries



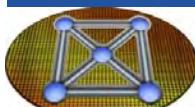
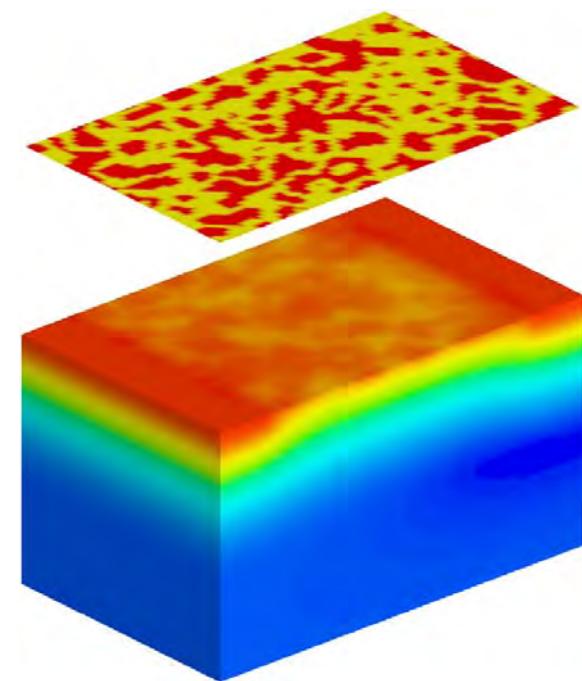
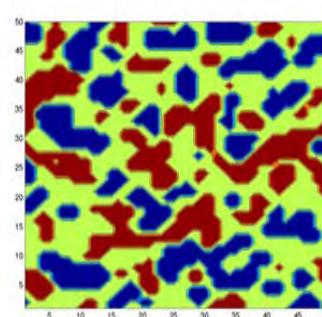
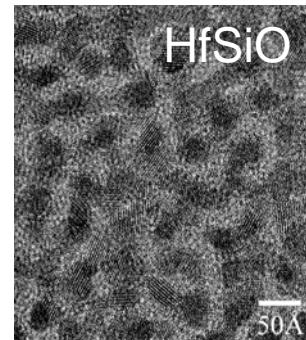
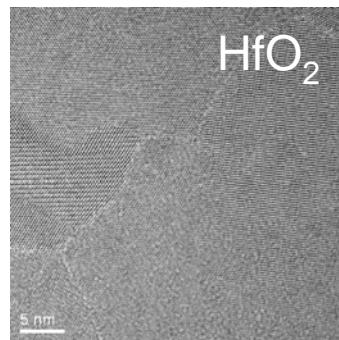
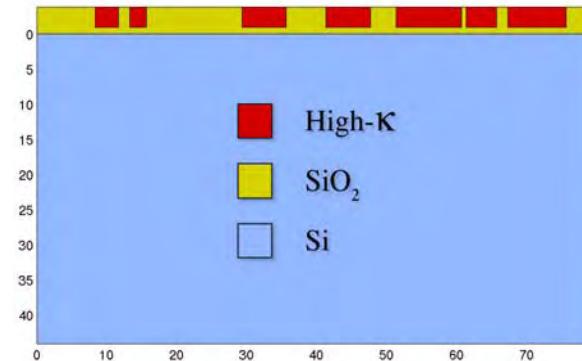
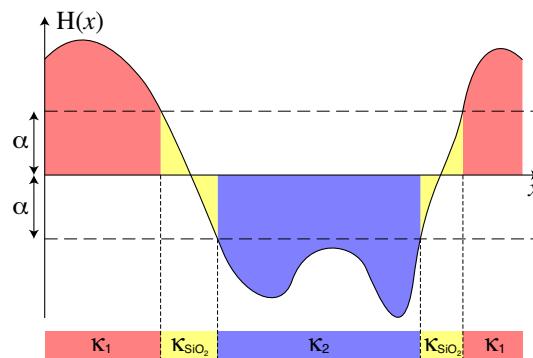
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High- κ morphology



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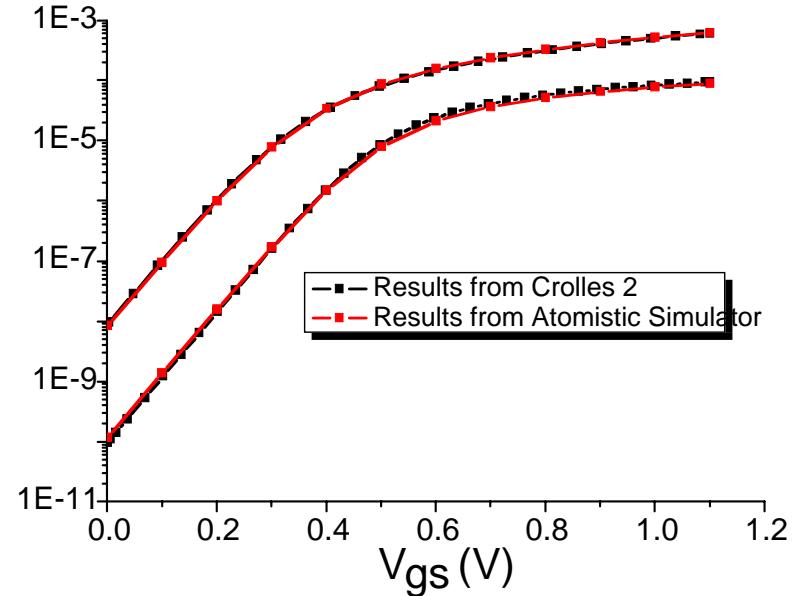
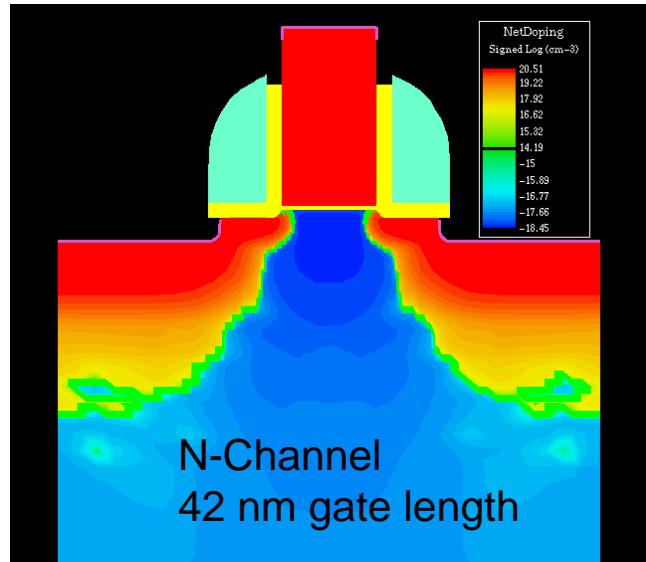
DEVICE
Modelling
Group

Measured and simulated variability

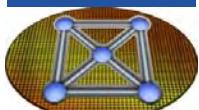
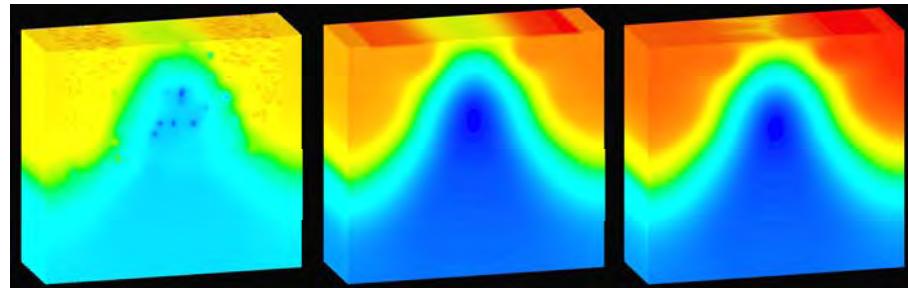
LP MOSFETs 45nm technology node



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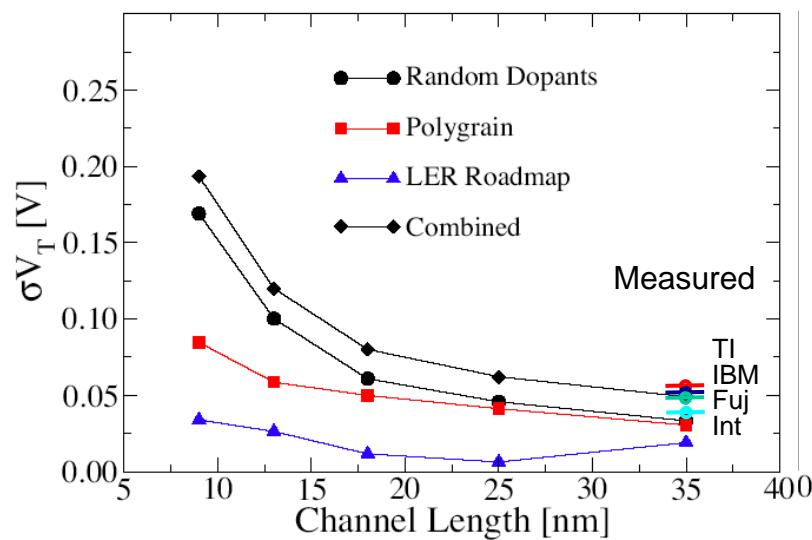
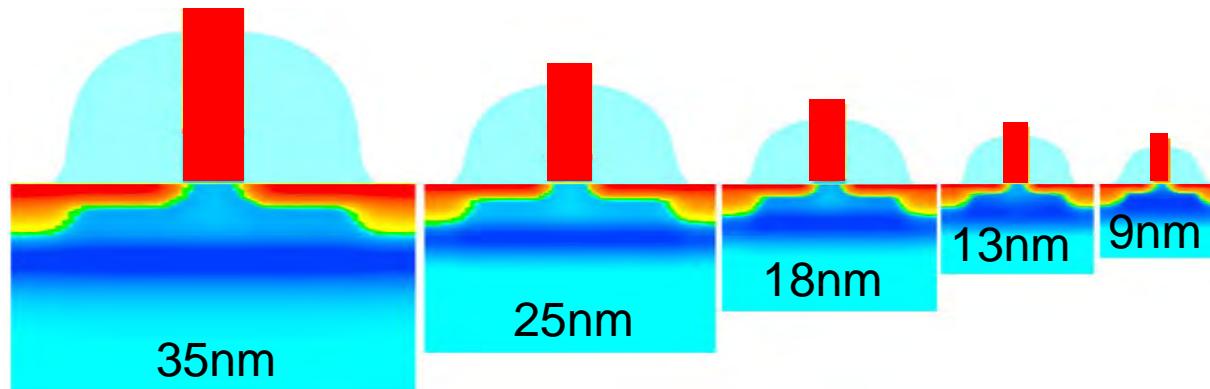
| | σV_T (50 mV) | σV_T (1.1 V) |
|------------|-------------------------|-------------------------|
| Experiment | 62 mV | 69 mV |
| Simulation | 62 mV | 67 mV |



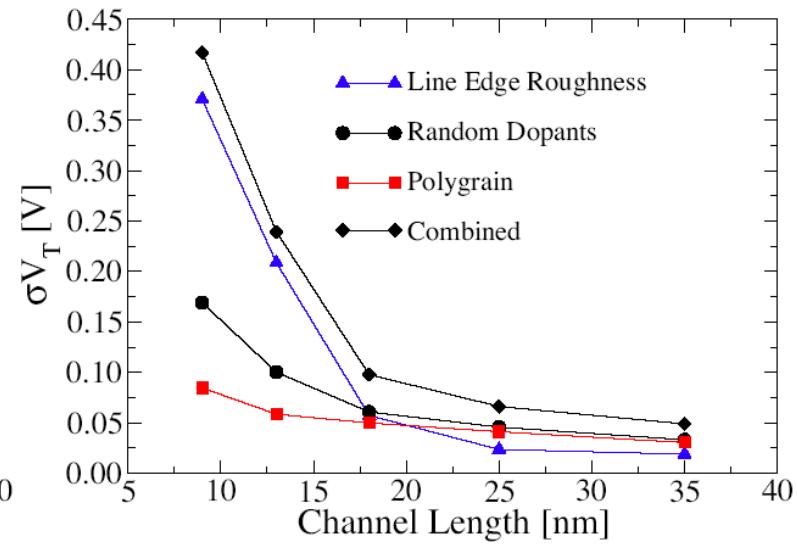
Combined variability in bulk MOSFETs



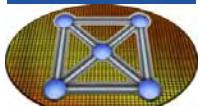
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LER follows ITRS



LER=4nm



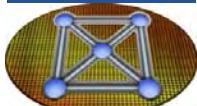
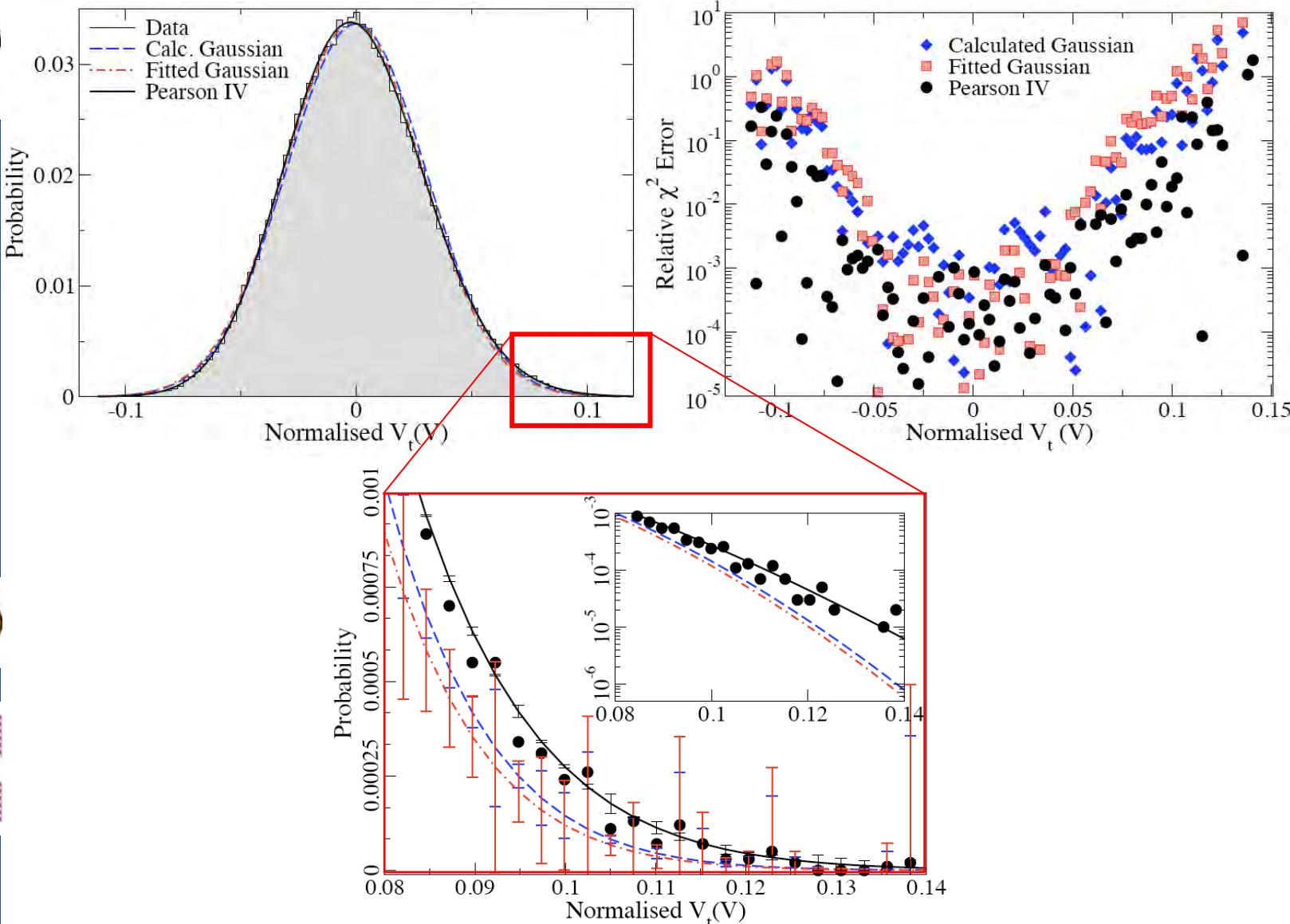
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The true shape of the distribution

Based on the simulation of 100000 transistors



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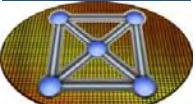


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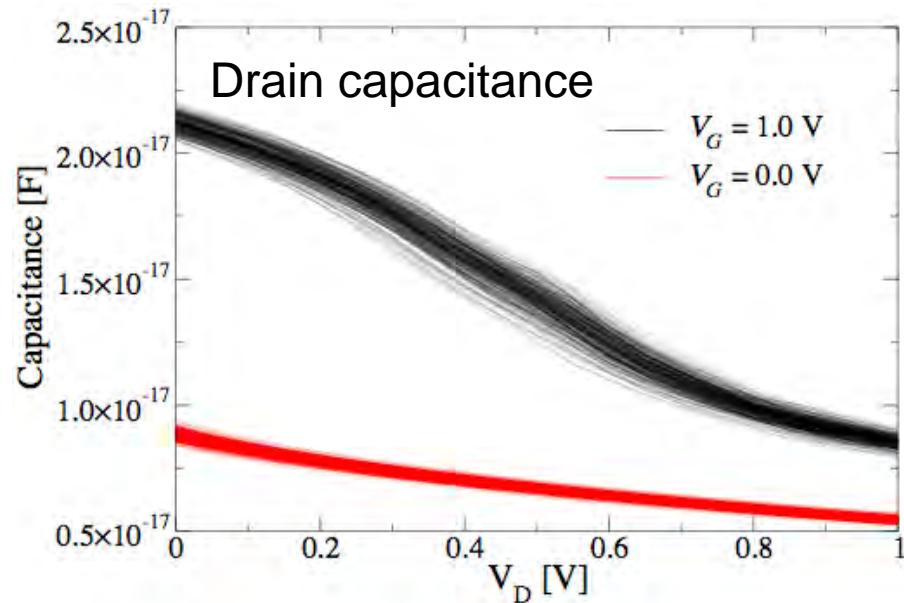
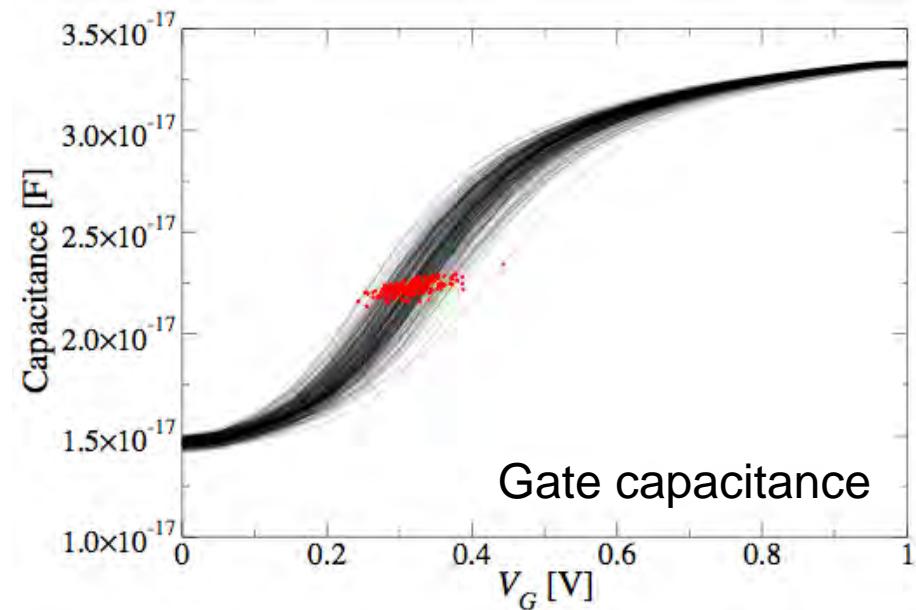
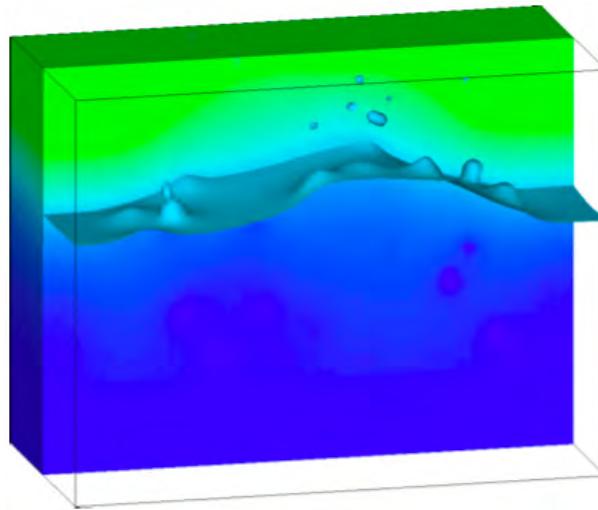
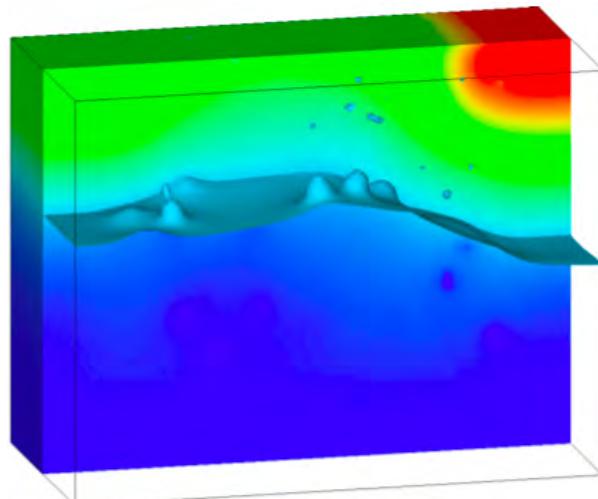
MOSFET capacitance variability



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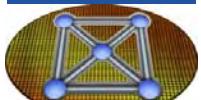
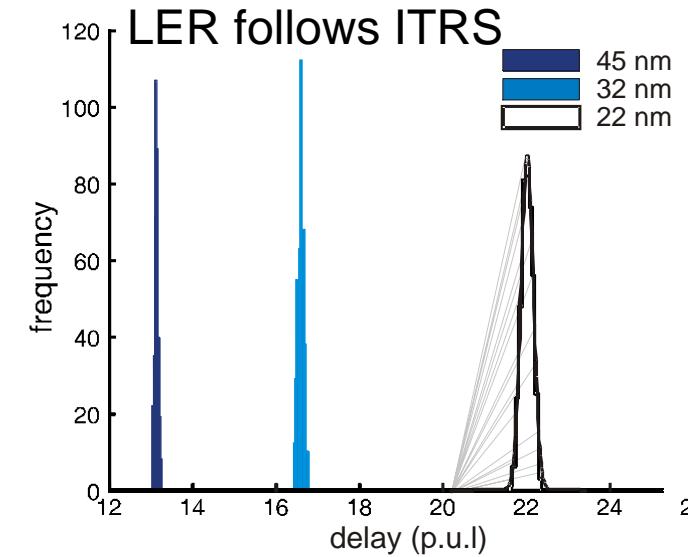
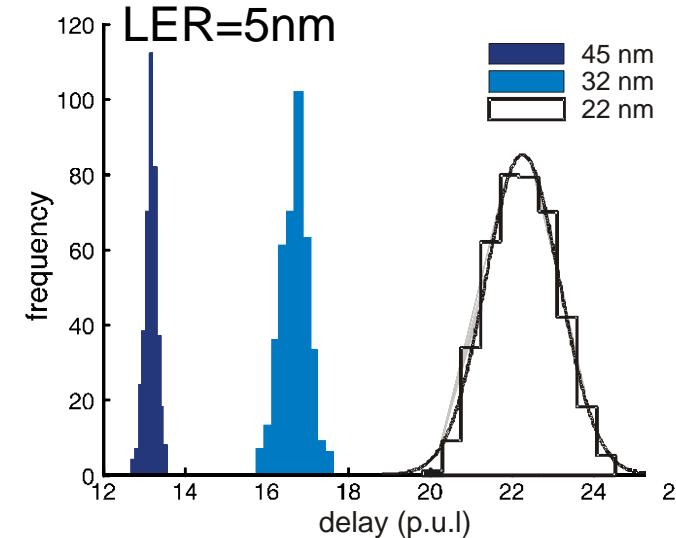
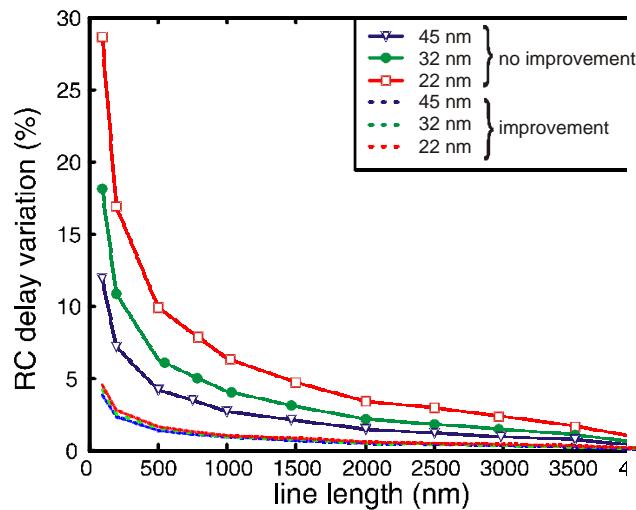
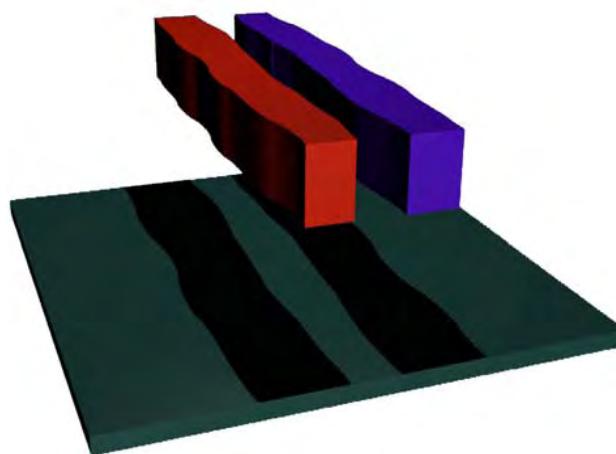


Interconnect variability

After: *T. D. Drysdale*



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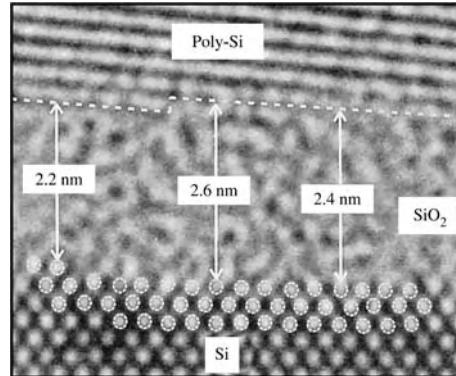


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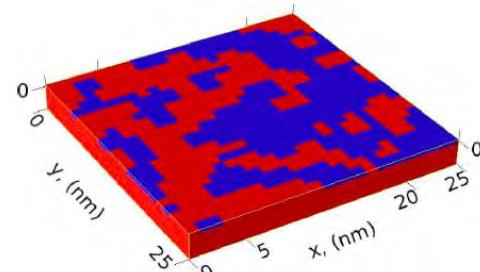
Gate tunnelling leakage variability



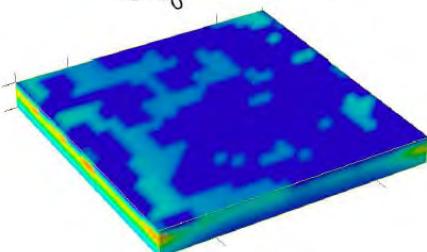
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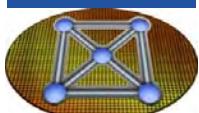
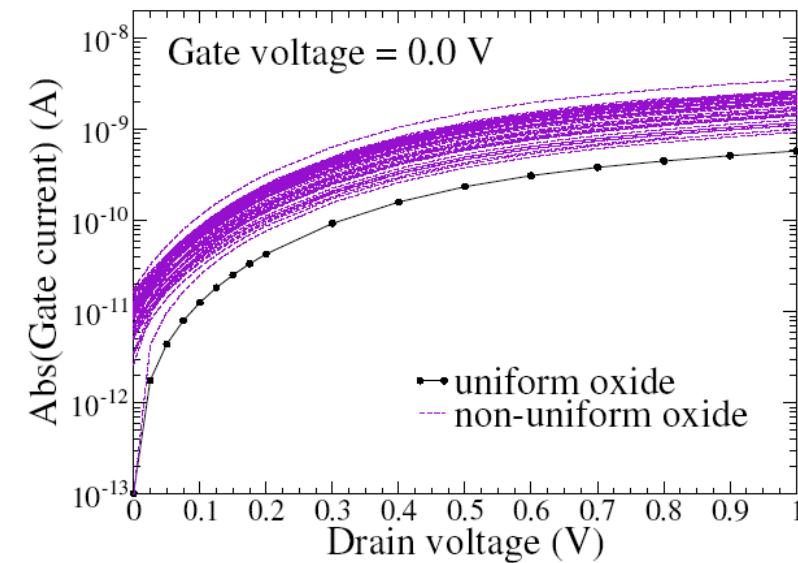
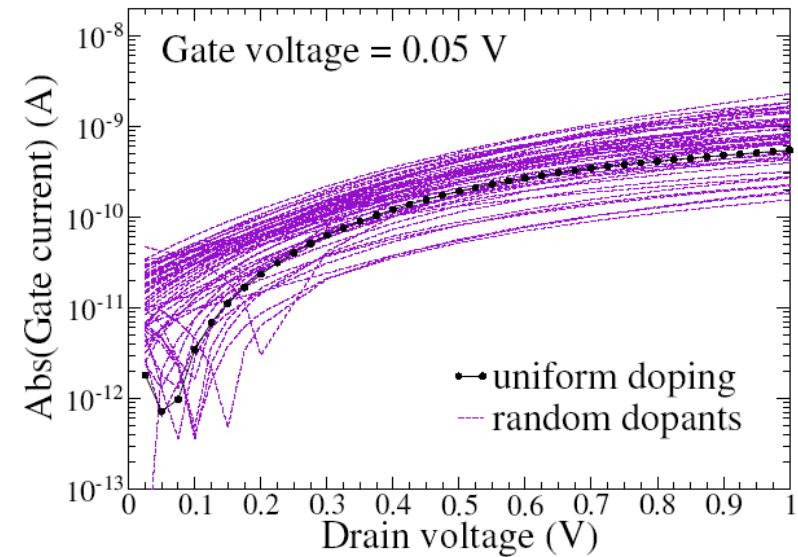
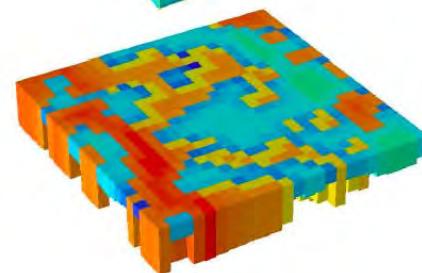
Interface pattern



Electron distribution



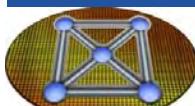
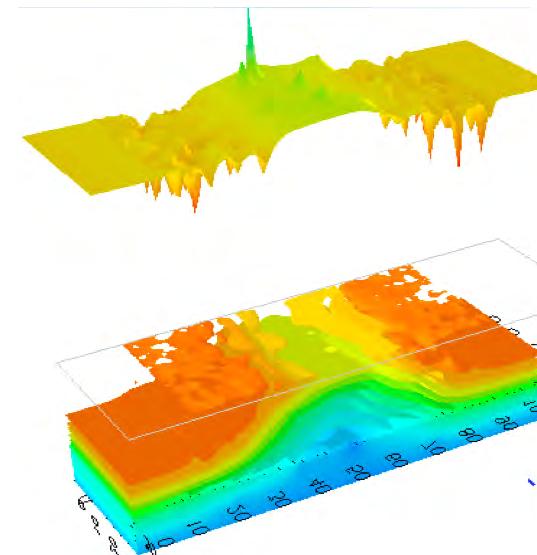
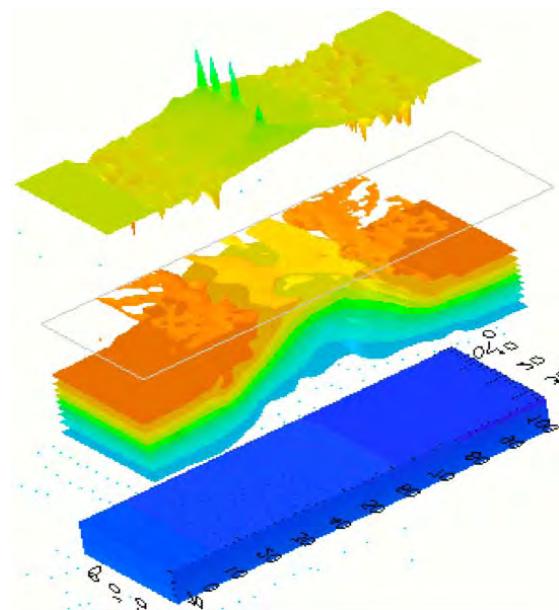
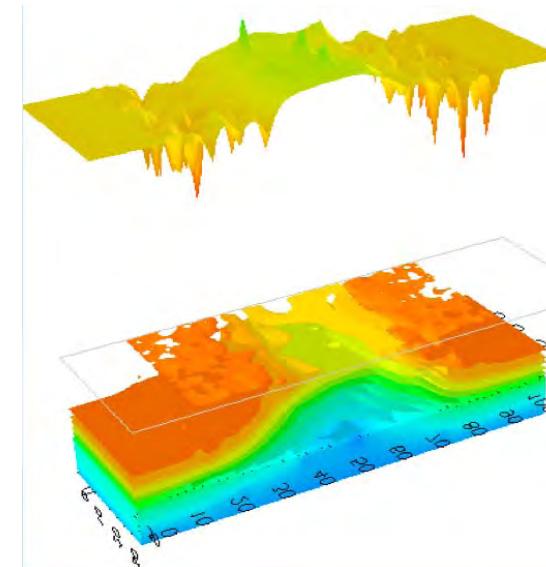
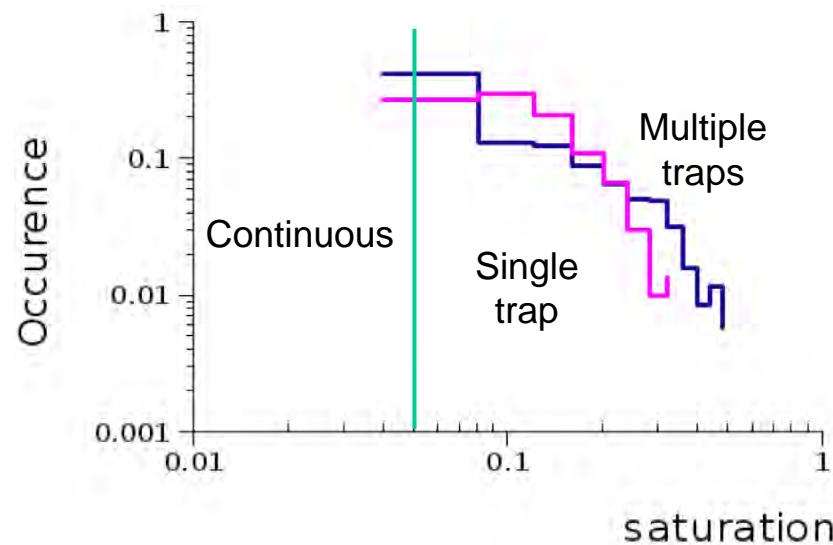
Current density



Statistical reliability



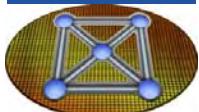
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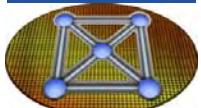




Summary

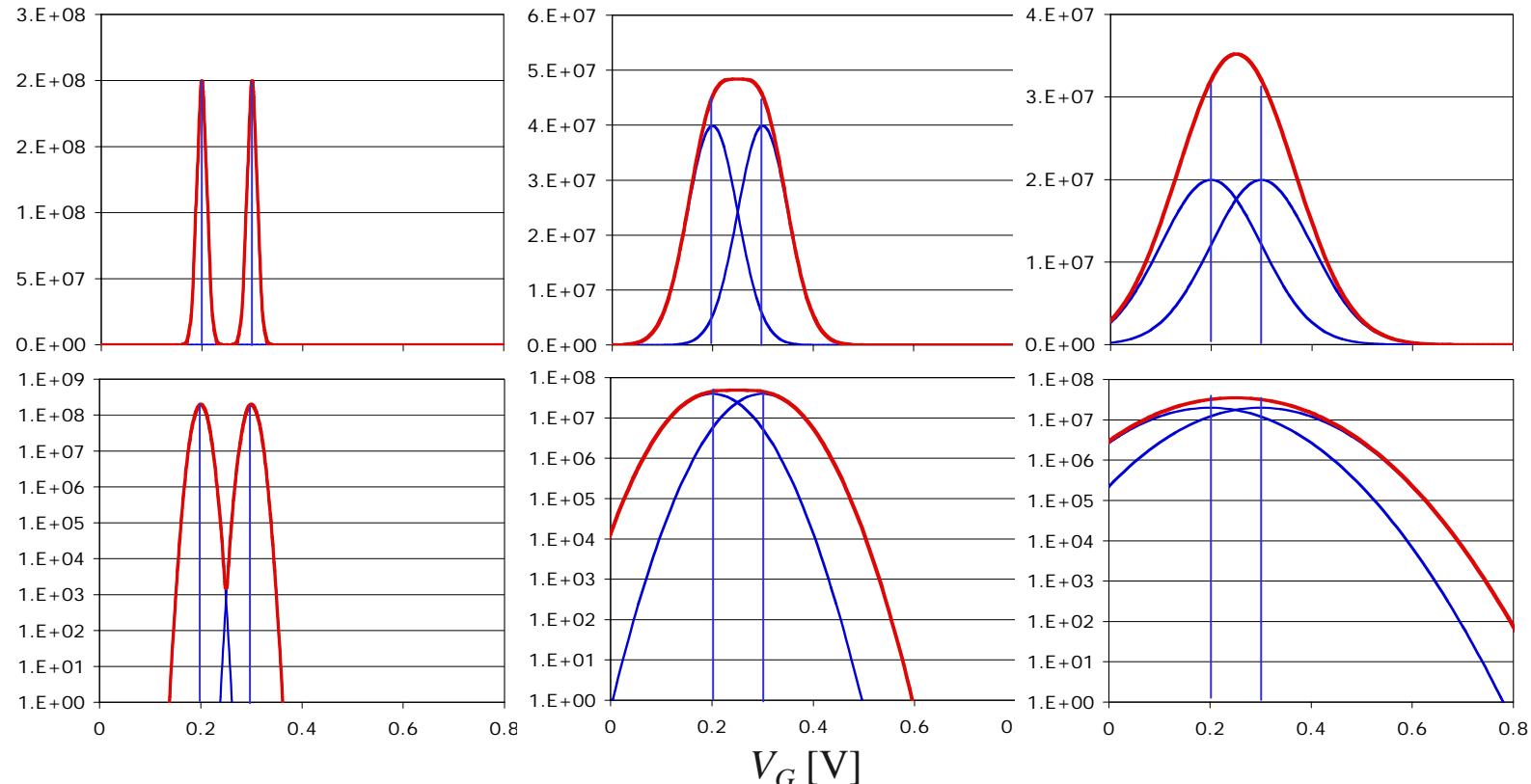
- Motivation
- Deterministic variability
- Statistical variability
- Impact on circuits**
- EU variability projects
- Conclusions





Deterministic vs. statistic variability

2 billion transistors: $V_{T1}=200\text{mV}$ $V_{T2}=300\text{mV}$



$$\sigma V_T = 10\text{mV}$$

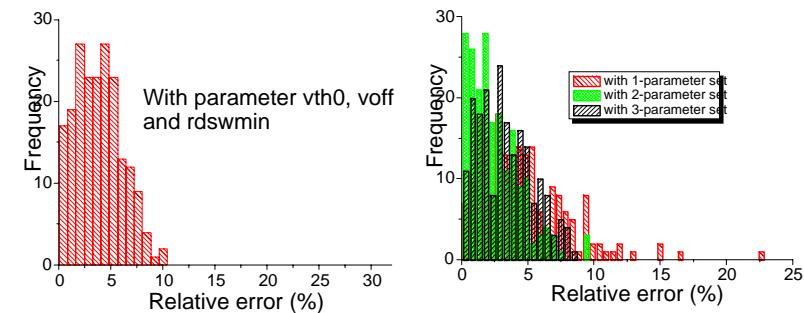
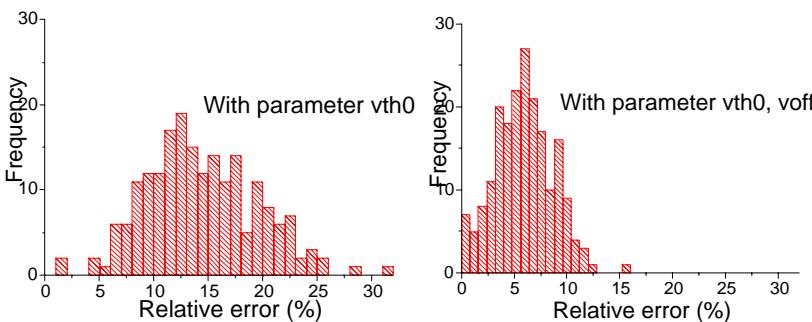
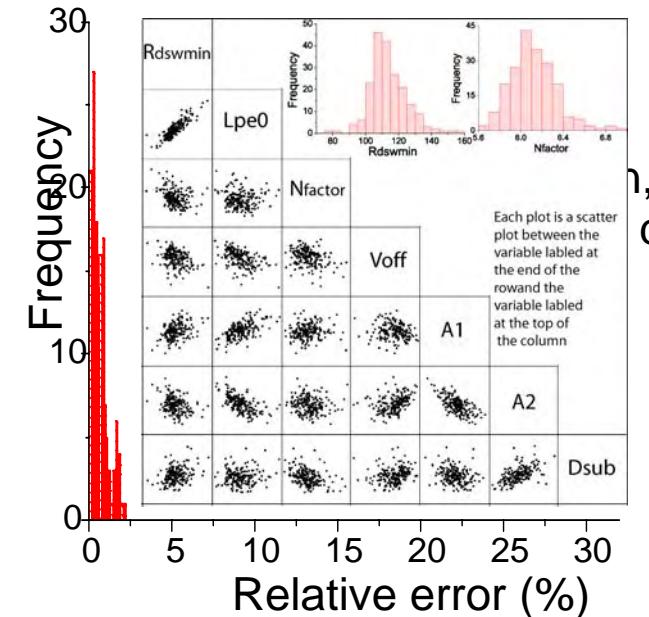
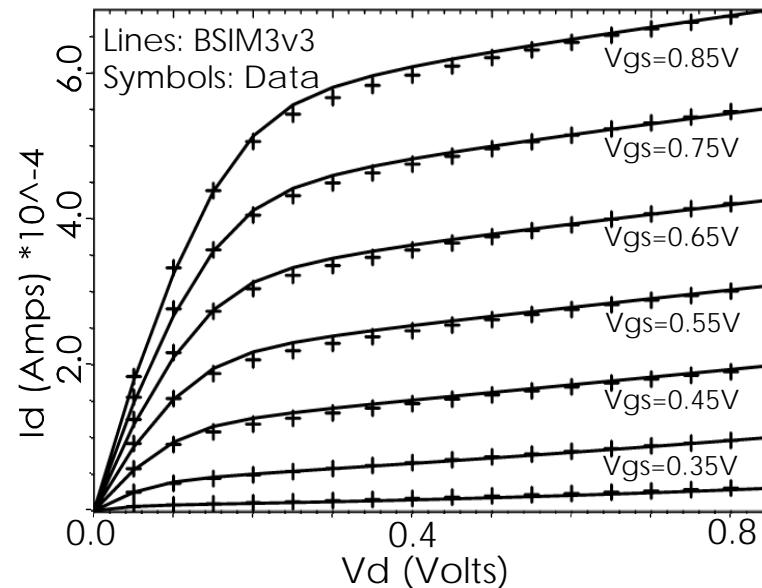
$$\sigma V_T = 50\text{mV}$$

$$\sigma V_T = 100\text{mV}$$

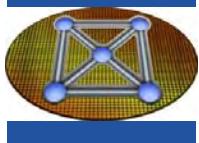
Compact model strategies



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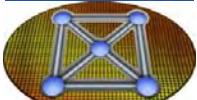
BSIM



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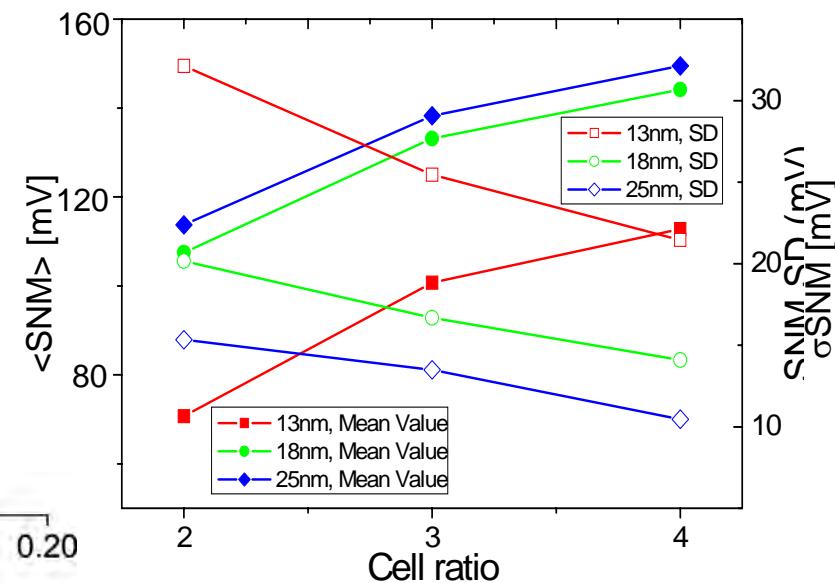
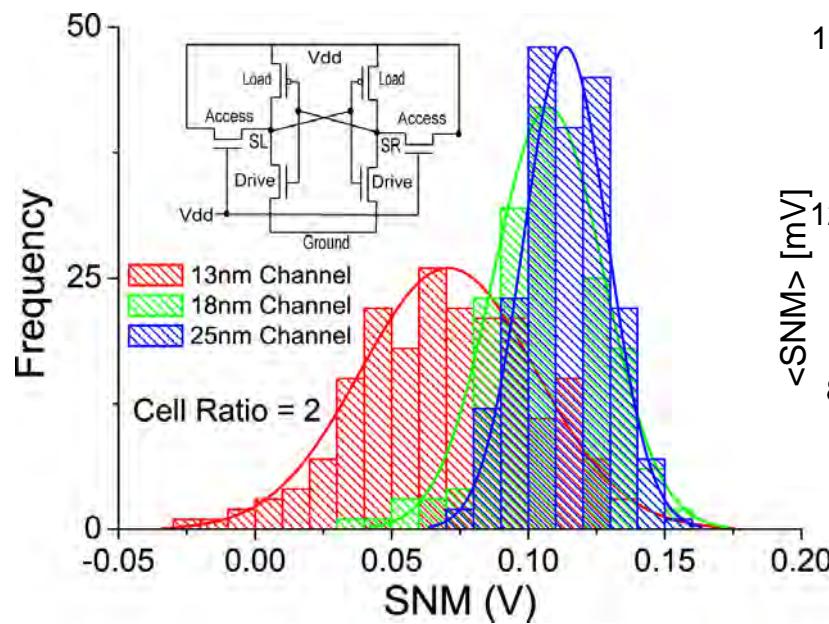
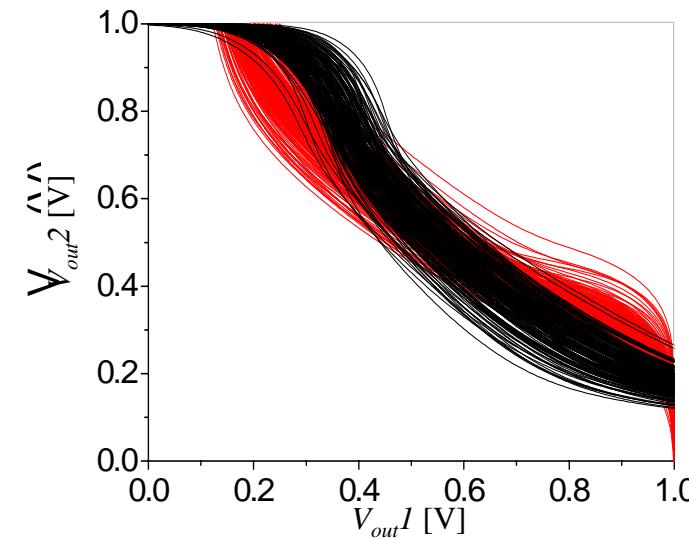
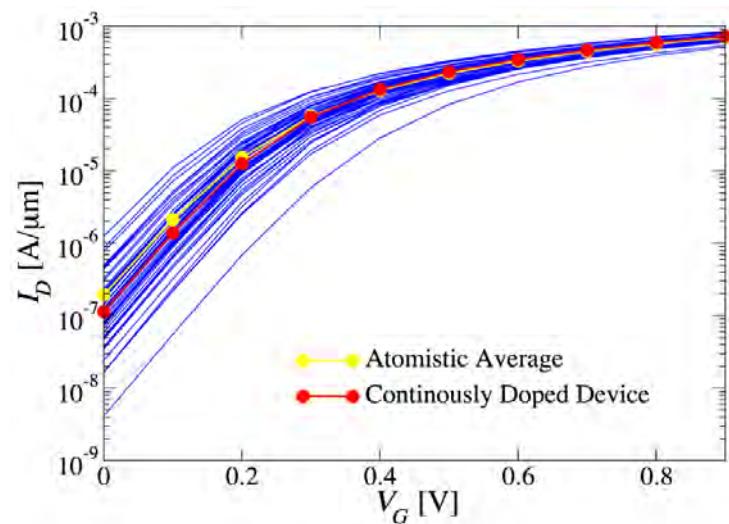


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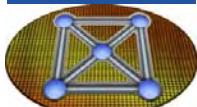
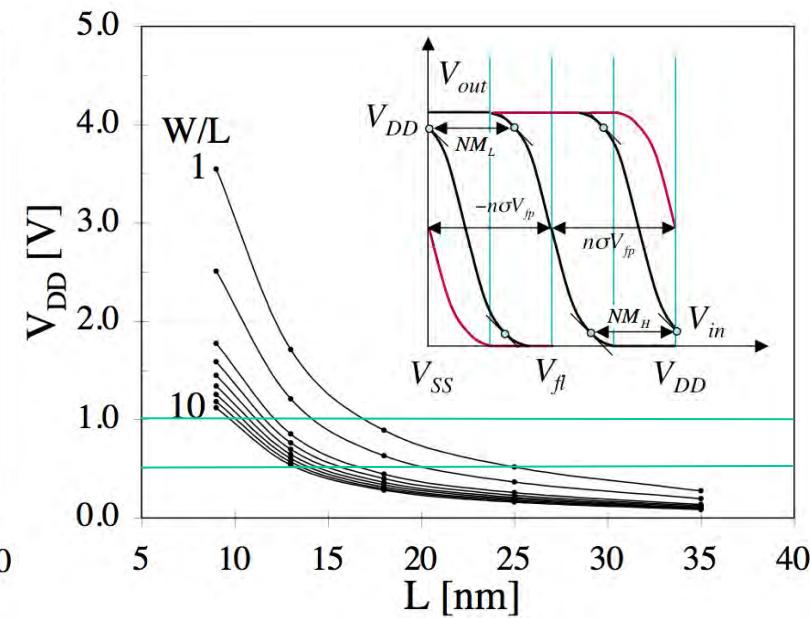
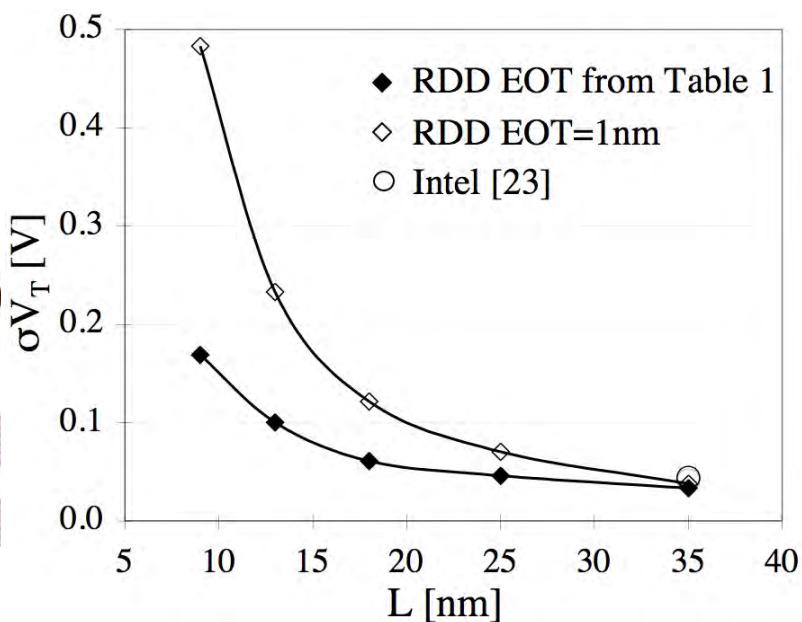
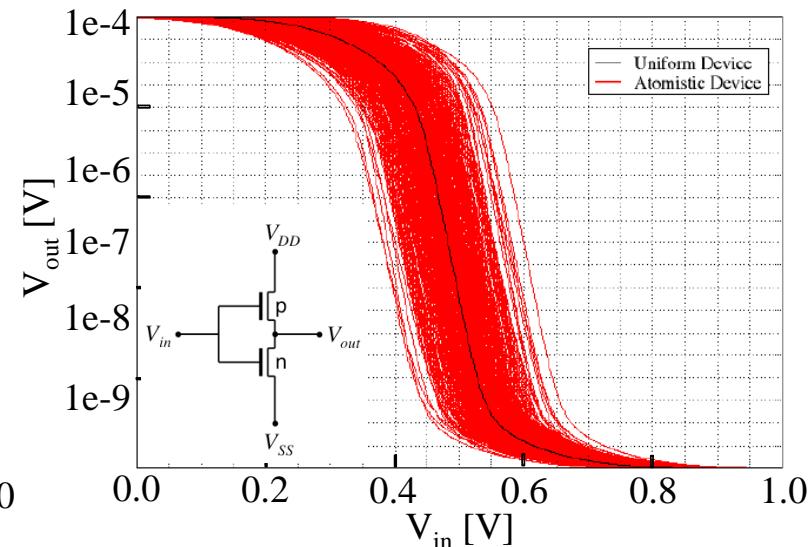
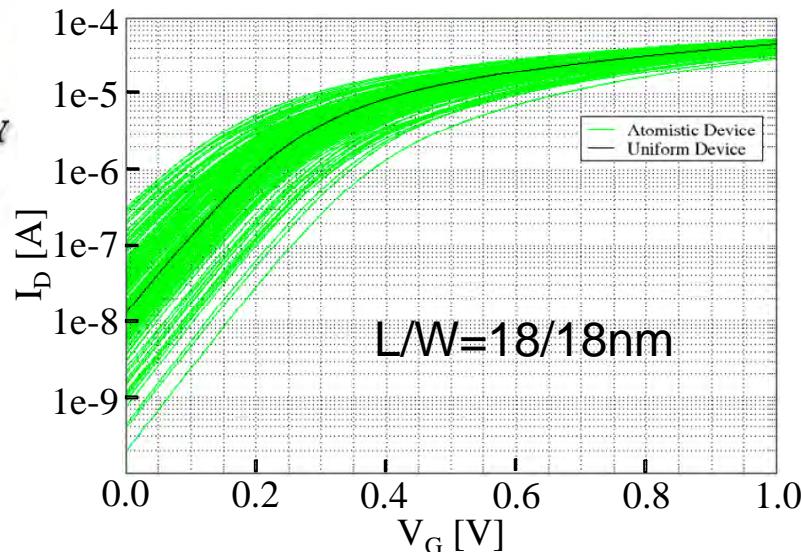
Impact of bulk MOSFET scaling of SRAM



Hard logic faults



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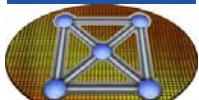
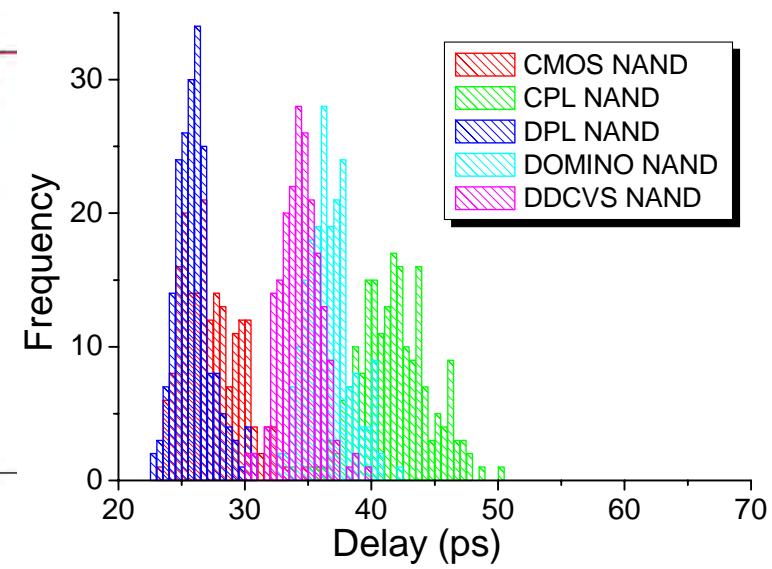
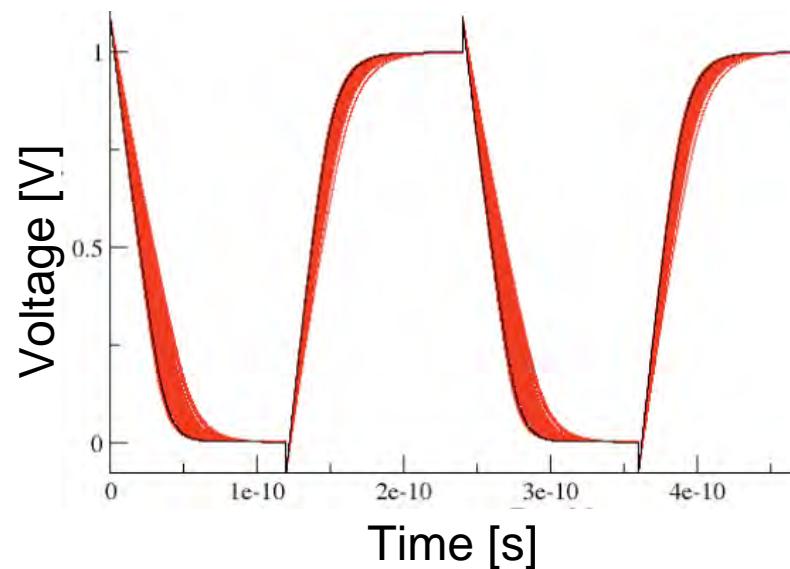
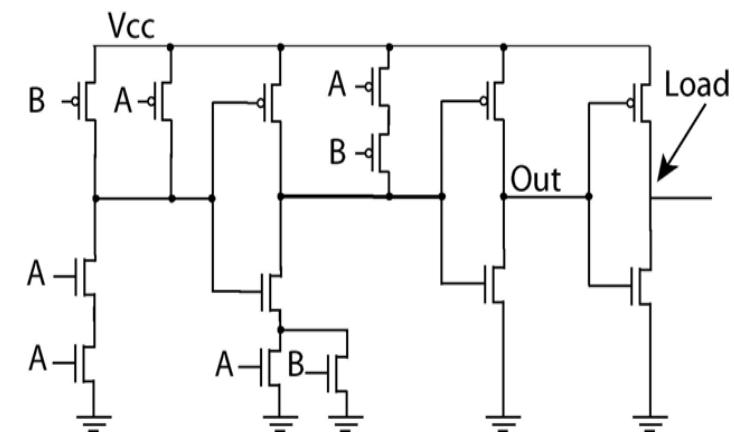
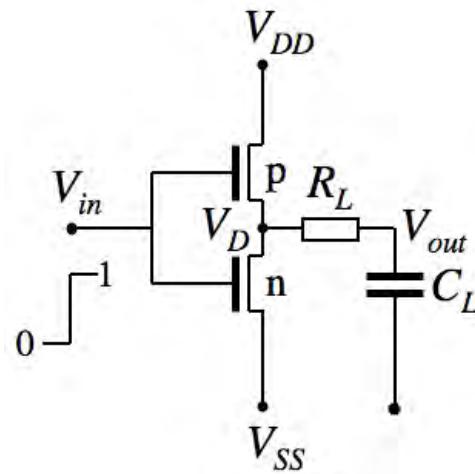


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Timing variability



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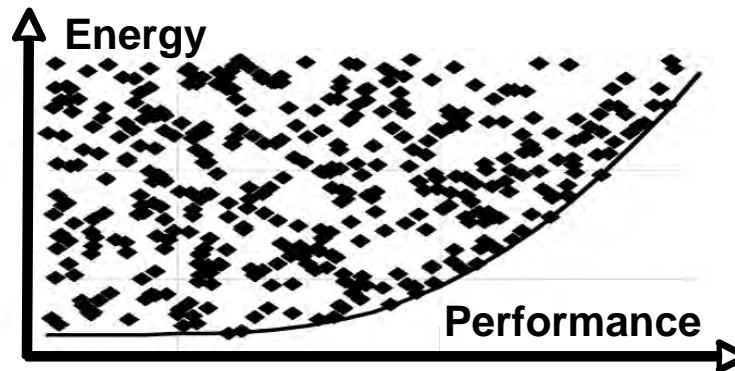


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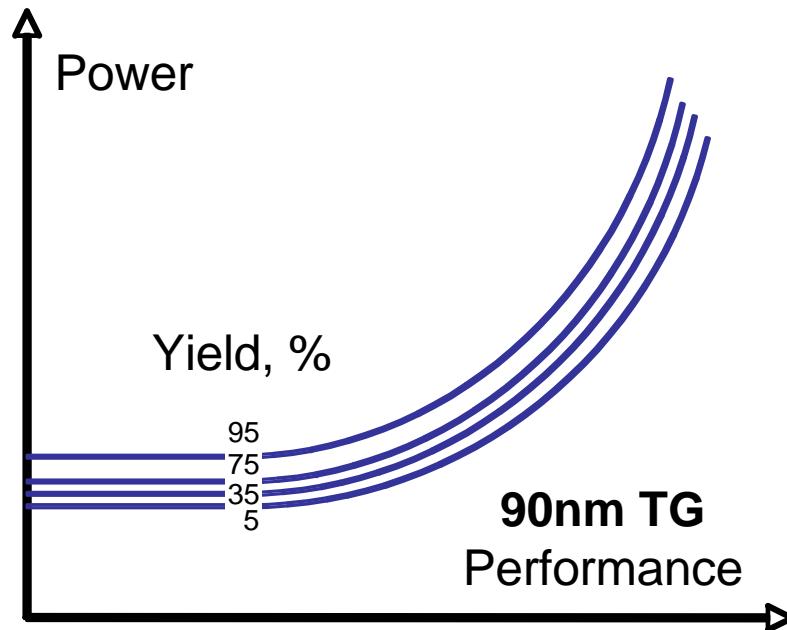
Performance/Power/Yield (PPY) trade-off



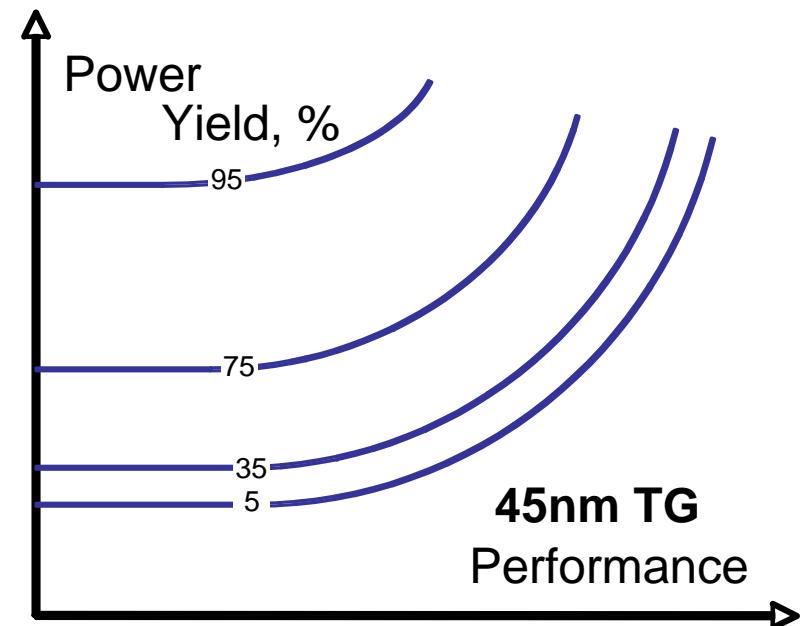
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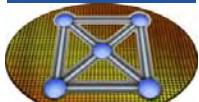
Pareto optimal curve
(M. Horowitz, IEDM05)



90nm TG
Performance



45nm TG
Performance

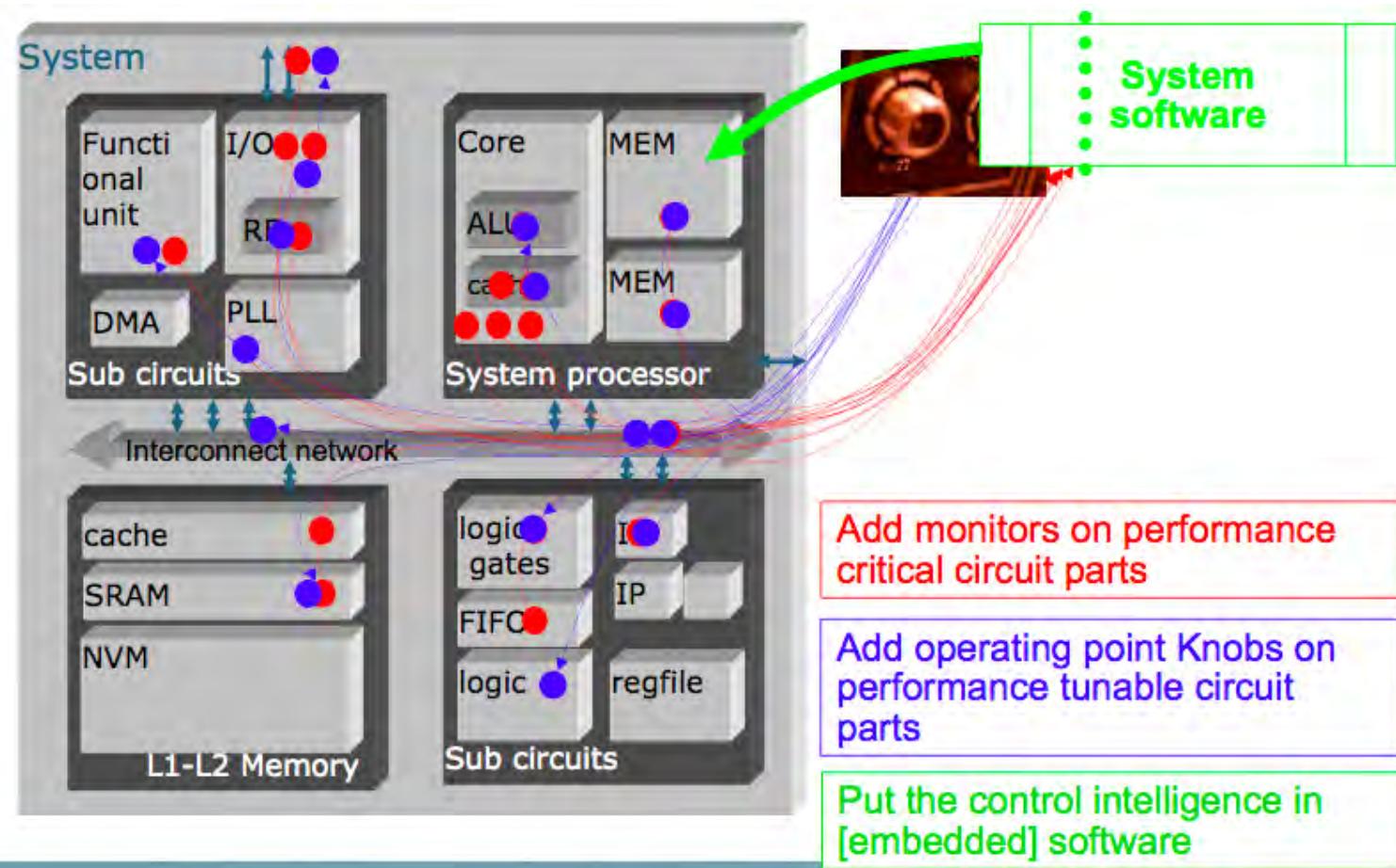
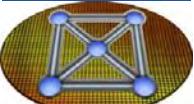


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The monitors and knobs approach



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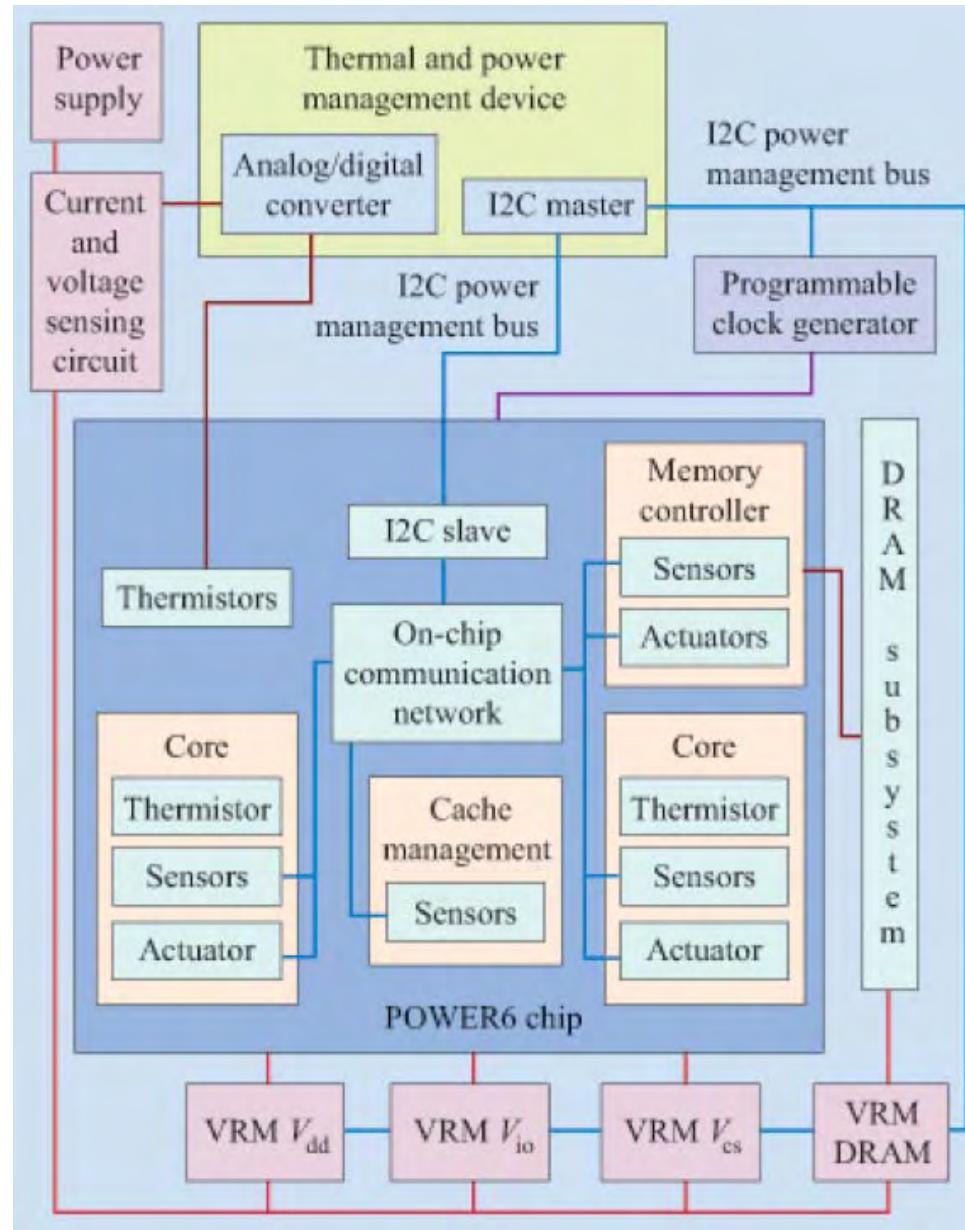
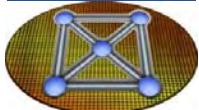


The “Technology Aware Design” of IMEC

The Power 6 processor of IBM



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Summary

- Motivation
- Deterministic variability
- Statistical variability
- Impact on circuits
- EU variability projects
- Conclusions





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Meeting the Design Challenges of Nano-CMOS Electronics - eScience Pilot Project

University Partners

Edinburgh University MMDGUE, NeSCE

Glasgow University DMGUG, MSTGUG, NeSCG

Manchester University APTGUM, eSNW

Southampton University ESDGUS

York University ISGUY

Industrial Partners

Synopsys, ARM, Wolfson Microelectronics,

Freescale, National Semiconductors, Fujitsu, NMI

Resources

£3.3M EPSRC, £4.1M FEC, £5.3M IC

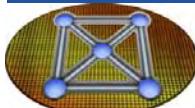
11 PDRAs 7 Science4 e-Sci 7 PhD



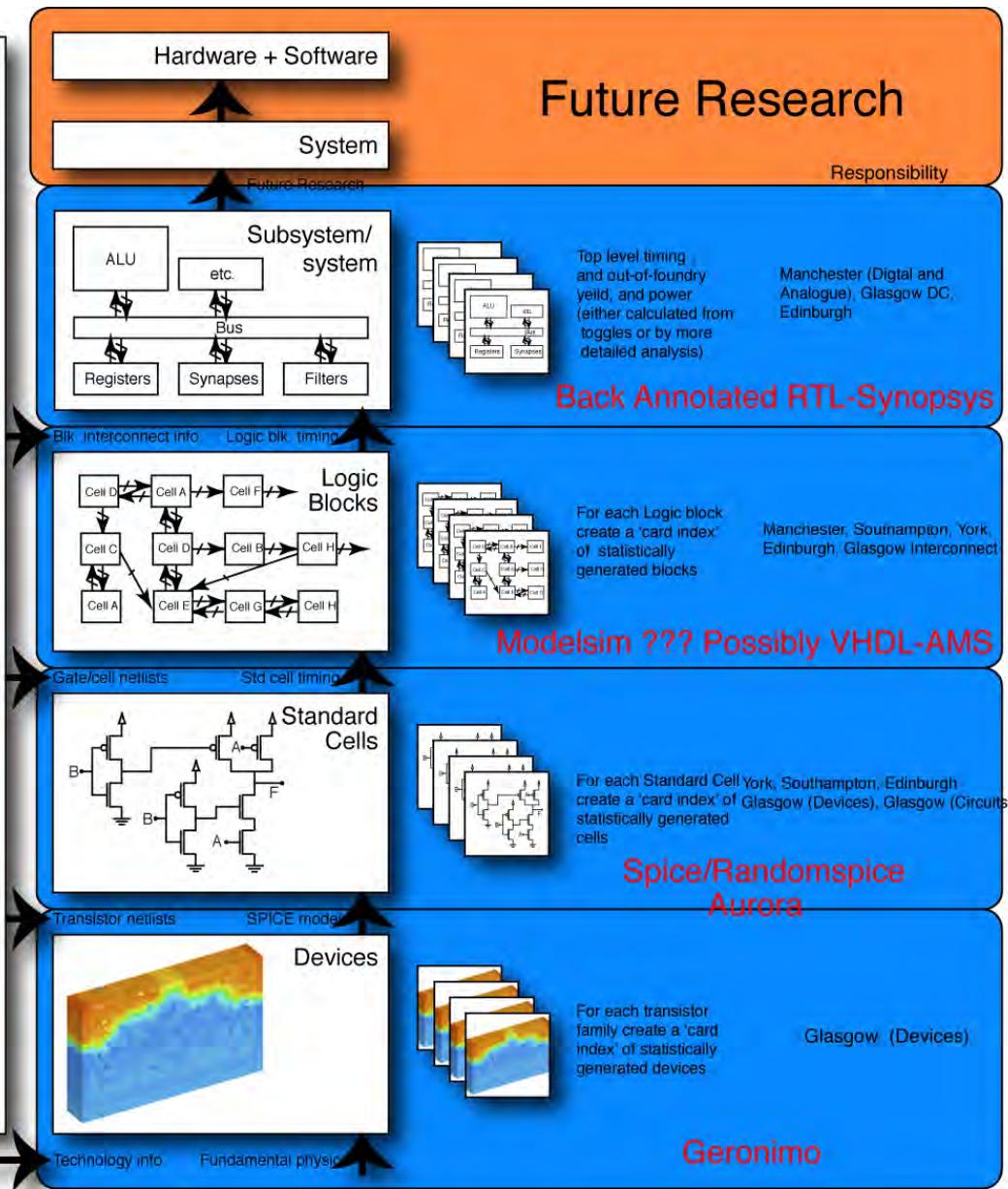
Grid based statistical simulation



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Standard toolflow for some practical design, (90nm, 45nm?) complete, down past place & route,
so that we have complete cell, device, interconnect information.





CMOS variability research in Europe

ESSDERC/ESSIRC 2008 Workshop

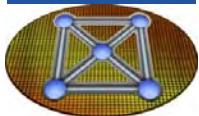
NANOSIL: Silicon-based nanostructures and nanodevices for long term nanoelectronics applications (EU FP7), R. Clerc

PULLNANO: Pulling the limits of the nano CMOS Electronics (EU FP6), H. Maes

REALITY: Reliable and variability tolerant system on a chip design in More-Moore technologies (EU FP7)
B. Dierickx, IMEC

NanoCMOS: Meeting the design challenges of the nano-CMOS electronics (UK EPSRC), A. Asenov, GU

NanoMat: Meeting the material challenges of the nano CMOS electronics (UK EPSRC), A. Shluger, UCL





Summary

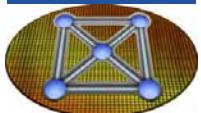
- Motivation
- Deterministic variability
- Statistical variability
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Conclusions

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- The statistical variability will be increasing in the next technology nodes.
 - The statistical variability can not be reduced by fine tuning the technology, OPC and regular designs.
 - The statistical variability demands statistical approach to design and will force fundamental design changes.
 - The fabless and the chipless companies have to learn more about technology and devices.





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Acknowledgements to all members of the Device Modelling Group



Asen Asenov
Prof



John Barker
Prof



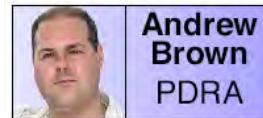
Scott Roy
Senior Lecturer



Jeremy Watling
EPSRC
ARF



Karol Kalna
EPSRC
ARF



Andrew Brown
PDRA



Binjie Cheng
PDRA



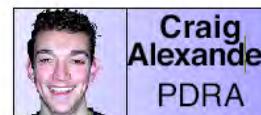
Campbell Millar
PDRA



Antonio Martinez
PDRA



Giulio Ferrari
PDRA



Craig Alexander
PDRA



Gareth Roy
PDRA



Khairulmizam Samsudin
PhD



Craig Riddet
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Stanislav Markov
PhD



Sonia Paluchowski
EngD



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PhD

Department of Electronics and Electrical Engineering
University of Glasgow

