Statistical Device Variability and its Impact on Design

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Summary

- Motivation
- Deterministic variability
- Statistical variability
- Impact on circuits
- EU variability projects
- Conclusions
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The variability is becoming a major headache

G. Declerck, Keynote talk, VLSI Technol. Symp. 2005
The local stochastic variability becomes a major source of concern.

<table>
<thead>
<tr>
<th>Process</th>
<th>Environment</th>
<th>Temporal</th>
</tr>
</thead>
<tbody>
<tr>
<td>Global</td>
<td></td>
<td></td>
</tr>
<tr>
<td>&lt;Lₐ&gt; and &lt;W&gt;</td>
<td>T environment range</td>
<td>&lt;NBTI&gt;</td>
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<tr>
<td>&lt;layer thicknesses&gt;</td>
<td>V&lt;sub&gt;d&lt;/sub&gt; range</td>
<td>Hot electron shifts</td>
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<td>&lt;doping&gt;</td>
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<tr>
<td>&lt;V&lt;sub&gt;body&lt;/sub&gt;</td>
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<td>Global Deterministic</td>
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<td>OPC</td>
<td>Self-heating IR drops</td>
<td>Distribution of NBTI</td>
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<td>Phase shift</td>
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<td>Voltage noise</td>
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<td>Layout mediated strain</td>
<td></td>
<td>SOI V&lt;sub&gt;body&lt;/sub&gt; history</td>
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<tr>
<td>Well proximity</td>
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<td>Oxide breakdown history</td>
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<td>Local Stochastic</td>
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<td>Random dopants</td>
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<td>Line Edge Roughness</td>
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<td>Poly Si granularity</td>
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<td>Interface roughness</td>
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<td>High-k morphology</td>
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<td>Across-chip</td>
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<td>Line width due to pattern</td>
<td>Thermal hot spots due to</td>
<td>Computational load</td>
</tr>
<tr>
<td>density effects</td>
<td>non-uniform power dissipation</td>
<td>dependent hot spots</td>
</tr>
</tbody>
</table>

After D. J. Frank, IBM
Summary

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OPC and strain related variability
65 nm example Synopsys (SISPAD 06)
Strain induced variability

After W. Fichtner
ECAD tools can deal reasonably well
With deterministic variability
Restricted design rules and uniformity

After H. Onodera

- Irregular gate-poly pitch
- Horizontal poly wires
- Constant pitch with dummy poly insertions
- Dummy poly patterns
- Stretched gate-poly extensions
- Constant pitch with dummy poly insertions
- Stretched gate-poly extensions
- Single orientation
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Statistical variability

The simulation Paradigm now

A 22 nm MOSFET
In production 2008

A 4.2 nm MOSFET
In production 2023
Random discrete dopants

Atomistic process simulation
M. Jaraiz

Continuous process simulation
Synopsys

KMC Simulator
Line edge roughness (LER)

1D Fourier synthesis

\[ \Delta = 2 \text{ nm} \]
\[ \Delta = 12 \text{ nm} \]

\[ S(q) \text{ [arb.]} \]
\[ \text{wavenumber} \ [10^9 \text{ m}^{-1}] \]

\[ H(x) \text{ [nm]} \]
\[ \text{Distance [nm]} \]
Poly silicon grain boundaries

Poly Si grains, SEM

Interdigitised
High-κ morphology

\[ \text{HfO}_2 \]

\[ \text{HfSiO} \]
Measured and simulated variability
LP MOSFETs 45nm technology node

N-Channel
42 nm gate length

<table>
<thead>
<tr>
<th></th>
<th>$\sigma V_T$ (50 mV)</th>
<th>$\sigma V_T$ (1.1 V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Experiment</td>
<td>62 mV</td>
<td>69 mV</td>
</tr>
<tr>
<td>Simulation</td>
<td>62 mV</td>
<td>67 mV</td>
</tr>
</tbody>
</table>

Results from Crolles 2
Results from Atomistic Simulator
Combined variability in bulk MOSFETs

LER follows ITRS

LER = 4nm
The true shape of the distribution
Based on the simulation of 100,000 transistors
MOSFET capacitance variability

Gate capacitance

Drain capacitance
Interconnect variability

After: T. D. Drysdale

LER follows ITRS

LER=5nm

[Graphs showing delay distributions for different line lengths and process nodes]
Gate tunnelling leakage variability

- Interface pattern
- Electron distribution
- Current density

![Graphs showing gate voltage and current density for different conditions.](image-url)
Statistical reliability

- Continuous
- Single trap
- Multiple traps
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Deterministic vs. statistic variability

2 billion transistors: $V_{T1}=200\text{mV}$ $V_{T2}=300\text{mV}$

$\sigma V_T=10\text{mV}$ $\sigma V_T=50\text{mV}$ $\sigma V_T=100\text{mV}$
Compact model strategies

Lines: BSIM 3v3
Symbols: Data

Vgs = 0.35V
Vgs = 0.45V
Vgs = 0.55V
Vgs = 0.65V
Vgs = 0.75V
Vgs = 0.85V

Houston, We have a problem

Each plot is a scatter plot between the variable listed at the end of the row and the variable listed at the top of the column.

Vgs = 0.45V
Vgs = 0.35V
Vgs = 0.55V
Vgs = 0.65V
Vgs = 0.75V
Vgs = 0.85V

Relative error (%)

With parameter rdswmin, nfactor, voff, a1, a2 and d

With parameter vth0

With parameter vth0, voff

With parameter vth0, voff and rdswmin

Vd (Volts)
Impact of bulk MOSFET scaling of SRAM

![Graphs and diagrams illustrating the impact of bulk MOSFET scaling on SRAM performance.](image)

- **Top-left graph:** Shows the relationship between channel current density ($J_c$) and gate voltage ($V_G$) for atomistic average and continuously doped devices.

- **Top-right graph:** Displays the voltage output ($V_{out}$) for different cell ratios.

- **Bottom-left graph:** Represents frequency distribution for different channel lengths (13nm, 18nm, 25nm) with a cell ratio of 2.

- **Bottom-right graph:** Graphs SNM (Signal to Noise Margin) against cell ratio for different channel lengths and their mean values.
Hard logic faults

L/W=18/18nm

Vin [V]  Vout [V]

\( V_G \) [V]

\( V_{in} \) [V]

\( I_D \) [A]

\( V_{DD} \) [V]

\( \sigma V_T \) [V]

\( L \) [nm]

\( W \) [nm]

RRD EOT from Table 1

RRD EOT=1nm

Intel [23]
Timing variability

Timing variability

CMOS NAND
CPL NAND
DPL NAND
DOMINO NAND
DDCVS NAND

Voltage [V]

Time [s]

Frequency

Delay (ps)
Performance/Power/Yield (PPY) trade-off

Pareto optimal curve
(M. Horowitz, IEDM05)
The monitors and knobs approach

The “Technology Aware Design” of IMEC
The Power 6 processor of IBM
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Meeting the Design Challenges of Nano-CMOS Electronics - eScience Pilot Project

**University Partners**
- Edinburgh University *MMDGUE, NeSCE*
- Glasgow University *DMGUG, MSTGUG, NeSCG*
- Manchester University *APTGUM, eSNW*
- Southampton University *ESDGUS*
- York University *ISGUY*

**Industrial Partners**
- Synopsys, ARM, Wolfson Microelectronics, Freescale, National Semiconductors, Fujitsu, NMI

**Resources**
- £3.3M EPSRC, £4.1M FEC, £5.3M IC
- 11 PDRAs 7 Science4 e-Sci 7 PhD
Grid based statistical simulation

Future Research

Hardware + Software

System

Top level timing, and out-of-layout yield, and power (either calculated from toggle or by more detailed analysis). Manchester (Digital and Analogue), Glasgow DC, Edinburgh

Back Annotated RTL Synopsys

For each Logic block create a ‘card index’ of statistically generated blocks. Manchester, Southampton, York, Edinburgh, Glasgow Interconnect

Modelsim ??? Possibly VHDL-AMS

For each Standard Cell York, Southampton, Edinburgh, create a ‘card index’ of Glasgow (Devices). Glasgow Circuits statistically generated cells

Spice/Randomspice Aurora

For each transistor family create a ‘card index’ of statistically generated devices. Glasgow (Devices)

Geronimo

Standard toolset for some practical design, 80nm, 45nm?) complete, down past place & route, so that we have complete cell, device, interconnect information.
NANOSIL: Silicon-based nanostructures and nanodevices for long term nanoelectronics applications (EU FP7), R. Clerc

PULLNANO: Pulling the limits of the nano CMOS Electronics (EU FP6), H. Maes

REALITY: Reliable and variability tolerant system on a chip design in More-Moor technologies (EU FP7), B. Dierickx, IMEC

NanoCMOS: Meeting the design challenges of the nano-CMOS electronics (UK EPSRC), A. Asenov, GU

NanoMat: Meeting the material challenges of the nano CMOS electronics (UK EPSRC), A. Shluger, UCL
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Conclusions

- The statistical variability will be increasing in the next technology nodes.
- The statistical variability can not be reduced by fine tuning the technology, OPC and regular designs.
- The statistical variability demands statistical approach to design and will force fundamental design changes.
- The fabless and the chipless companies have to learn more about technology and devices.
Acknowledgements to all members of the Device Modelling Group

Department of Electronics and Electrical Engineering
University of Glasgow