# Physical Implementation of the DSPIN Network-on-Chip in the FAUST Architecture

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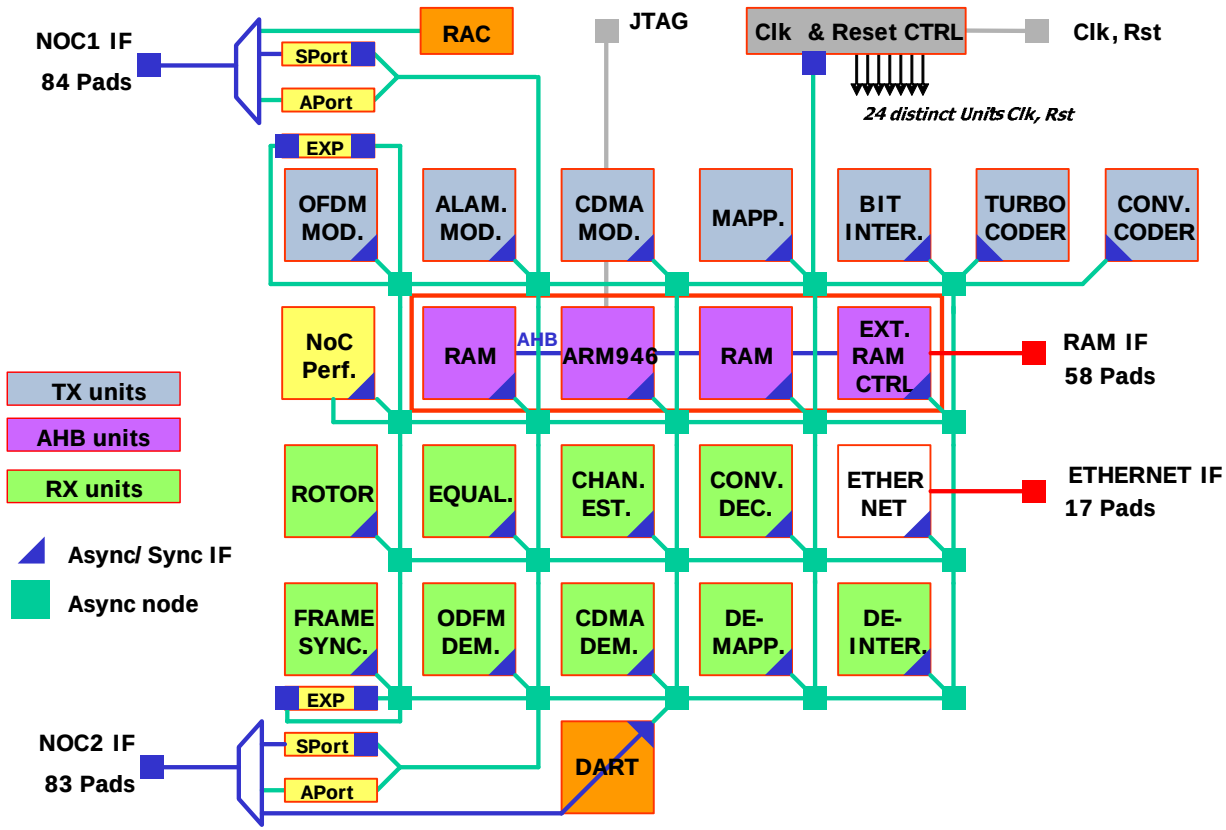
# Outline

- Motivation
- FAUST architecture
- Migration of DSPIN into FAUST
- DSPIN implementation
- Networks comparison

# Motivation

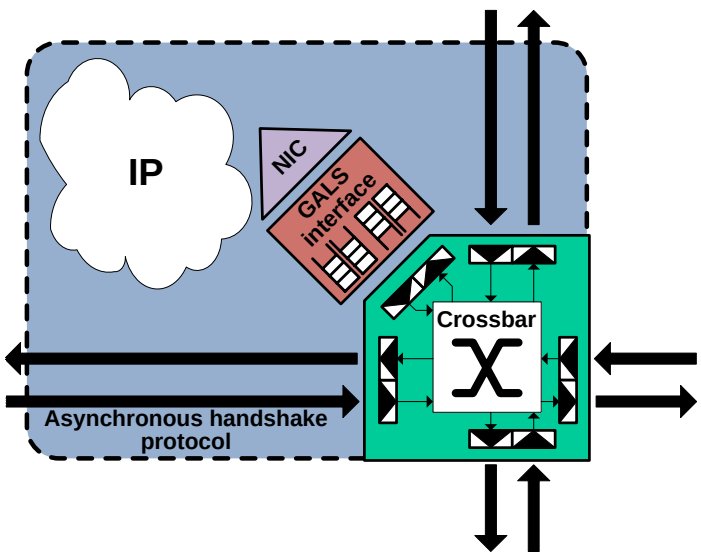
- Physically implement the DSPIN NoC into the FAUST application platform
  - DSPIN is a NoC developed between Lip6 and ST
  - FAUST is a stream-oriented application platform for 4G telecom applications, based on ANOC, developed by CEA-Leti.
- Compare the performances between ANOC and DSPIN on a real application and traffic

# FAUST architecture



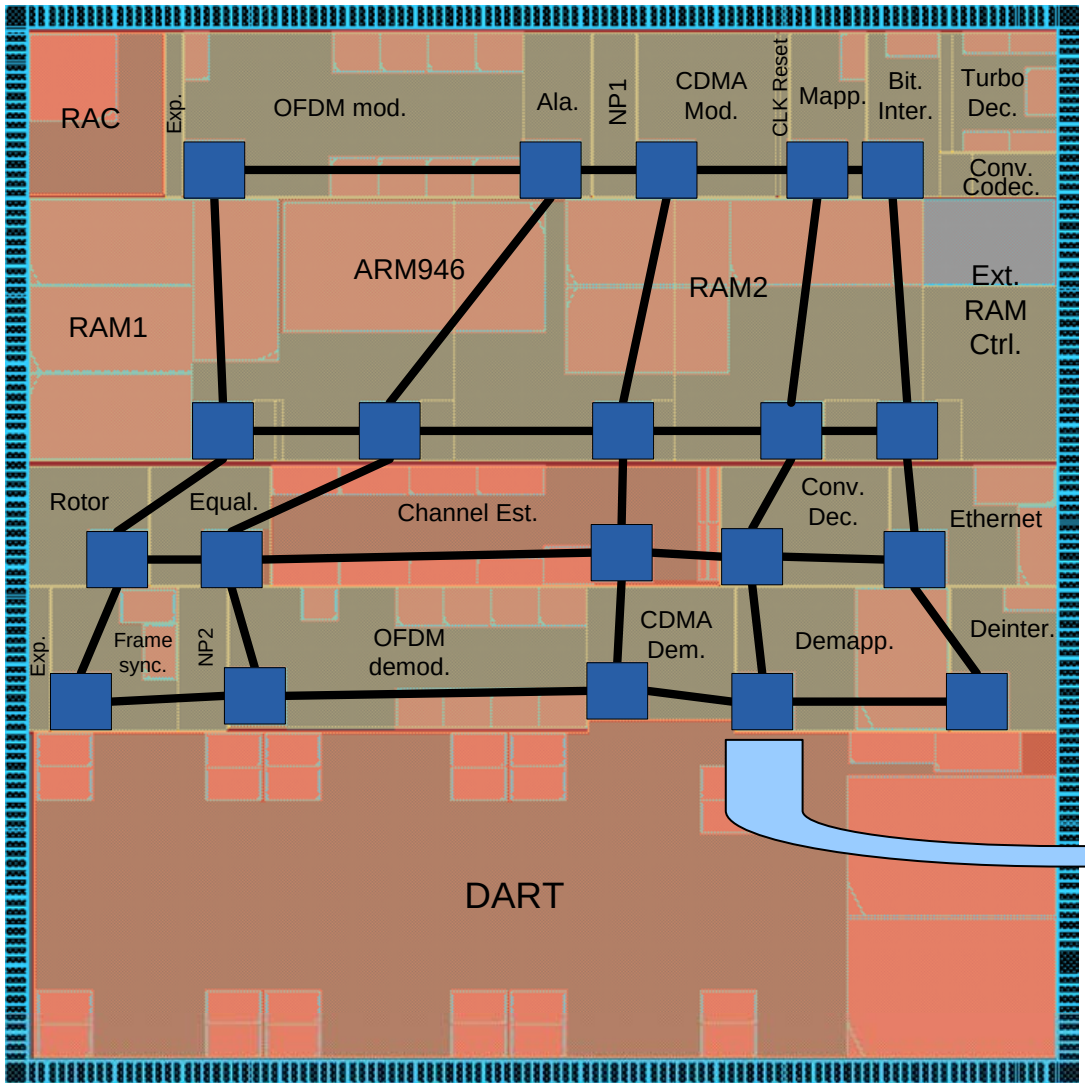

- 23 computation units
- Asynchronous NoC (ANOC)
- 20 ANOC routers
- GALS conception
- 24 independent Clks
- Ethernet port
- Internal/External RAM
- CPU ARM946ES
- Cache 4KB-I 4KB-D
- Hardware OFDM modulation/demodulation

# ANOC architecture



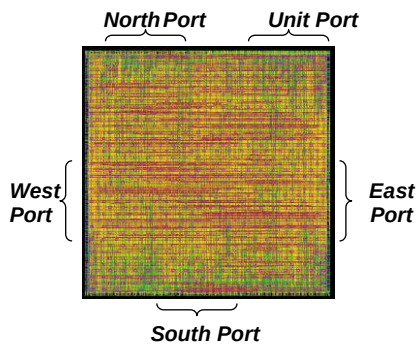

- Asynchronous NoC
  - Asynchronous send/accept handshake protocol
  - QDI 4-phase/4-rail asynchronous logic
  - QoS with two Virtual Channels (Best Effort, Guaranteed Service)
- NoC Routers
  - 5 ports router
  - Source routing
  - Wormhole packet switching
  - 32 bits payload
- FIFO based GALS interfaces
- Mapped onto libraries
  - CMOS ST 130nm
  - TIMA TAL130 library

# FAUST floor-plan with ANOC




- 4.5 M Gates
- 276 chip pins
- Chip area 80 mm²
- ST CMOS 130nm
- 166 MHz (worst-case)

- NoC implementation :
  - Uses ANOC router hard-macro
  - Perform buffering and routing of ANOC links
  - No spaghetti routing at top level !




ANOC router (0.211 mm²)

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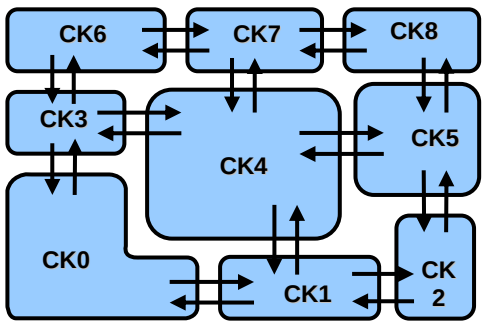
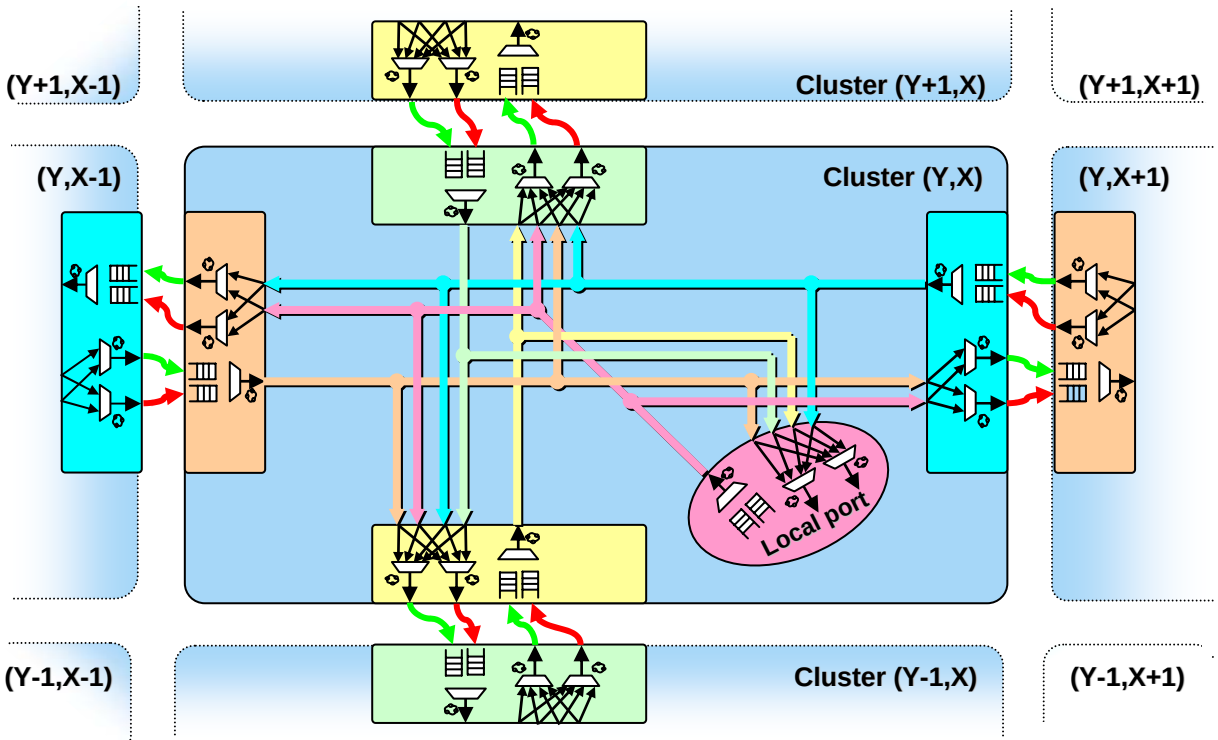
# DSPIN architecture




- Packet base
- Distributed router architecture
- Suited to GALS approach
- **Mesochronous links** between routers
- **Synthesizable with standard cells**
- **Neither asynchronous nor custom cells**
- Metastability resolved by “bi-synchronous FIFO”

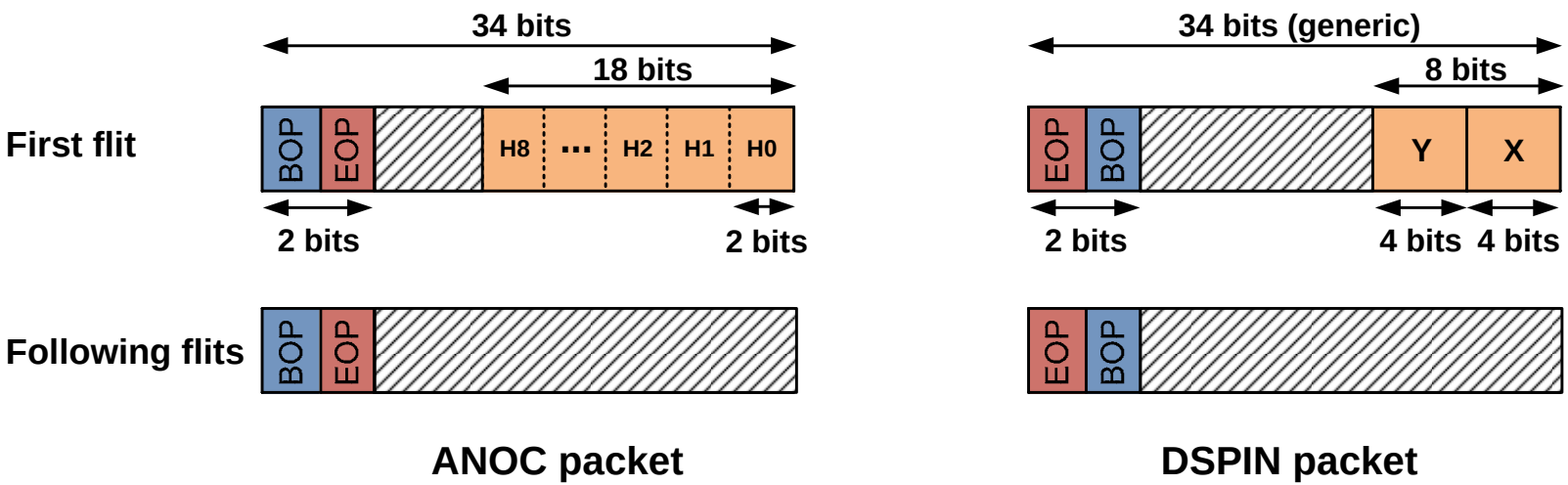
More details in:

*"A Low Cost Network-on-Chip with Guaranteed Service Well Suited to the GALS Approach“* NanoNet’06

# NoC architectures comparison

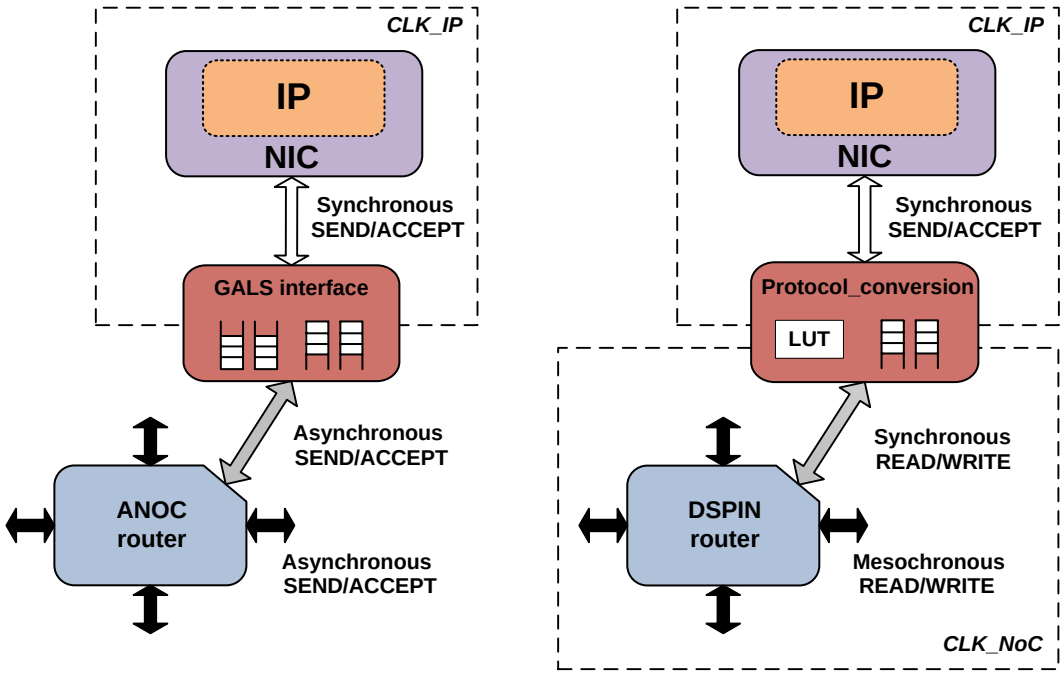
| | ANOC | DSPIN |
|---|---|---|
| Router arity | 5 port router | 5 port router |
| Topology | Irregular 2D mesh | Regular 2D mesh |
| Routing technique | Source routing (9 hops) | Address-based (8 bits) X-First algorithm |
| Switching technique | Wormhole | Wormhole |
| Flit size (payload) | 34 bits (32 bits) | Generic: 34 bits (32 bits) |
| Flow control bits on the flit | Begin of packet (BOP)<br>End of packet (EOP) | Begin of packet (BOP)<br>End of packet (EOP) |
| Virtual channels | Best effort<br>Guaranteed service | Best effort<br>Guaranteed service |
| Programming model | Message passing | Shared memory (2 routers per cluster)<br>Message passing (1 router per cluster) |
| Clocking scheme | Fully asynchronous (QDI) with GALS interfaces | Multi-synchronous with mesochronous interfaces |
| Flow control protocol | Send/accept asynchronous handshake | FIFO protocol (Write and WriteOk) |
| Clock tree | None | One per router |
| Physical implementation | Hard macro | Soft macro distributed on five modules |
| Long wires | Inter-router wires | Intra-cluster wires |

# Packet format




- Similar packet format and control bits
- ANOC uses Source-routing (18 bits) allowing 9 hops
- DSPIN uses Address-based (8 bits)
- Packet conversion module required:
  - Design of ***Protocol_conversion*** module

# FAUST integration




**ANOC IP template** **DSPIN IP template**

**Protocol_conversion module:**

- Translates the routing algorithm using a LUT
- Adapts the flow control signals:
  - ANOC: Send/Accept
  - DSPIN: FIFO protocol
- Implements two bi-synchronous FIFOs

**ANOC GALS Interface:**

Implements 4 FIFOs

synchronous↔asynchronous

*FAUST IPs and NICs are not modified*

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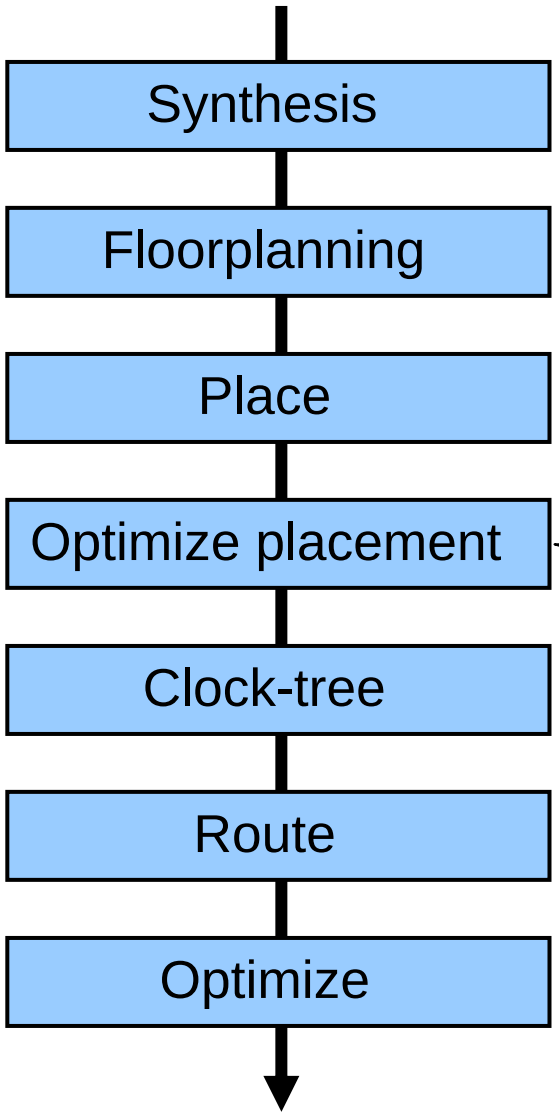
# DSPIN implementation

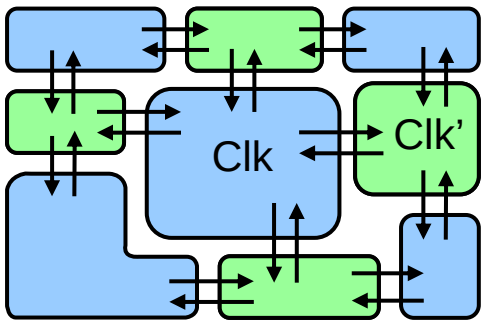


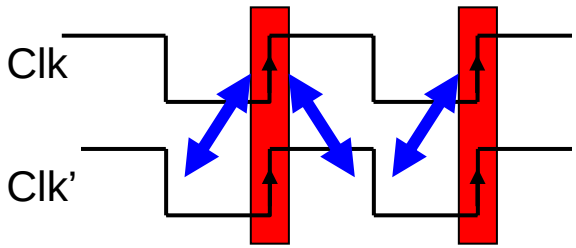

- Hierarchical synthesis
- Low Power CMOS ST 130nm technology
- Standard cells
- Without asynchronous nor custom cells

- Timing constraints file:
  - Muti-cycle path (mesochronous interfaces)
  - False path (asynchronous interfaces)

- GALS compatible
- Clock gating
- Implemented in 4 steps

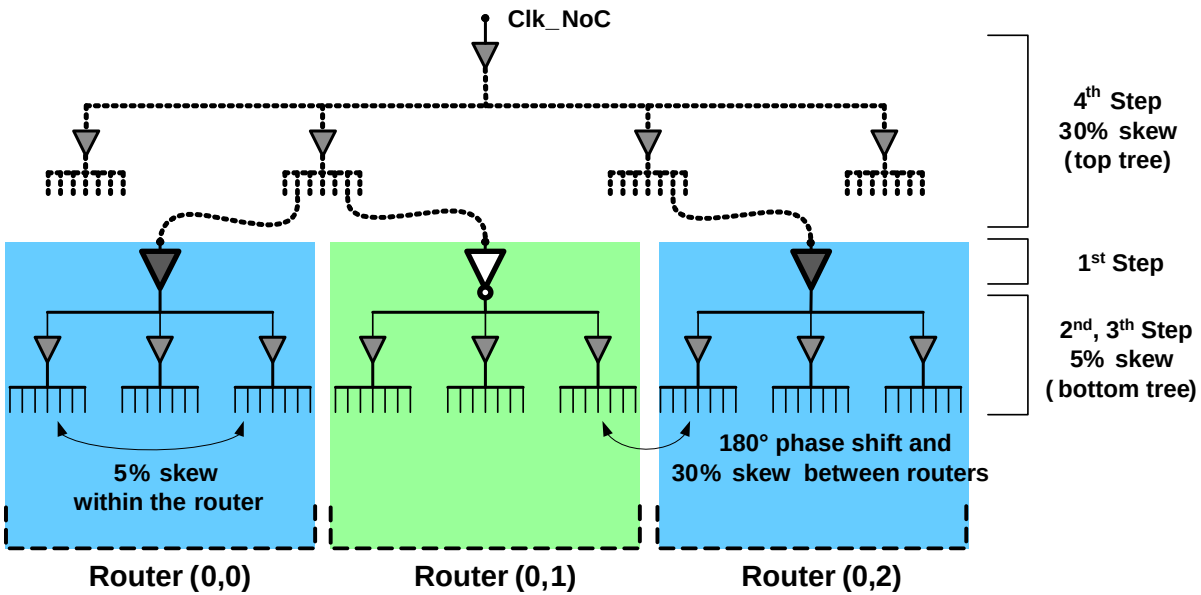
# DSPIN clock-tree




**Mesochronous links**

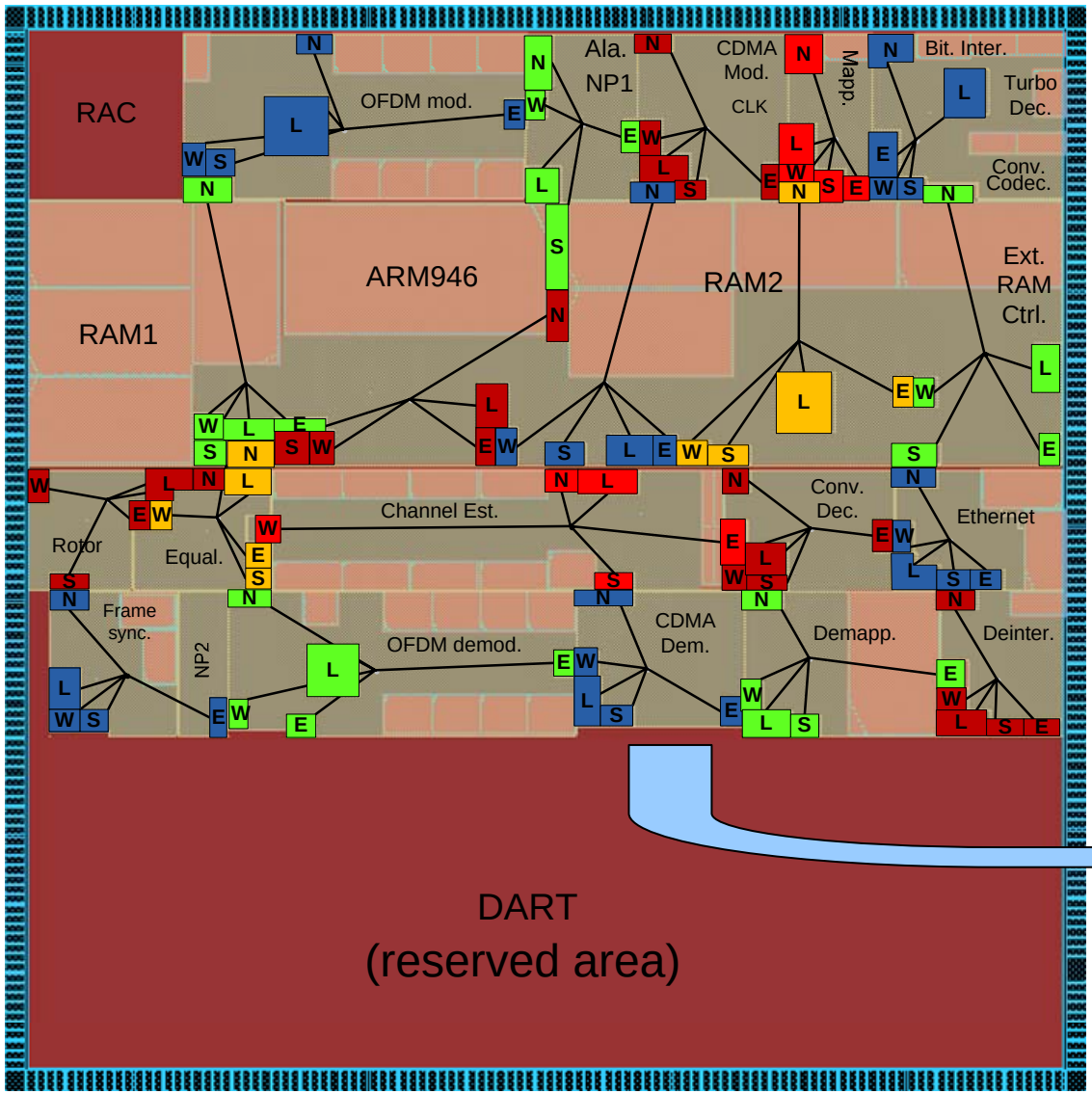
- GALS compatible
- Bi-synchronous FIFO [NOCS 2007]
- Max skew 50% clock period
- Timing constraints: set_multi_cycle_path



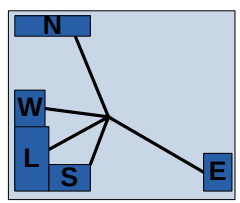

**Clock-tree implementation**

1. Add buffers/inverters
2. Built bottom clock tree (5% skew)
3. Characterize bottom clock-tree
4. Build top clock-tree (30% skew)

# FAUST floor-plan with DSPIN



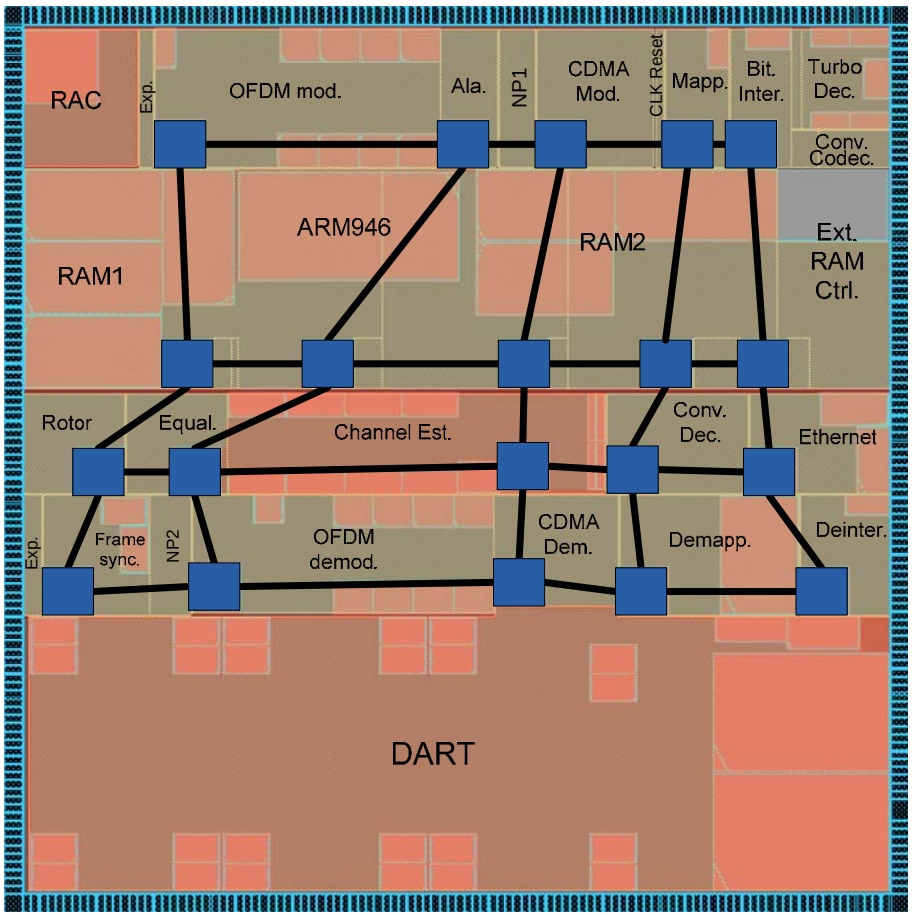

- Distributed router implementation
- Soft macro approach
- Higher floor-plan flexibility
- NoC adapts to the SoC
- Long wires are routed in a tree manner
- Different router configurations are possible



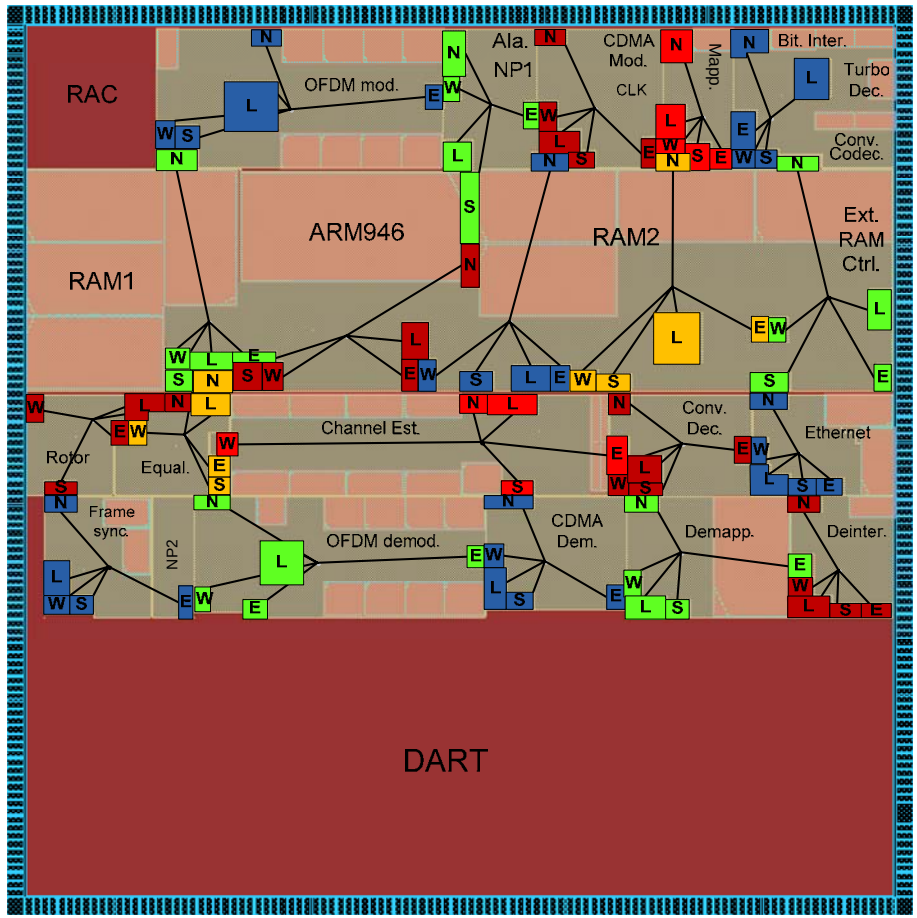

DSPIN router

Placement density: 60-70 %

# FAUST floor-plan




FAUST with ANOC




FAUST with DSPIN

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# NoC Area

| | ANOC | DSPIN |
|---|---|---|
| Router | 0.211 mm² | 0.161 mm² |
| Interface GALS | 0.070 mm² | 0.024 mm² |
| Clock tree | 0.000 mm² | 0.0016 mm² |
| **Total** | **0.281 mm²** | **0.187 mm²** |

CMOS 130nm

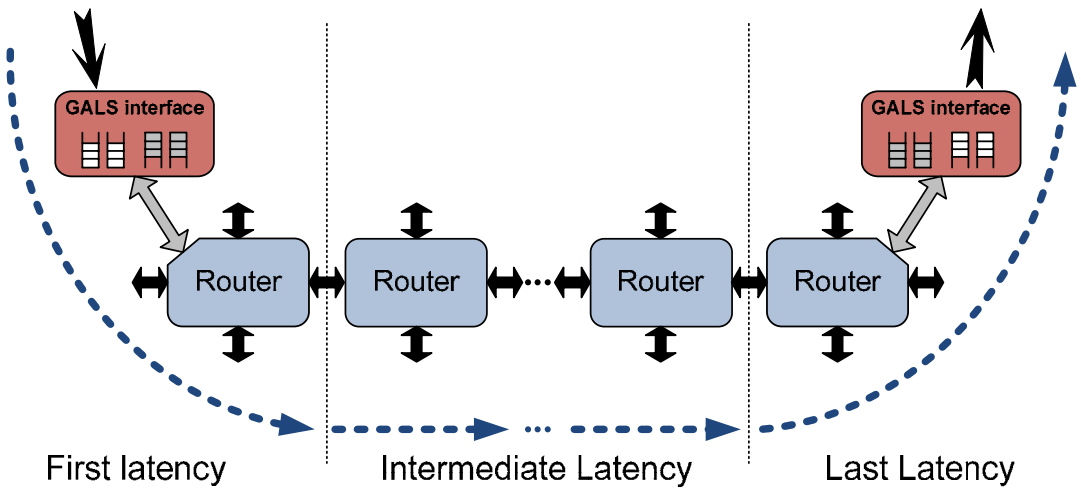
- ANOC is implemented as a hard macro
- DSPIN is implemented as a soft macro
- DSPIN is 33% smaller than ANOC

# NoC Throughput

| | ANOC | DSPIN |
|---|---|---|
| Throughput on worst-case conditions | ~ 160Mflit/s | ≤ 289Mflit/s |
| Throughput on nominal conditions | ~ 220Mflit/s | ≤ 408Mflit/s |

- DSPIN throughput is **deterministic** with respect to the clock frequency (one flit per clock cycle)
- Long wire latency penalty on throughput:
  - DSPIN: critical path crosses one time the long wires
  - ANOC: critical path crosses 4 times the long wires, 4-phase protocol
    - ANOC link pipelining is feasible
- In a commercial circuit, DSPIN will be clocked not far away from worst-case (289 MHz) to improve the fabrication yield

# Packet latency (1)




| | ANOC | DSPIN | ANOC | DSPIN |
|---|---|---|---|---|
| | F = 150 MHz | | F = 250 MHz | |
| Intermediate router latency | 6.80 ns | 16.66 ns | 6.80 ns | 10.00 ns |
| First + Last latency | 60.00 ns | 56.66 ns | 47.00 ns | 34.00 ns |

- Compute the packet latency through many routers
- DSPIN has **deterministic** packet latency with respect to clock frequency
- DSPIN has lower *First* and *Last* packet latencies
- ANOC *intermediate latency* is lower than DSPIN. DSPIN resynchronize the data on each router

# Packet latency (2)

| | ANOC | DSPIN | ANOC | DSPIN |
|---|---|---|---|---|
| | F = 150 MHz | | F = 250 MHz | |
| Latency for 5 hops path | 80.00 ns | 106.66 ns | 68.00 ns | 64.00 ns |
| Latency for 9 hops path | 106.66 ns | 173.30 ns | 96.00 ns | 104.00 ns |

- The packet latency are similar for clock frequencies >250 MHz
- *Intermediate packet latency* is important but the application should be mapped in order to optimize the data locality (try to communicate with neighbor IPs rather than with faraway IPs)

# Power consumption

| | ANOC | DSPIN | |
|---|---|---|---|
| | | F = 150 MHz | F = 250 MHz |
| Router | 2.07 mW | 2.89 mW | 4.85 mW |
| GALS interface | 1.62 mW | 0.56 mW | 0.81 mW |
| Clock tree | 0.00 mW | 2.44 mW | 4.73 mW |
| **Total** | **3.69 mW** | **5.89 mW** | **10.39 mW** |

- Power extraction after P&R
- Functional packet traffic (OFDM demodulation)
- Power consumption majorly dominated by FIFO data registers
- The DSPIN clock-gating reduced the power consumption by 67%
- DSPIN clock-tree consumes as much power as the router itself
  - Needs to improve DSPIN clock-gating
  - GALS clock-tree consumes only 2.5% of total clock-tree power

# Conclusion

- Physical implementation of the DSPIN Network-on-Chip on FAUST platform
  - Comparison between ANOC and DSPIN at architecture level
  - Adaptation of DSPIN architecture to manage stream-oriented communications
  - Implementation up to layout of DSPIN network on FAUST platform

  => *DSPIN mesochronous links fully implemented with standard tools*

- Comparison between DSPIN and ANOC NoCs (*STMicroelectronics 130nm*)
  - Area of DSPIN is 33% smaller than ANOC one
  - Maximum sustained throughput of DSPIN is 31% higher than ANOC
  - ANOC has lower packet latency
  - DSPIN power consumption 1.5 to 3 times higher than ANOC
- ANOC is a good candidate for low latency and low power applications, while DSPIN is more suited to low area and high performance applications


*See you at my PhD defense on May 20th*