Asynchronous Nano-Electronics

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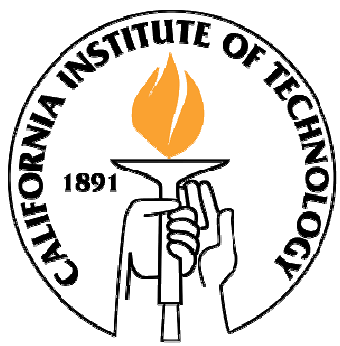


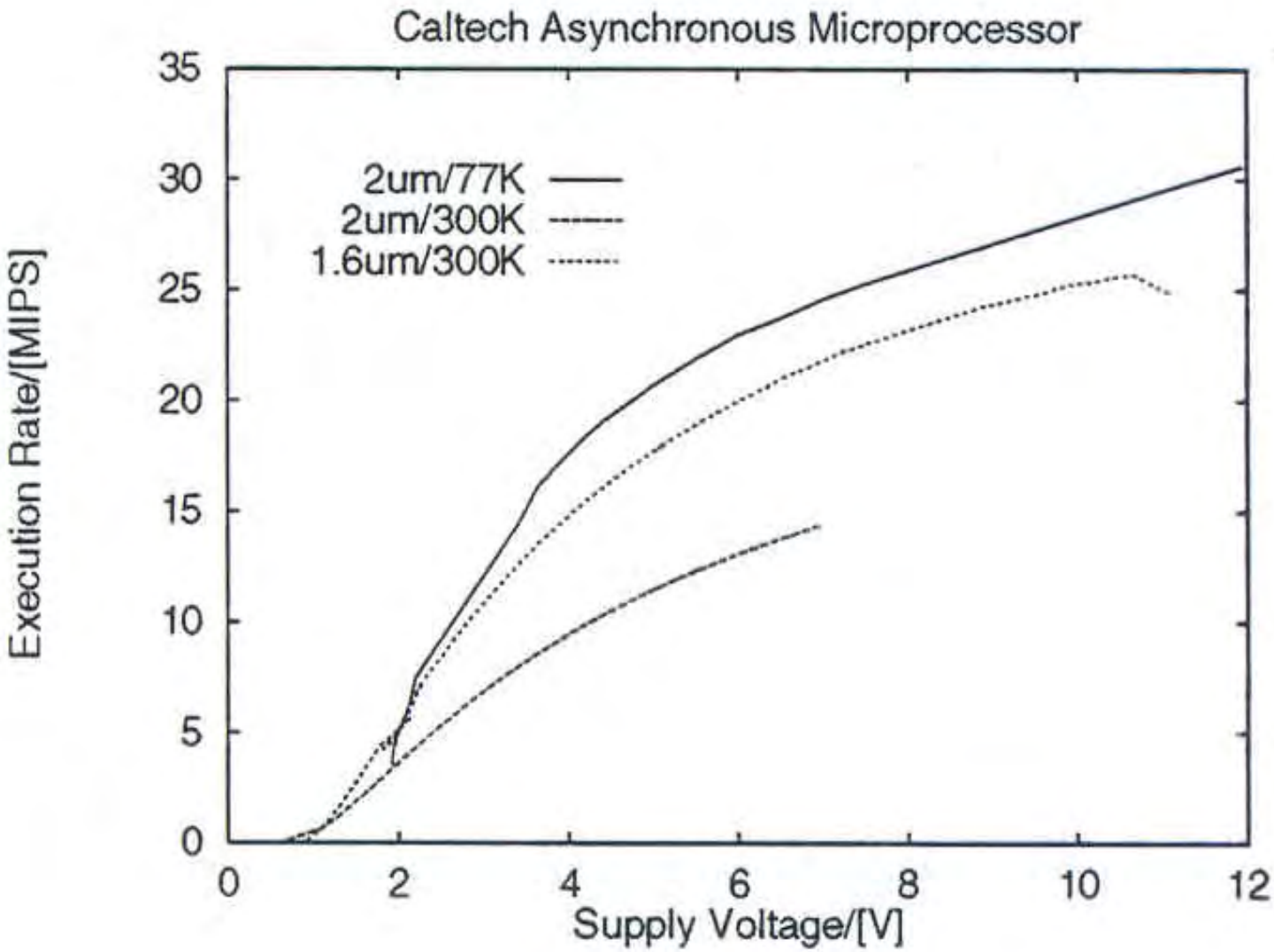
Async2008, April 2008

Why Asynchrony for nano?

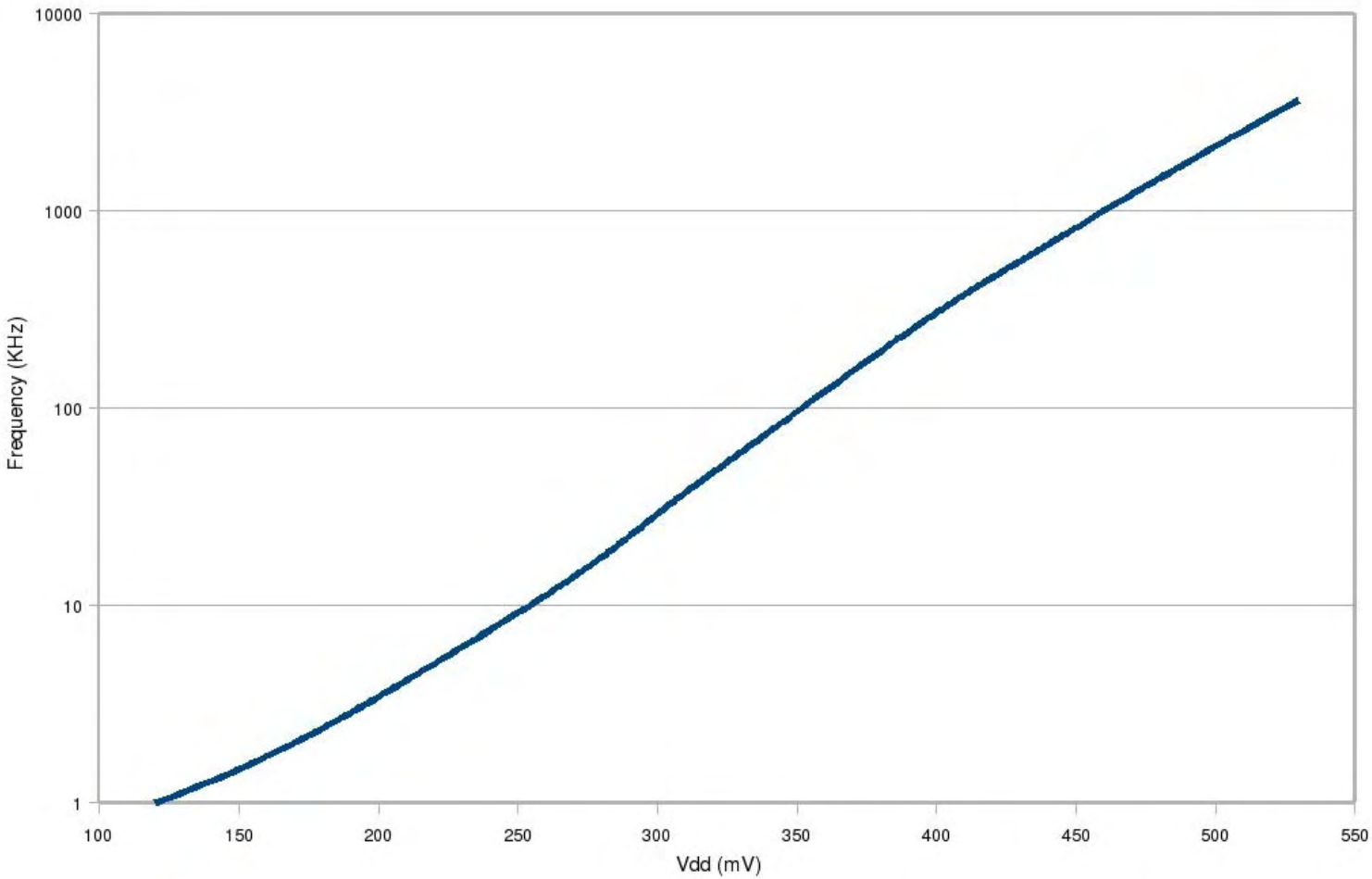
- The robustness of asynchronous QDI logic to timing variations can absorb the important parameter variations of nano technology
- No clock network in nano
- Can we increase the reliability of QDI even further (XQDI)?
- Applicable to nano CMOS as well

QDI tolerance to variations

Robustness to Voltage and Temperature Variations



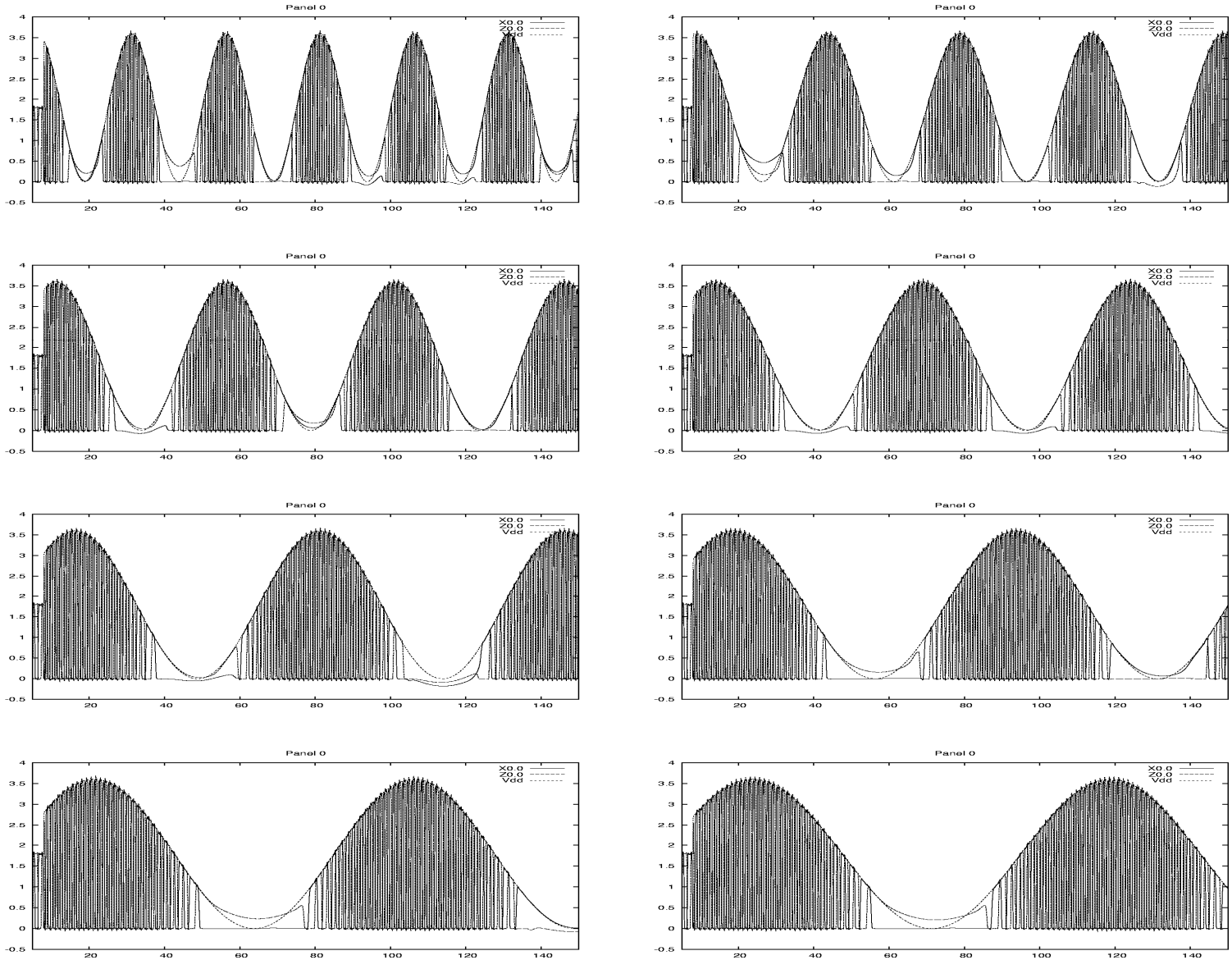
SUBTHRESHOLD OPERATION (RING OF PCHBs in TSMC 0.18)



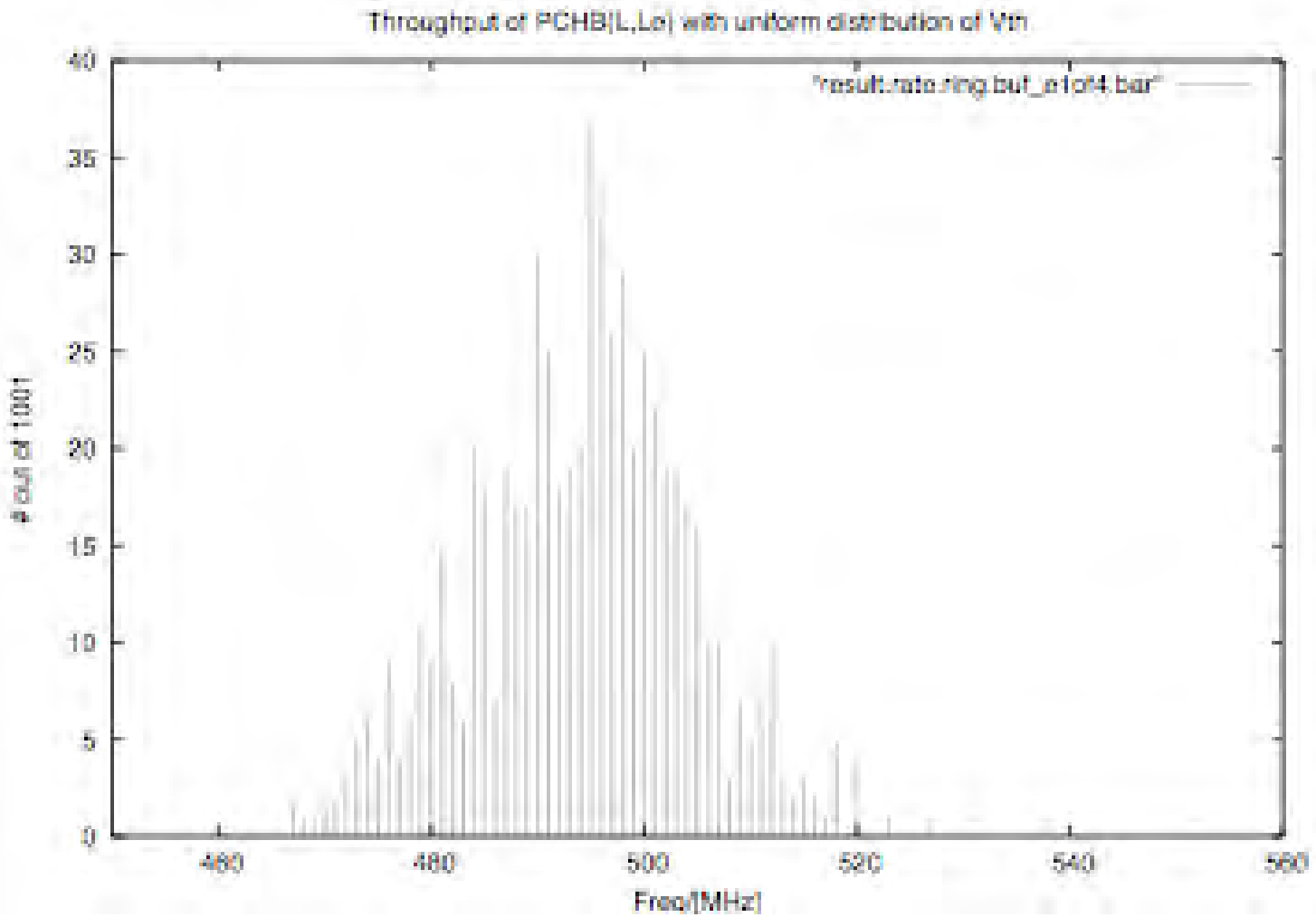
Robustness to Power-Supply Noise

The following slide shows the result of an HPSICE simulation of a typical QDI asynchronous circuit:
A five-stage ring of async (PCHB) pipeline stages.
Technology: TSMC 0.18micron CMOS
Vdd: 1.8V, Vt : .5V, Complete layout.
Vdd is oscillating between 3.5V and 0V (maximal amplitude), and at various frequencies. The circuit keeps working correctly!
(It will malfunction at some very high-frequency noise in phase with circuit frequency.)

Robustness to Power-Supply Noise



Tolerance to Vth Variation

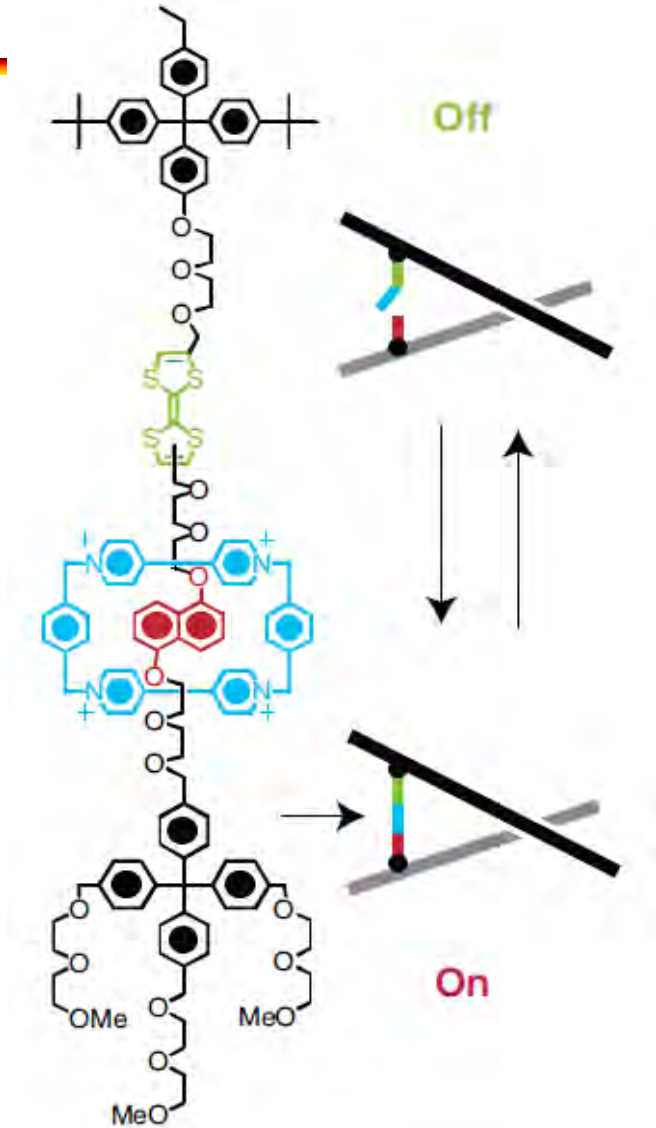


Molecular Nano-electronics

Molecular Nano-electronics

- Self-assembly (or nano-imprint) of molecular silicon nano-wires (NW) arranged in a grid
- Wire ~ 5nm diameter, < 10 micron length
- Resistors and diodes can be constructed at junction of 2 orthogonal wires
- High density: 10**10 to 10**12 devices/cm2
- Enough to build wired-or logic, but no gain
- Transistors with gain also possible at a junction: top metal wire crossing a doped semiconducting bottow NW create a transistor (p-type easier to build than n-type but both exist)

Programmable Junction

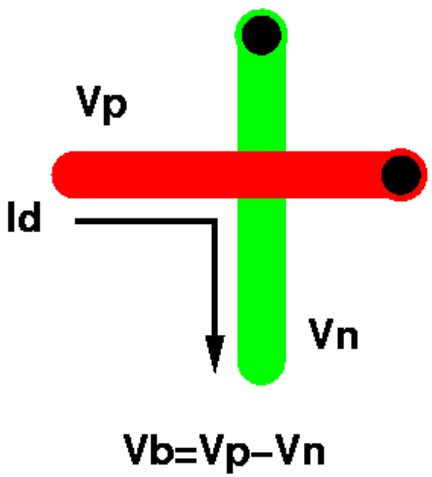


From Science 2004, Flood et al.

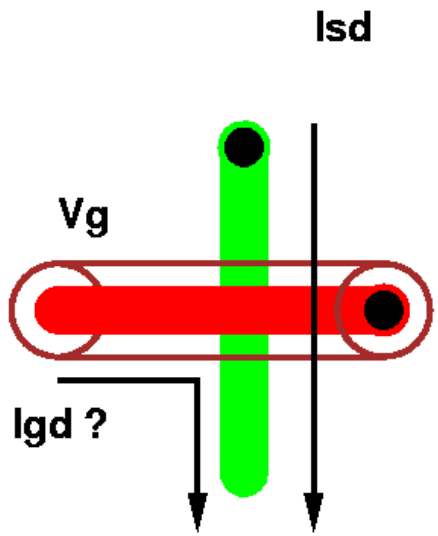
Junction Devices

Doped nanowires give:

Diode and FET Junctions



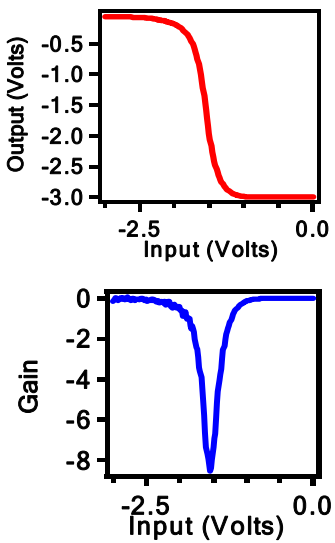
Cui…Lieber (2001)
Science 291 p851

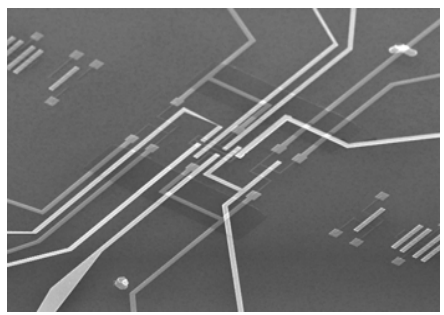


Huang…Lieber (2001)
Science 294 p1313

Complementary NW Transistors

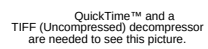
Improved p- and n-type NW transistors with good performance and reliability built in Heath's lab at Caltech.
High yield inverters with gain ~10 are obtained reliably.
The fabrication process enables complex circuitry such as the XOR gate shown on the right.





Complementary NW Transistors

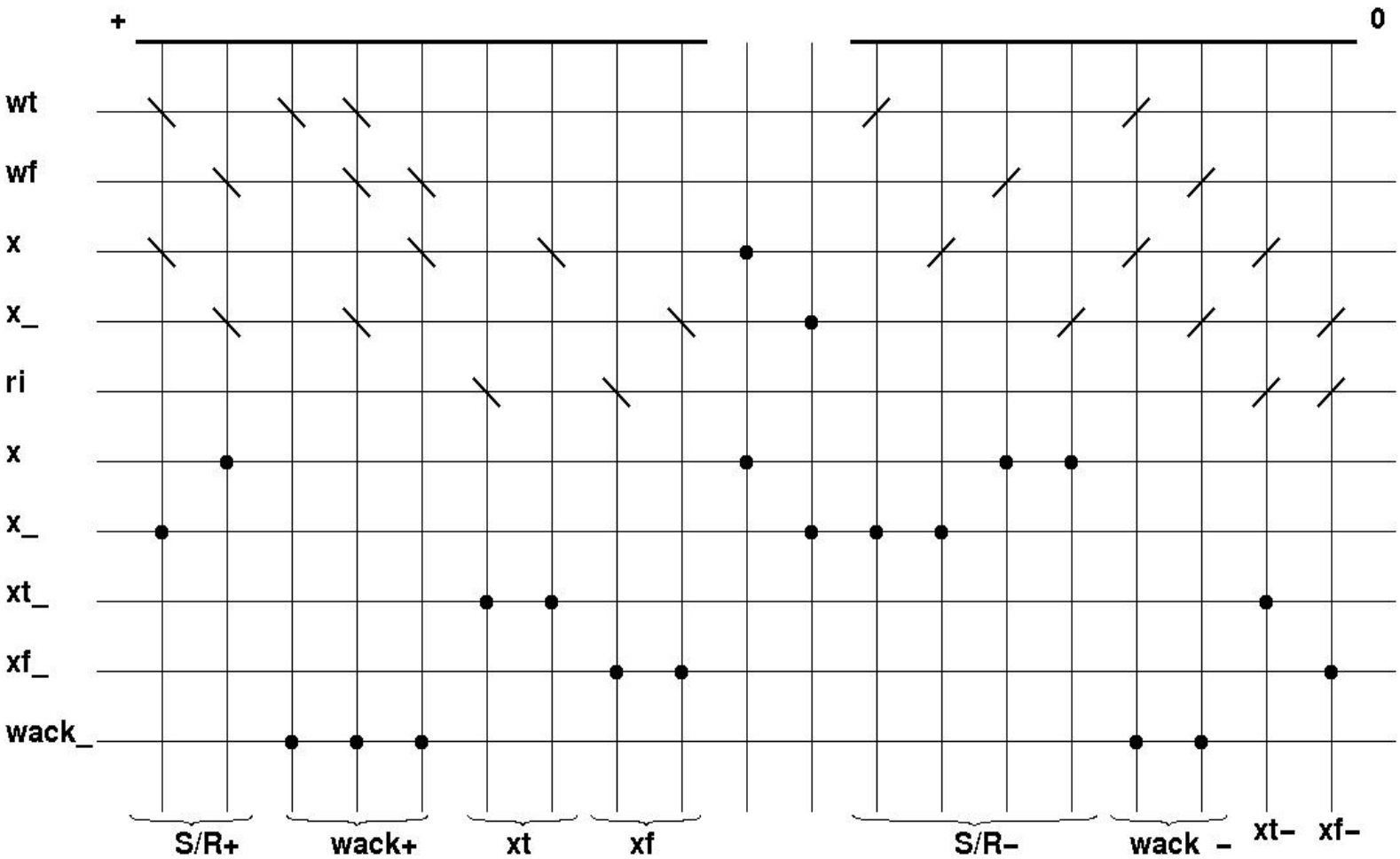
From C.Lieber, Harvard



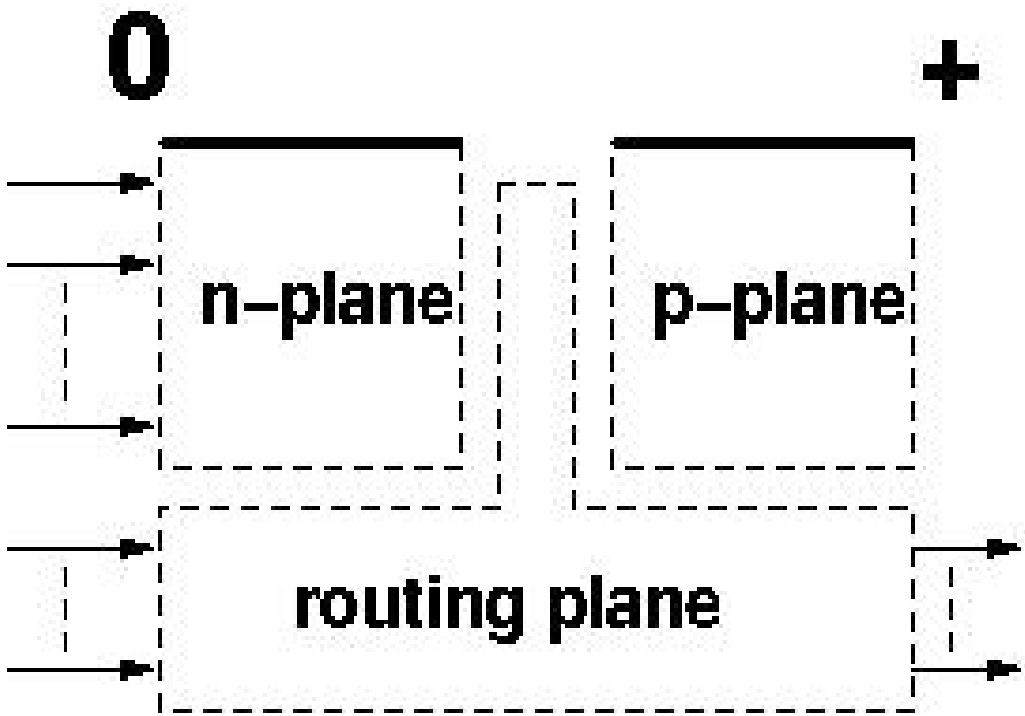
Hypothetical Target Technology

- Inspired by HP technology
- Basic building block: tile of about 100x100 wires
- Tile can be either only routing or computing
- Connections only through orthogonal crossing
- Computing tile: n-plane, p-plane, routing plane
- Connection resistance high (~100K ohms) and highly variable
- Transistor gain “good enough” (~10)
- Up to 10% wires broken
- Vdd/ GND in silicon layer

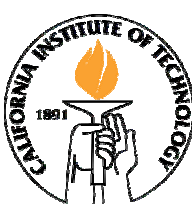
Example: Register Nano-Layout



General Layout Scheme

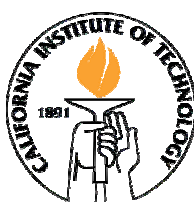


Nano-async



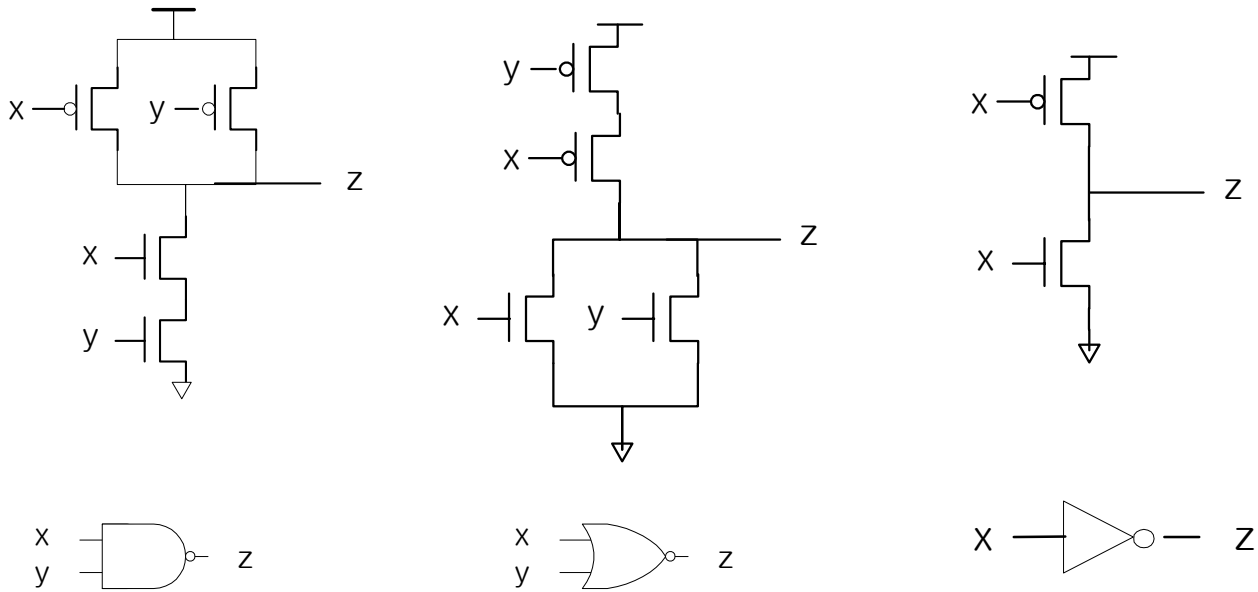
Reliability Issues in Nano-QDI

- Designing gates:
  - Restricted geometry
  - State-holding gates
- Designing systems:
  - Isochronic forks
  - Oscillating rings of gates
- Defect and fault tolerance
  - Not part of this talk



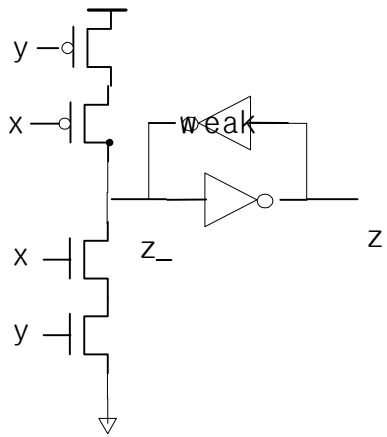
Combinational Gates

- nand, nor, inverter

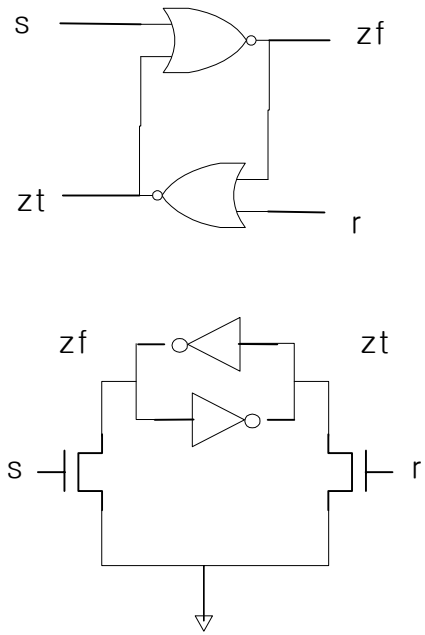


State-holding Gates

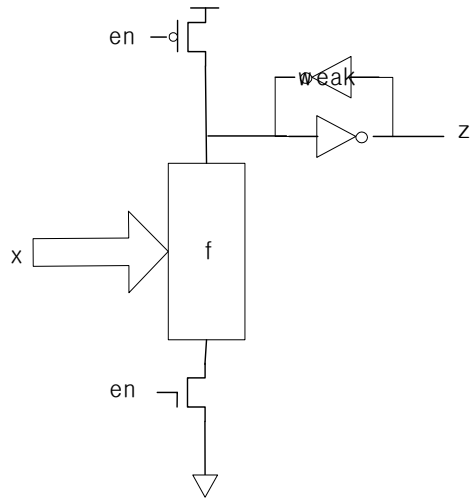
- C-element , Set-reset latch, precharge logic



C-element



Set-reset latch

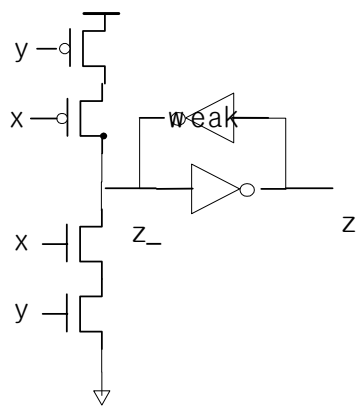


precharge logic

Holding State

- A gate is the implementation of the pair of production rules:
  $Bu \rightarrow z\uparrow$
  $Bd \rightarrow z\downarrow$
  What happens when Bu and Bd are both false?
- State-holding gate: z must keep its current value.
- Usual solution ("keeper" or "staticizer") always maintain the current value:
- $Bu \vee z \rightarrow z\_\downarrow \quad , \quad \neg z\_ \rightarrow z\uparrow$
  $Bd \vee \neg z \rightarrow z\_\uparrow \quad , \quad z\_ \rightarrow z\downarrow$

Fight when the value of z is changed!



Holding State with Keeper

- Keeper requires balancing current strengths.
- The current through the weak pullup $\neg z\_ \rightarrow z\uparrow$ must be:
  - (1) strong enough to compensate leakage and
  - (2) weak enough to "loose the fight" against the current through the pulldown Bu $\rightarrow z\_\downarrow$
- And similarly for the weak pulldown

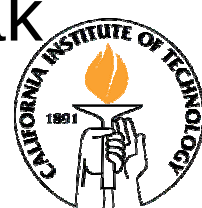
- Two-sided inequality on currents. Difficult with variability…

Holding State without Keeper

- Any state-holding gate can be transformed into a combinational gate with feedback
- General transformation: add the extra terms only when $\neg Bu \wedge \neg Bd$ holds (in the "floating" states)

- $Bu \vee \neg Bd \wedge z \rightarrow z\_\downarrow$, $\neg z\_ \rightarrow z\uparrow$
  $Bd \vee \neg Bu \wedge \neg z \rightarrow z\_\uparrow$, $z\_ \rightarrow z\downarrow$

- Drawback: possibly complex conditions with many transistors in series, resulting in too weak current to prevent leakage.



C-element without Keeper

- $x \wedge y \rightarrow z\uparrow$

  $\neg x \wedge \neg y \rightarrow z\downarrow$

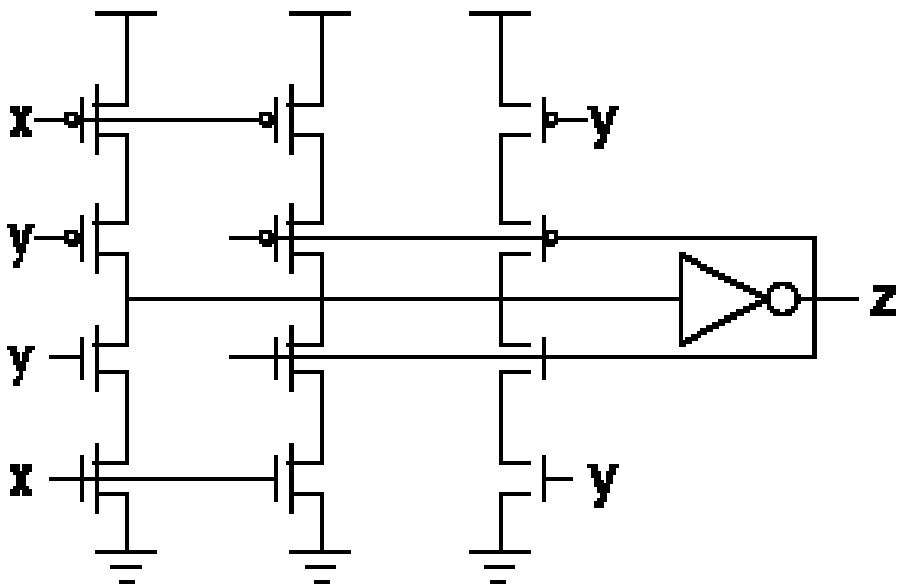
- Combinational logic transformation:

  $(x \wedge y) \vee (x \wedge z) \vee (y \wedge z) \rightarrow z\_\downarrow$

  $(\neg x \wedge \neg y) \vee (\neg x \wedge \neg z) \vee (\neg y \wedge \neg z) \rightarrow z\_\uparrow$

  $\neg z\_ \rightarrow z\uparrow$

  $z\_ \rightarrow z\downarrow$



Precharge Function

- $en \wedge F \rightarrow z\_\downarrow$
  $\neg en \rightarrow z\_\uparrow$

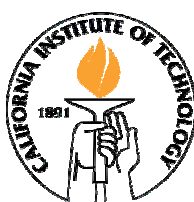
General transformation:

- $en \wedge F \ v \ en \wedge z \rightarrow z\_\downarrow$
  $\neg en \ v \ \neg F \wedge \neg z \rightarrow z\_\uparrow$

- It may be possible to simplify or eliminate the floating states using invariants: example of dual-rail precharge function
- The performance of fine-grain PCHB-like pipelines may be difficult to achieve without keepers…

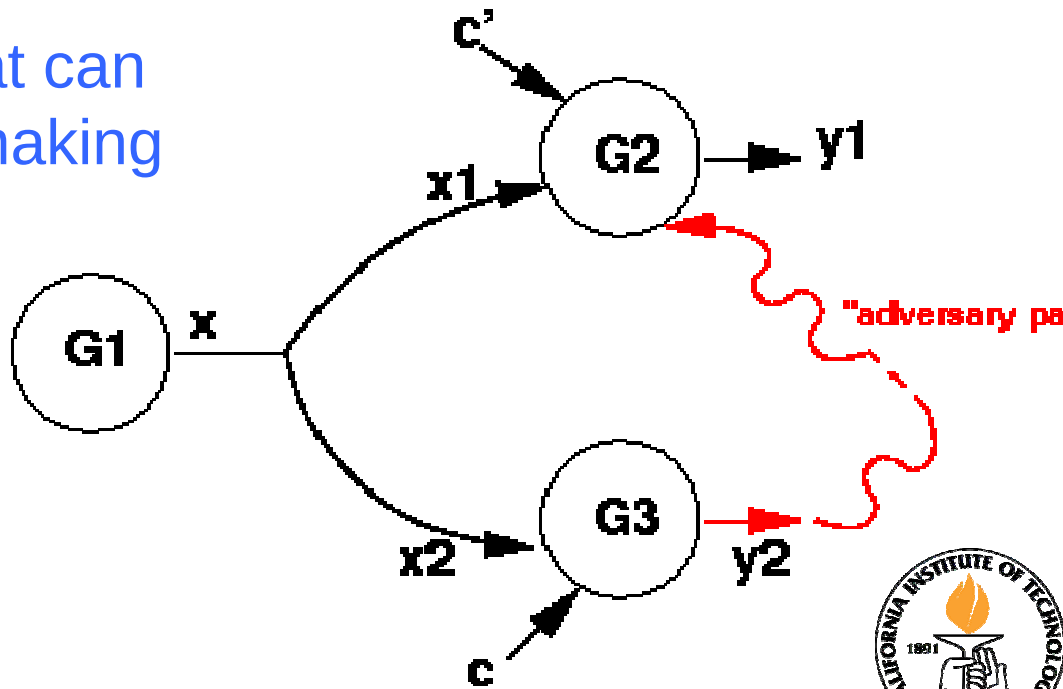
Second Issue: Isochronic Forks

- We have proved that the class of entirely DI circuits (no isochronic fork) is very limited: We cannot avoid isochronic forks.
- The usual timing assumption on isochronic forks is too strong. (Sufficient but not necessary.)
  - "the difference between the delays on the branches of the fork is negligible."
- Difference between "cut" and "tie" transitions



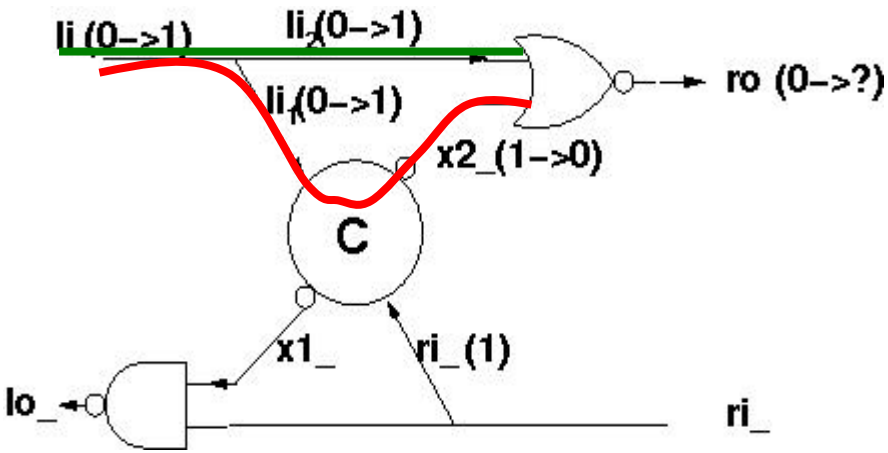
Weakest Isochronic Fork Assumption

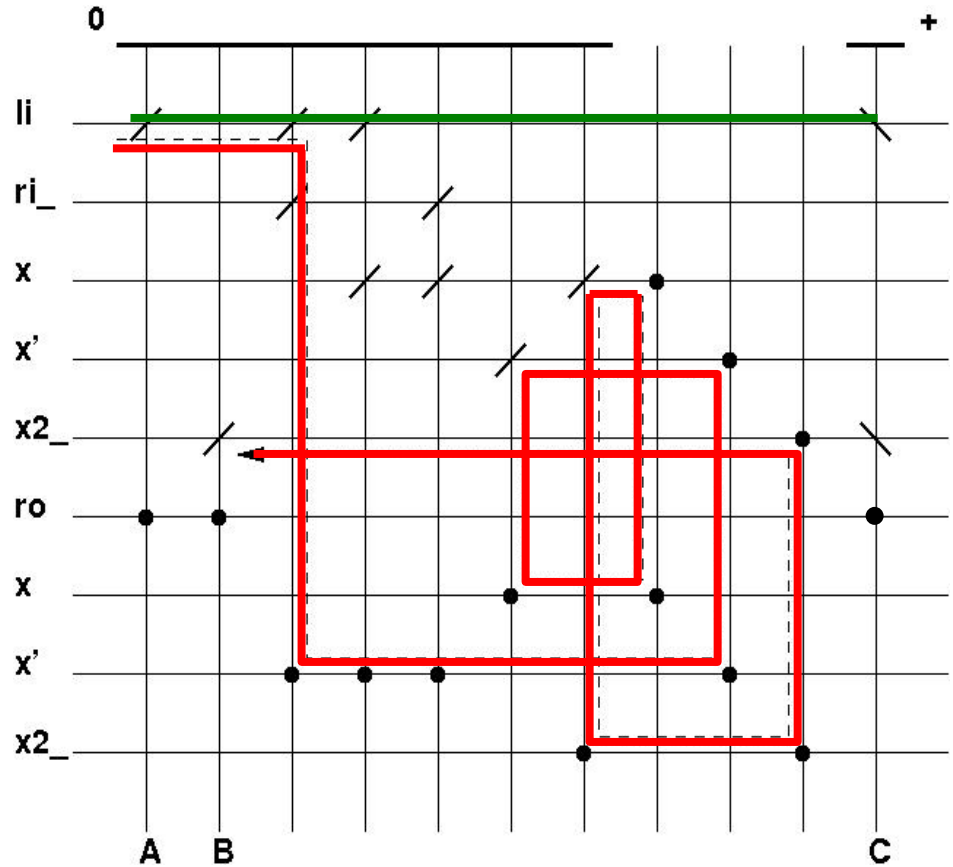
- Transition delay of the isochronic branch is less than the delay of the adversary path
- d(single transition) << d(multi-transition path)
- One-sided inequality that can always be satisfied by making adversary path longer



Isochronic Fork: Nano implementation

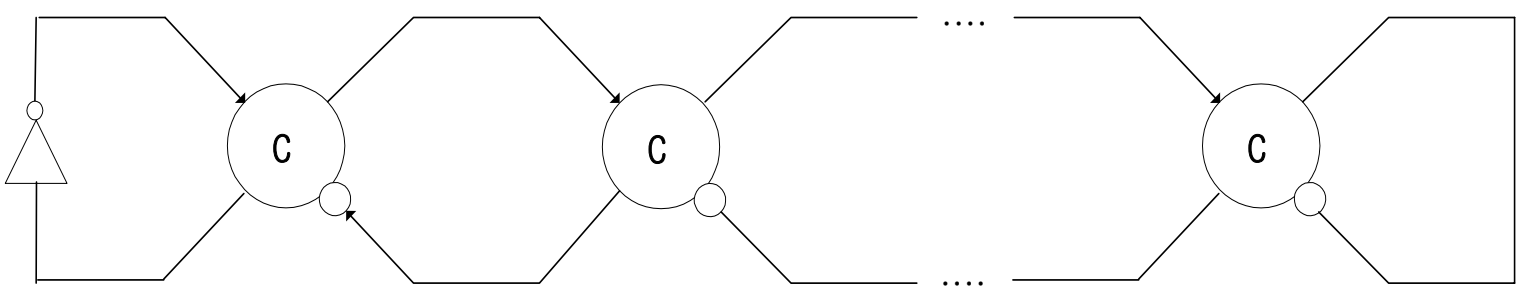
d(single transition)<<3*d(transistor-chain)+9*RC-delays





Third Issue: Ring Oscillators

- An async system is a collection of rings of operators.
- Each transition z↑ is eventually followed by a transition z↓ on a ring. How do we guarantee that z↑ does not self-invalidate through a sequence of fast transitions leading to z↓ ?



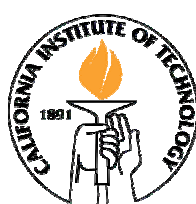
Ring Oscillators, cont.

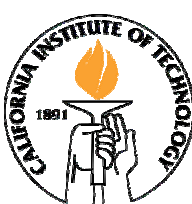
- What are the requirements on the technology to guarantee that each ring oscillates?
- Sufficient condition (requires gain):
- Longest transition << shortest transition * (n-1)
- Where n = # inverting stages

Conclusion: Recipe to build XQDI circuits

- At least diodes to build boolean logic
- Transistors for gain
- State-holding gates: avoid keepers entirely (possible but can be expensive)
- It is not possible to avoid isochronic forks but…
- Timing assumption on isochronic fork is a one-sided inequality that can always be satisfied
- Rings of operators need to have gain and satisfy a one-sided timing inequality that can always be satisfied

- ***It is possible to design XQDI circuits with only two types of one-sided timing inequalities that can always be satisfied by adding inverters.***

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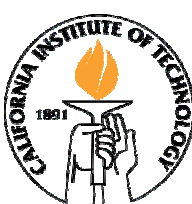
1891


CALIFORNIA INSTITUTE OF TECHNOLOGY
1891

Dual-rail Precharge Function

- $en \wedge F1 \rightarrow zt\_ \downarrow$
  $\neg en \rightarrow zt\_ \uparrow$
  $en \wedge F2 \rightarrow zf\_ \downarrow$
  $\neg en \rightarrow zf\_ \uparrow$

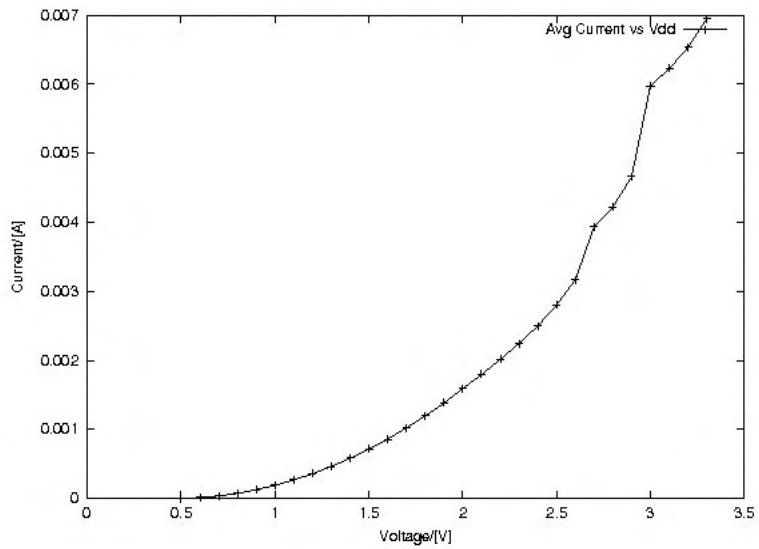
- Floating states : $en \wedge \neg F1$ and $en \wedge \neg F2$
- If we can guarantee that: $en \Rightarrow (F1 \vee F2)$, then in the floating state $en \wedge \neg F1$, $\neg zf\_$ holds, and in the floating state $en \wedge \neg F2$, $\neg zt\_$ holds. Which leads to the simple transformation:

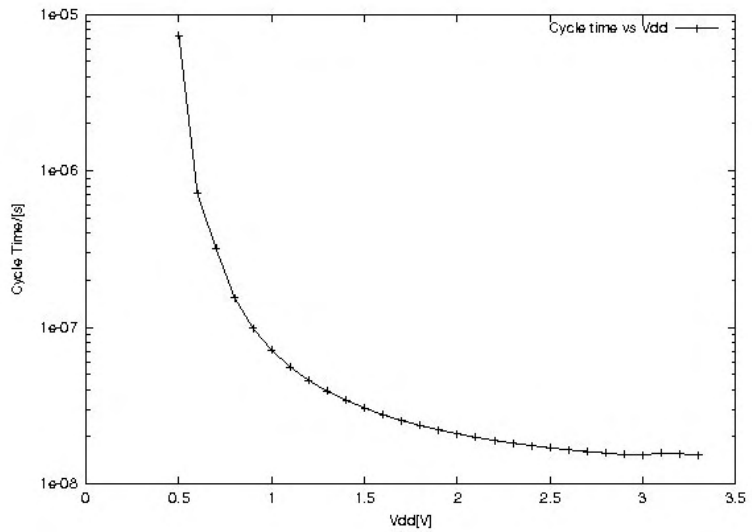
- $en \wedge F1 \rightarrow zt\_ \downarrow$
- $\neg en \vee \neg zf\_ \rightarrow zt\_ \uparrow$

$en \wedge F2 \rightarrow zf\_ \downarrow$
$\neg en \vee \neg zt \rightarrow zf\_ \uparrow$

MiniMIPS Low-Voltage Operation

- Functional from 0.5V Vdd up
- Functional at 0.4V with some transistor resizing

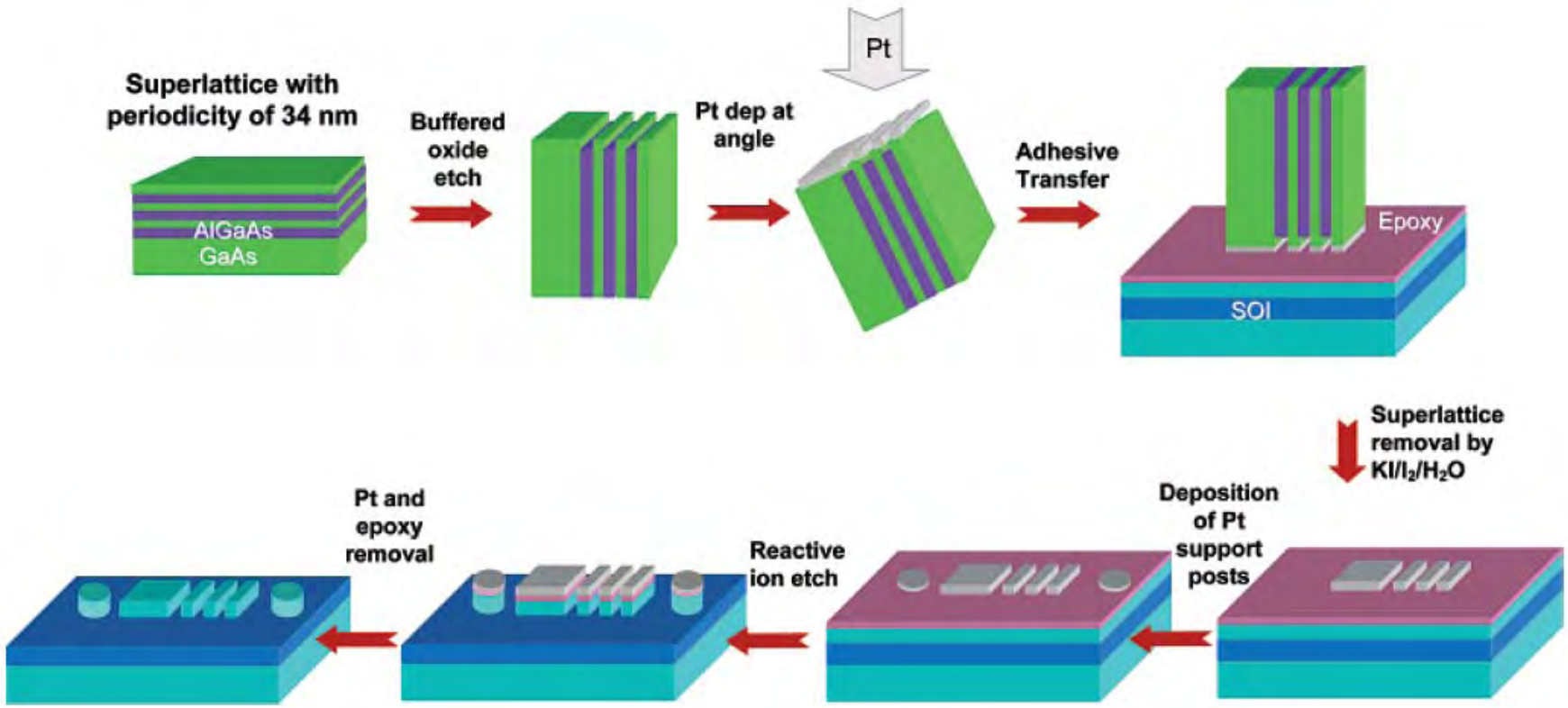




PROGRAMMABLE JUNCTION

From Luo, Chem Phys Chem 2002

Nano-Imprint



SNAP process procedure for transferring nanoscale features from a cleaved superlattice to a flat substrate.

Nanoletters 2006, Jung et al.

Self-Assembly

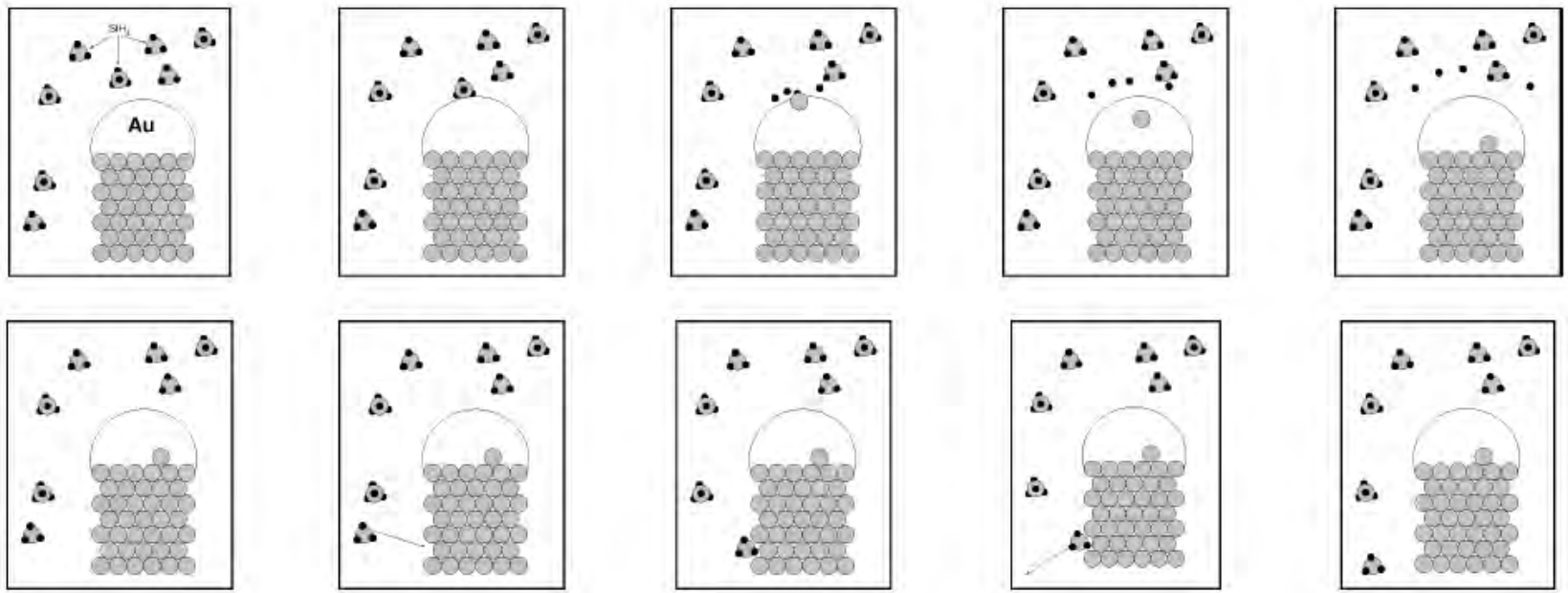
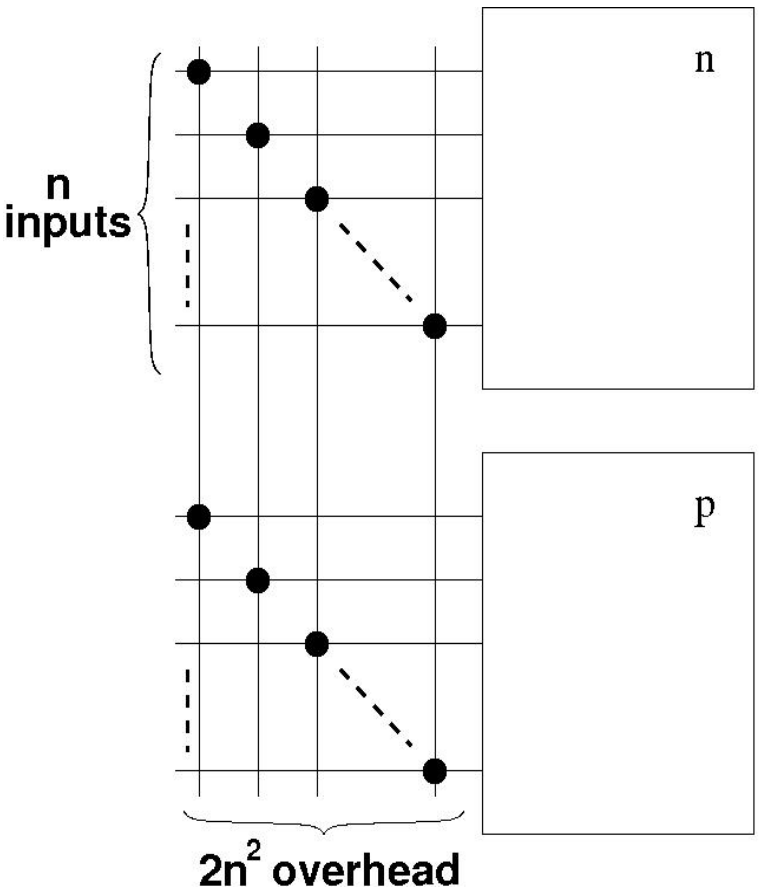
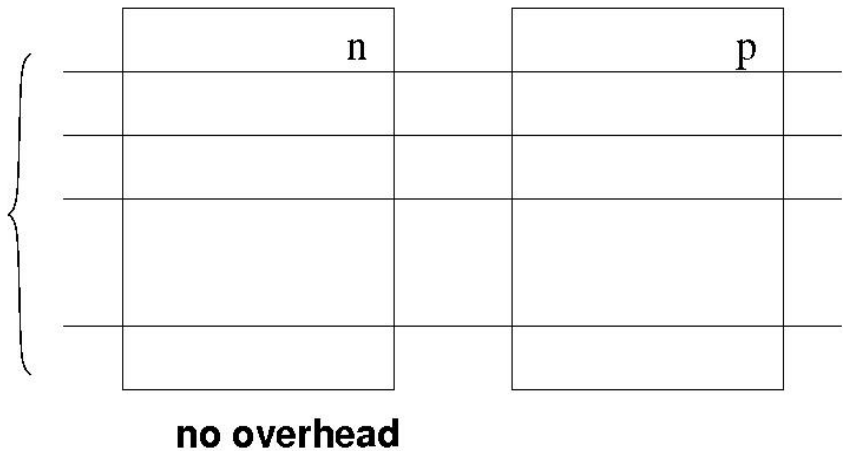


Fig. 1. SiNW growth cartoon. Top row shows how a gold (Au) catalyst allows the SiH_4 molecules to shed their Hydrogen termination so the Silicon can assemble onto the top of the growing NW. Bottom row shows how the Hydrogen termination on the SiH_4 molecule prevents it from assembling onto the edge of the growing NW where the catalyst is not present.

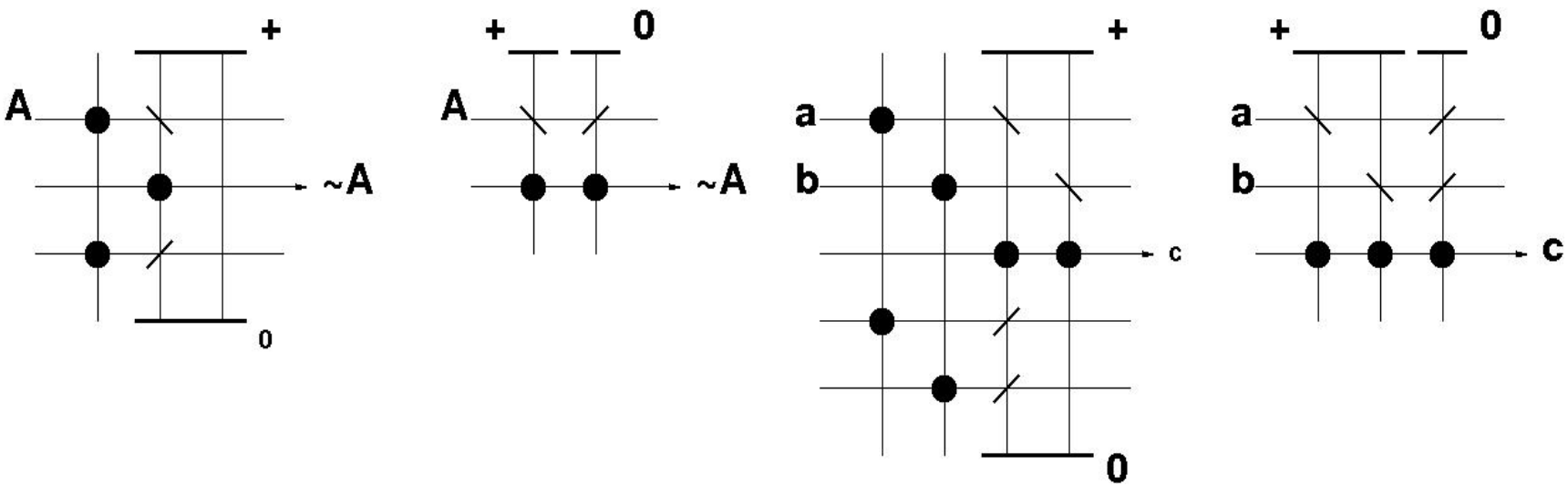
From DeHon, JETC, 2005

Two possible layouts for multiple-input cell





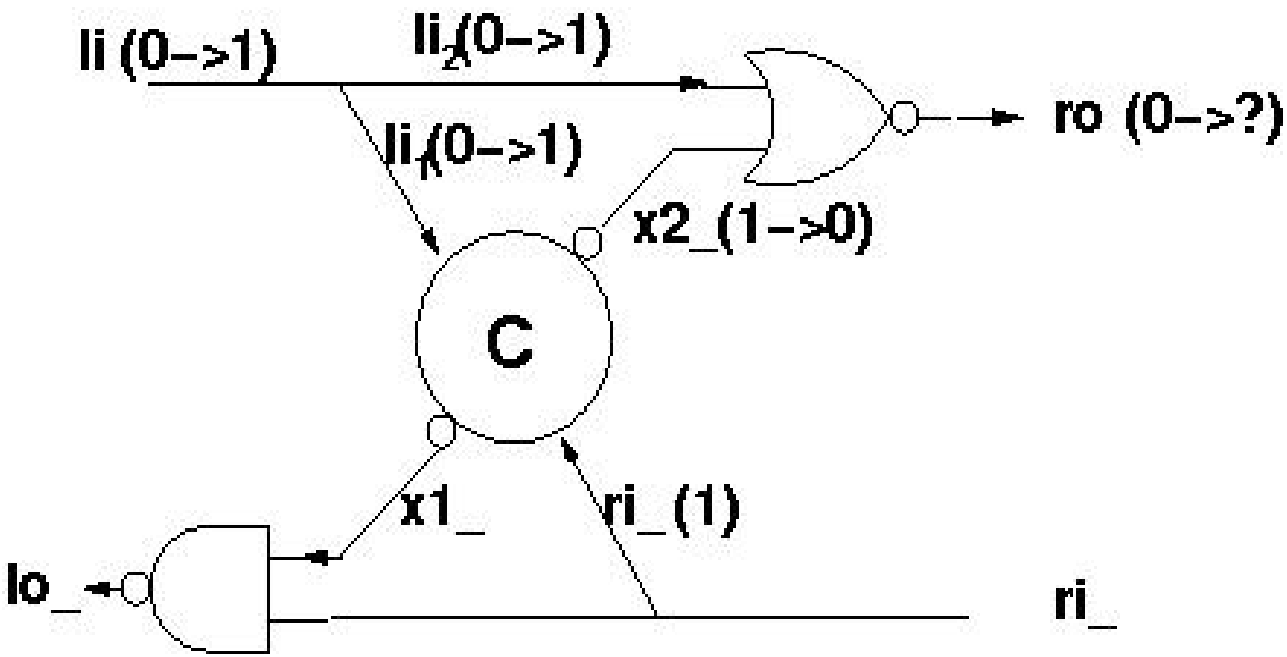
Nano layouts for inverter and 2-input nand-gate



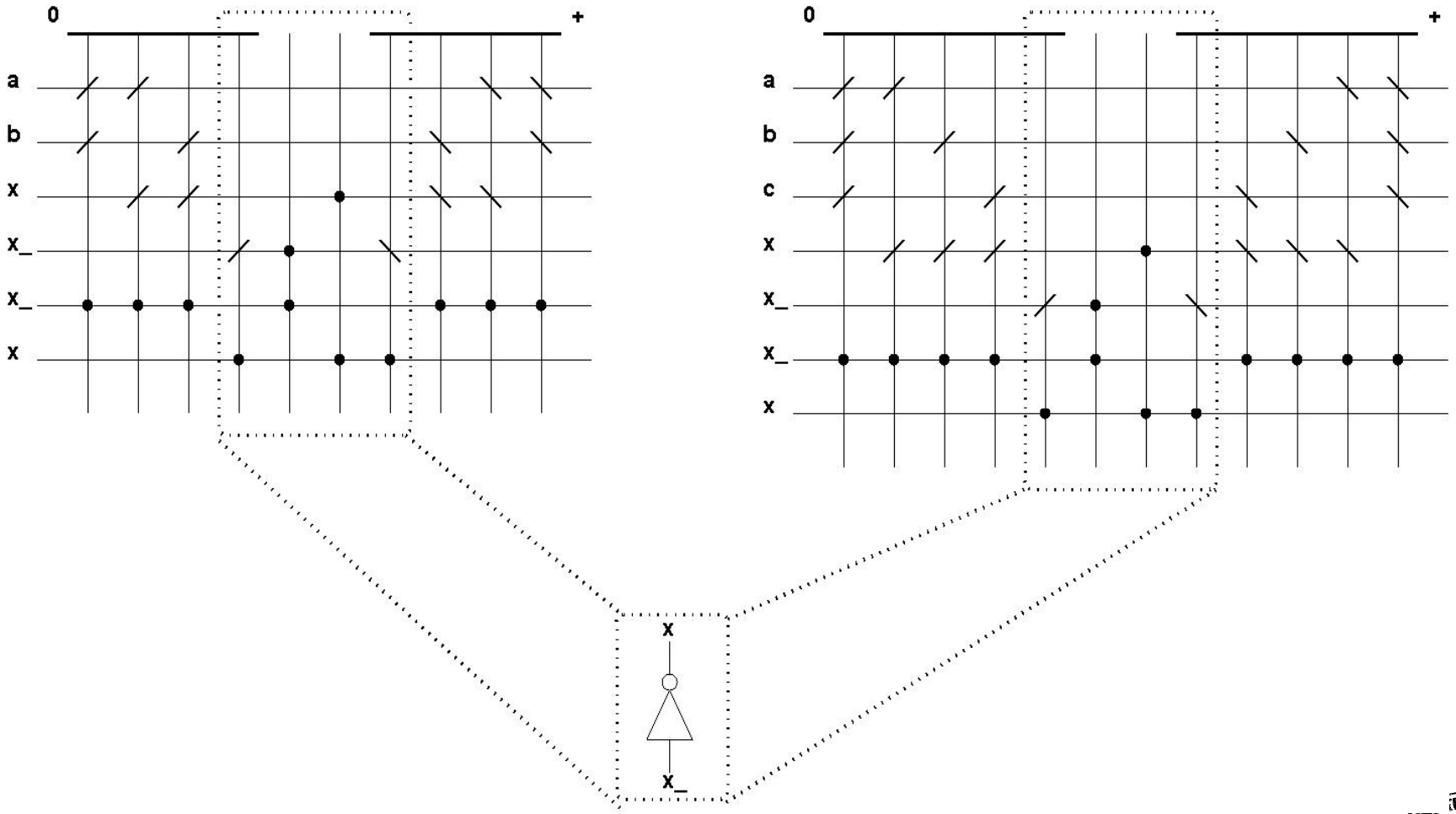
Isochronic Fork Example

Worst-case example! In CMOS: d(single transition)<< 3*d(gate)

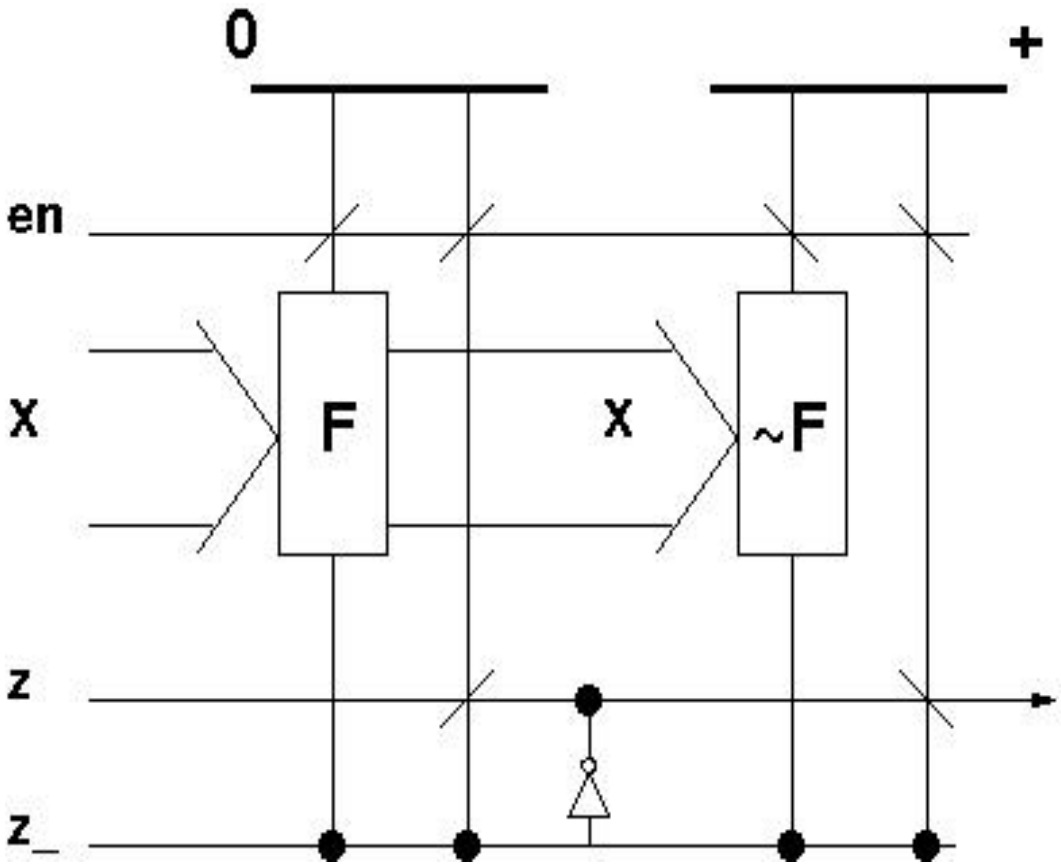
li+; (li1+,li2+); (x1_-, x2_-); lo+; li-; (li1-,li2-); ro+; ri_-; x1_+, x2_+; ro-; ri_+; lo-



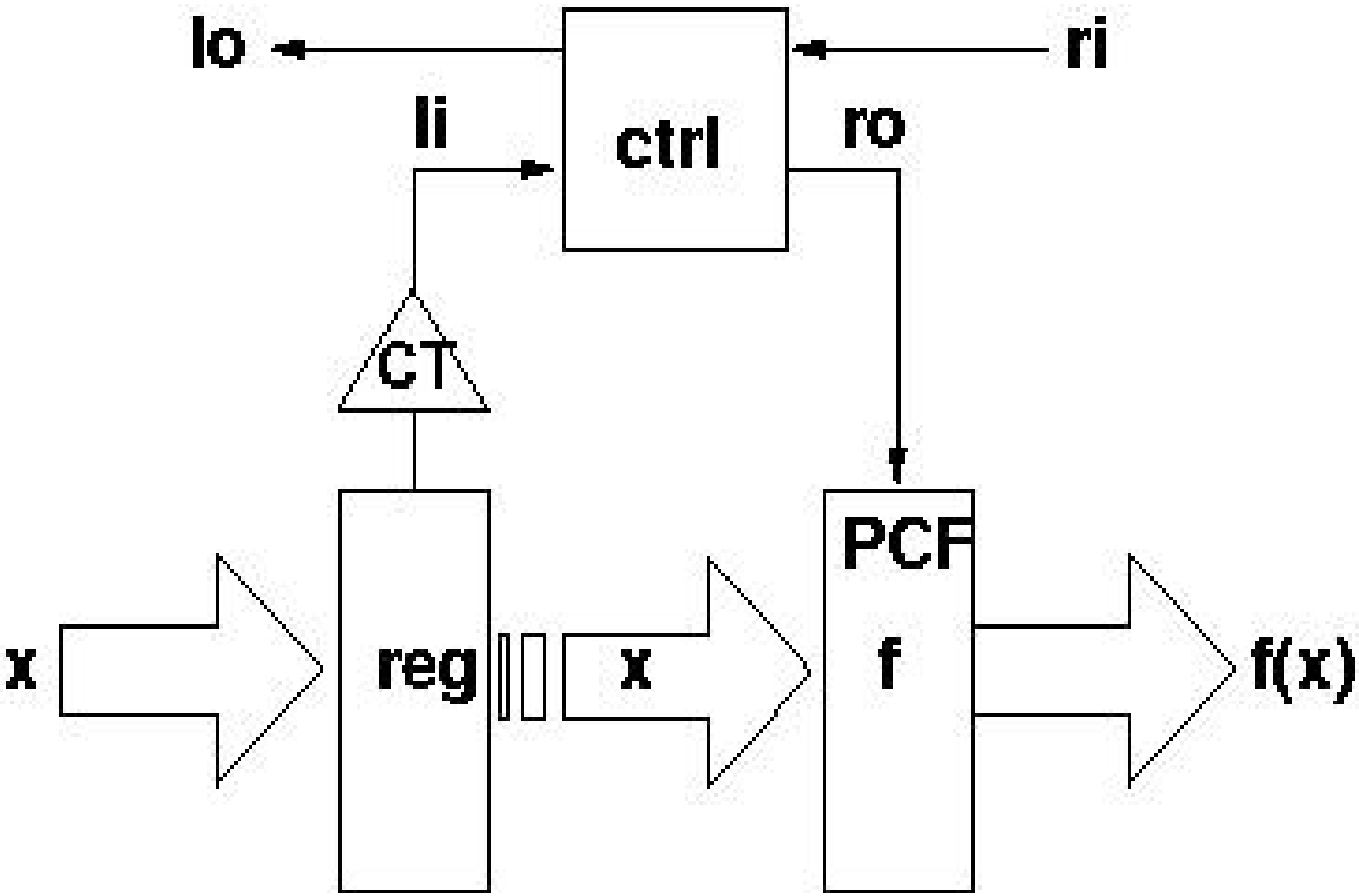
Layout of 2 and 3 input C-elements



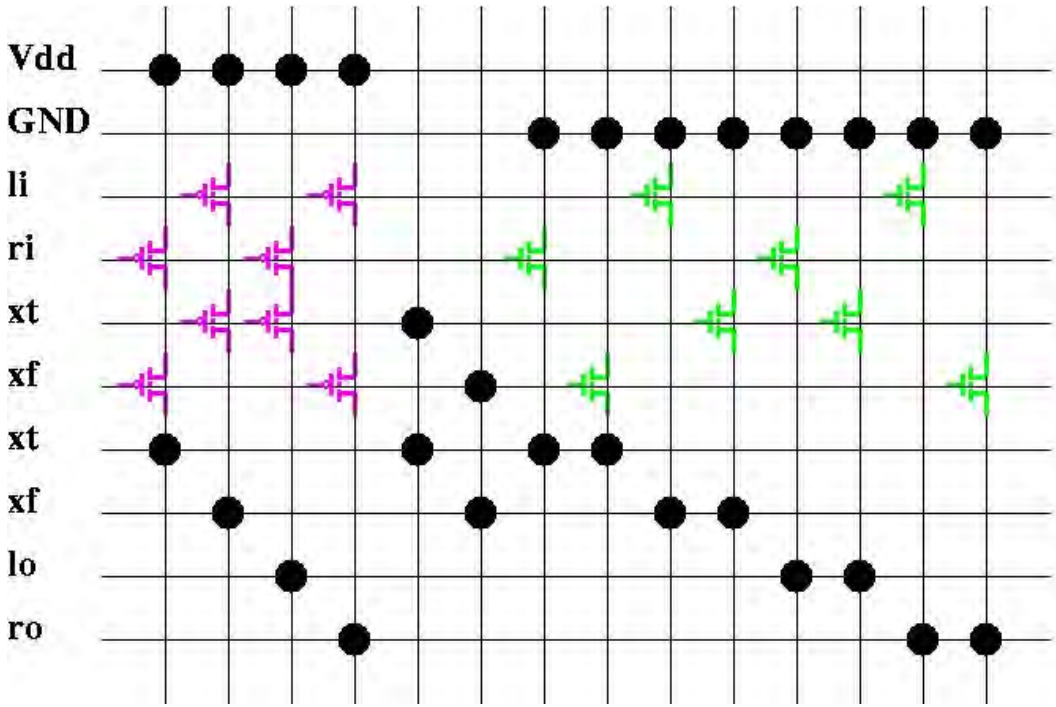
Function Block with single output

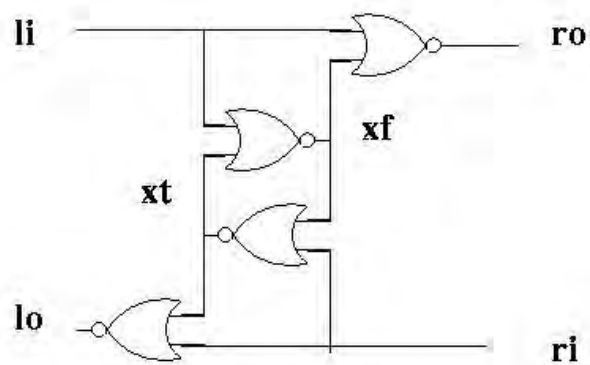


Complete Pipeline Stage

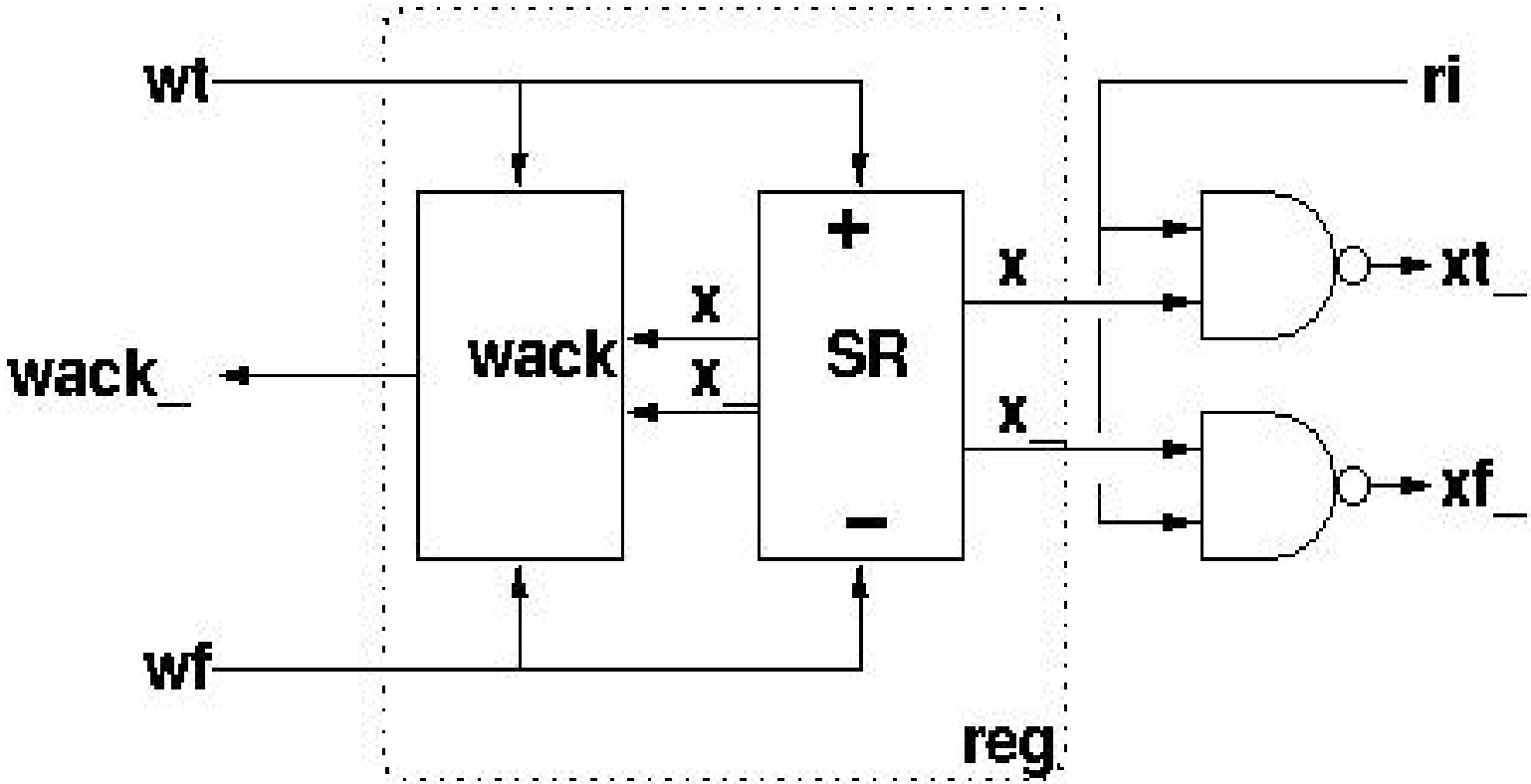


Two-port/Four-phase Sequencer



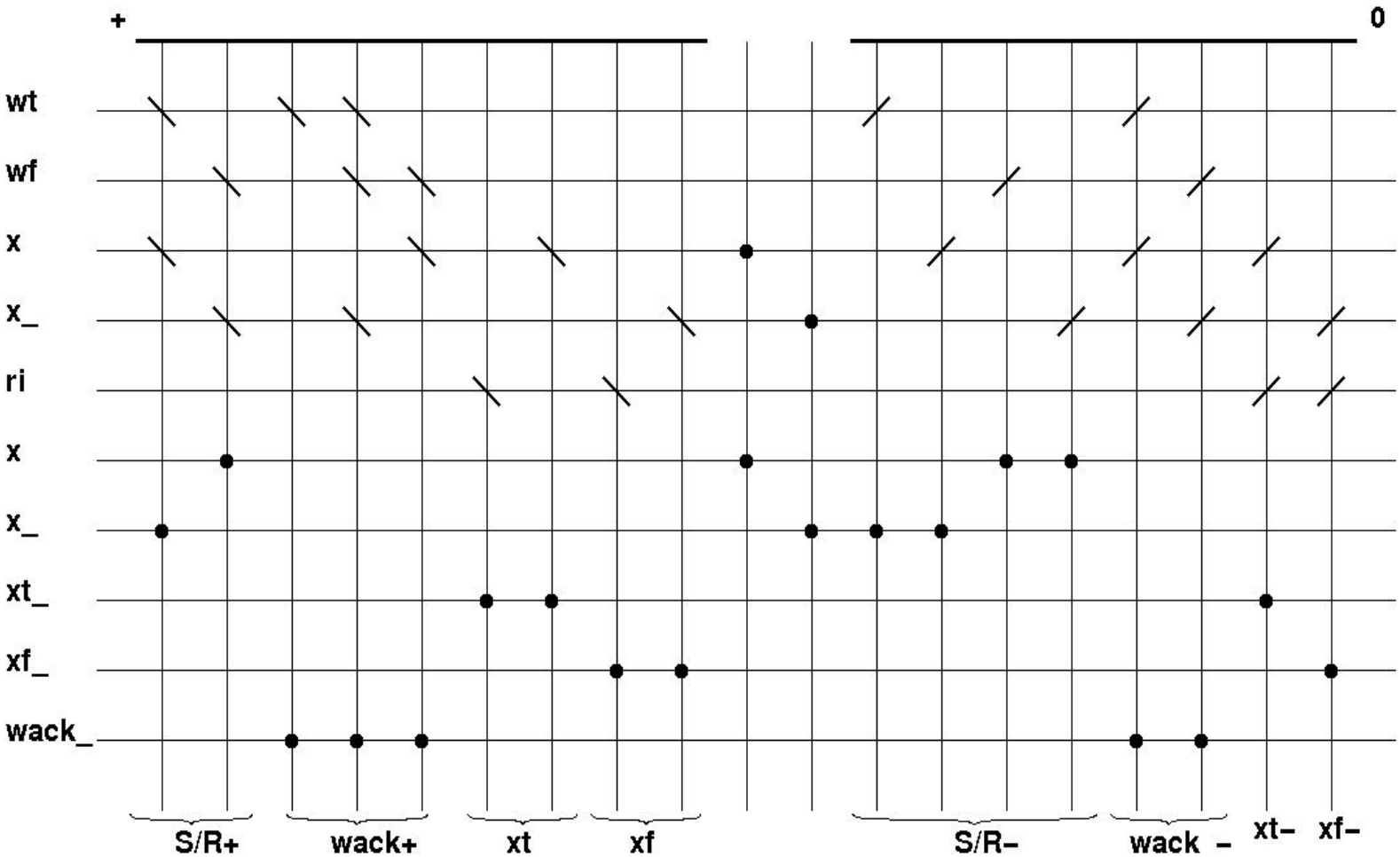


Read/write Boolean Register



(Only combinational gates as building blocks)

Register Nano-Layout



Sum Computation: Example of Function Block