Asynchronous circuit technology is on the market
Overview

- Introduction
  - Handshake Solutions
  - Handshake Technology

- Counting asynchronous millionaires

- More metrics
  - # trained people
  - # competition
  - # asynchronous circuits on the market
Introduction
Handshake Solutions

- Started as research project in Philips Research in 1986 (Tangram)

- Technology and tools used by Philips Semiconductors for products since 1995

- Line of Business of Philips Technology Incubator since January 1st 2004
  - License technology and offer products to parties both inside and outside Philips
  - Grow business
  - Form strategic partnerships
  - Spin-out planned
Solution ingredients: TiDE

Timeless Design Environment

- TiDE is a frontend to your existing EDA flow
- TiDE is *complementary to* and *compatible with* third-party EDA tools
- High-level design entry (Haste)
- Standard-cell hand-over
- Scan-test-based Design-for-Test
- FPGA prototyping through synchronous preview of design
- Integrated support for placement and routing, logic optimization and timing sign-off
Solution ingredients: IP blocks

- Bringing the advantages of Handshake Technology into standard IP blocks

- Microcontrollers and processors
  - HT80C51
  - HT80C51MX
  - ARM996HS

- Peripheral blocks
  - DES, 3DES
  - Timers

- Interface blocks
  - HTmAHB
    - multi-layer AHB bus
  - SPI, IIC
  - UART
Solution ingredients: services

- Architectural consultancy
- Training
- Design support
- Design service
- Design reviews

- We can redesign your microcontroller as an IP block (as we did for 80C51)

- We can develop a product on your specification (as we did for display drivers)
Technology benefits

Handshake ARM996HS

Clock-gated ARM968E-S

Power  Current peaks  Emission
Market proven

- More than 300 million ICs with Handshake Technology sold
- 25+ market-tested products
- Proven by many years of use in design projects
- Applications in:
  - Smartcards
  - Automotive
  - Wireless connectivity
Counting asynchronous millionaires
Kevin Normoyle – Fear and Greed
Where are the asynchronous millionaires?

- **Fear** - “The competition will have something you don’t”

- **Greed** - “That you might be able to do something the competition can’t”

- “Synchronous everywhere is not the solution. But it’s not the broken solution that it’s sometimes made out to be.”
  “Don’t change until it breaks. Power is broken. EMI is not broken yet. Performance is broken.”

- “The issues with using Async technologies are complicated enough that the motivator has to be a big bang. Not incremental goodness.”
Other fears

- Fear of change
  - Disruptive technology (new language, new tools, ...)
  - Prove it in our technology
  - Prove it for our application domain
  - Power, emission, currents peaks are important but typically #2 unless they are broken
  - Cost of change (e.g. legacy code)

- Fear of leading
  - Following competition vs. trying to lead
  - Use proven technologies like clock gating, voltage scaling, etc.

- Most popular FAQ
  - Will I need to completely re-tool my business?
  - How is designing with TiDE different from what I’m used to?
  - Do you support Design for Test, Signal Integrity?
  - Is it true that clockless ICs are larger than clocked ones?
  - Does the whole design have to be done in the TiDE flow?
  - Can HS’ tools translate a clocked design into a HT design?
  - Is Handshake Technology already being used?
More metrics
Goodness metrics on the road to commercial success

- Steps we are taking
  - educating people
    - Academic program
    - Handshake Technology Courses
  - improving our image together with competition
  - improving our image together with partners
  - providing customers with a complete solution
  - developing and converting leads
    - Trade shows, conferences, road shows, customer visits
  - building prove points
    - Evaluations, designs, products
Academic Program and Courses

- **Academic program**
  - Enable academic institutes low cost access to Handshake Solutions design tools and flow (for educational and research purpose)
  - Joint by 15 universities (from Japan, Austria, Singapore, Italy, UK (3*), Finland (2*), Taiwan, Denmark, Israel, Netherlands, France, Canada)
  - Interesting topics (delay fault testing, clockless FPGA mapping, behavioral synthesis, ULP Controllers, ...)

- **Courses followed by >150 persons**
  - Introduction to Handshake Technology
  - Advanced Handshake Technology Backend course
  - Taste of Haste
Asynchronous companies

- **Achronix Semiconductor** ([http://www.achronix.com/](http://www.achronix.com/))
  - Ultra-fast (asynchronous) FPGAs
  - Reliability in high radiation environments and over wide temperature range

- **Elastix** ([http://www.elastix-corp.com](http://www.elastix-corp.com))
  - EDA for enabling variability-aware designs
  - Optimize power-performance trade-offs for 65 nm and beyond
  - Generate asynchronous implementations of synchronous designs automatically

- **Silistix** ([http://www.silistix.com/](http://www.silistix.com/))
  - EDA tools (CHAINworks) for the design and synthesis of customized on-chip interconnect using asynchronous circuits
  - Addressing timing closure, power consumption, and overall design complexity

- **Tiempo** ([www.tiempo-ic.com](http://www.tiempo-ic.com))
  - IPs and EDA tools for the design of clockless ICs
  - Ultra low power consumption, ultra low EME, robustness, reduced time-to-market

- Fulcrum Microsystems, Situs Logic, Camgian Microsystems, FTL Systems, ...
Partners and Eco System

- ARM Ltd.
- IBM Services Company Japan
- Silicon & Software Systems
- Bruco Integrated Circuits
- Seloco Korea
- Accent
- Cadence
- Magma
- Mentor Graphics
- Synopsys
Technology improvements in 2007

- Improved optimizations for area and speed
  - Improved timing handling (matching how synchronous tools constrain for timing)
  - Performance profiling tool (htprof)
  - Faster circuits for our FPGA flow
  - Reduced scan overhead
  - ScanDEF file generation to enable scan-chain reordering

- Providing a fully integrated tool flow
  - Added SystemC modelling of a Haste program
  - Support for additional synchronous tools (e.g. RTL Compiler, ETS, Conformal)
  - Extended layout support (Magma, Cadence, Synopsys)
  - Post-layout ATPG (bridging fault testing, post-production failure analysis)

- Ease of use
  - Increased expressiveness Haste (e.g. dataprobe, repeat until, clocked variables)
  - Easier (test and timing) integration of Haste blocks in larger synchronous designs

- Ready for 65 nm and beyond
  - Delay fault testing
  - Signal integrity (SI) (e.g. support for Celtic)
Lead database

- Lead database chart showing the number of leads and converted leads over time from March 2004 to March 2008.
- Key events:
  - ARM partnership announcement
  - ARM996HS launch

Date:
- March 2004 (Mar-04)
- June 2004 (Jun-04)
- September 2004 (Sep-04)
- December 2004 (Dec-04)
- March 2005 (Mar-05)
- June 2005 (Jun-05)
- September 2005 (Sep-05)
- December 2005 (Dec-05)
- March 2006 (Mar-06)
- June 2006 (Jun-06)
- September 2006 (Sep-06)
- December 2006 (Dec-06)
- March 2007 (Mar-07)
- June 2007 (Jun-07)
- September 2007 (Sep-07)
- December 2007 (Dec-07)
- March 2008 (Mar-08)
Asynchronous circuit technology is on the market
Smart card controllers
Products and derivatives

Energy efficiency enables high performance in contactless operation and extra non-volatile memory

- More than 80% of the world’s smart passports
- Access control at NASA
- Nokia’s 6131 NFC phone
Automotive MEMS
Lowest power 8051

Ultra low power HT80C51 maximizes battery life and enables seamless integration with analog, RF, and on-chip memories.
Flexible active radio
Challenge: 8051 running on flexible battery

Low peak current of HT80C51 enables radio operation from flexible battery

Budget was 1mA Chip runs at 0.5mA

Thin & flexible radio node

Flexible battery

Flexible substrate

Fully integrated transceiver + HT80C51

Printed antenna

Quartz Xtal
Automatic adaptation
8051 performance adapts to voltage
## Reed-Solomon decoder

<table>
<thead>
<tr>
<th></th>
<th>Synchronous</th>
<th>Handshake</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lines of Code</td>
<td>9750 RTL VHDL</td>
<td>780 Haste</td>
</tr>
<tr>
<td>Silicon area</td>
<td>2.78 mm²</td>
<td>0.83 mm²</td>
</tr>
<tr>
<td>Power</td>
<td>13 mW (at 0 errors)</td>
<td>2.1 mW (average)</td>
</tr>
<tr>
<td>Energy</td>
<td></td>
<td>1.0 µJ - 0 errors</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11.1 µJ - 1 error</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11.7 µJ - 32 errors</td>
</tr>
<tr>
<td>Peak power</td>
<td>12 mW</td>
<td></td>
</tr>
<tr>
<td>(all packets have max (32) errors)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Average power</td>
<td>2.1 mW</td>
<td></td>
</tr>
<tr>
<td>(90% correct, 10%/32 errors)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
# Viterbi decoder

## Summary of findings

<table>
<thead>
<tr>
<th>Metric</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
<td>D1: 18-83% saved, D2: 16-82% saved</td>
</tr>
<tr>
<td>Performance</td>
<td>D1: 175MHz, D2: 130MHz</td>
</tr>
<tr>
<td>Area</td>
<td>13-18% saved versus sync</td>
</tr>
<tr>
<td>Test coverage</td>
<td>&gt;99% stuck at</td>
</tr>
<tr>
<td>Design time</td>
<td>5-10% saved vs sync</td>
</tr>
<tr>
<td>Code size (bytes, lines of code)</td>
<td>&lt;30% of sync</td>
</tr>
</tbody>
</table>
**Viterbi decoder**

**Power analysis details**

<table>
<thead>
<tr>
<th>Condition</th>
<th>Synchronous</th>
<th>Handshake</th>
</tr>
</thead>
<tbody>
<tr>
<td>Idle with clock (leakage is included = 7.4uW)</td>
<td>50 uW</td>
<td>9 uW = -82%</td>
</tr>
<tr>
<td>Energy per bit for 16/64/256 states [nJ]</td>
<td>0.25/- /2.28</td>
<td>0.22/0.69/2.3</td>
</tr>
<tr>
<td>Average power for 1 block 64 states</td>
<td>67.4 uW</td>
<td>26.4 uW = -61%</td>
</tr>
<tr>
<td>Average power for 2*6 blocks 64 states</td>
<td>259 uW</td>
<td>218 uW = -16%</td>
</tr>
</tbody>
</table>
Bluetooth radio
Problem: interference to analog/RF

- RFCMOS radio consists of two main parts
  - one digital section and one analog RF
- The clocks in the radio digital can be seen on the supply
- The clocks in the BT digital unacceptably degrade the performance of the FM receiver
Bluetooth radio
Analysis: demodulator dominant

- Demodulator accounts for:
  - > 70% total complexity
  - > 80% total power dissipation (in Rx)
- Both energy consumption and current peaks should be reduced
- Asynchronous pipeline will spread out activity over time
Bluetooth radio
Results: reduced current peaks

Reference synchronous design
Asynchronous design
Bluetooth radio
Results: reduced interference

Reference synchronous design

Asynchronous design
## Bluetooth radio
### Results: summary

- Digital noise reduction is significant (main target)
- Area needs further optimization

<table>
<thead>
<tr>
<th></th>
<th>Synchronous</th>
<th>Handshake</th>
<th>Delta</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peaks (48+ M)</td>
<td>25</td>
<td>5</td>
<td>- 80%</td>
</tr>
<tr>
<td>Power</td>
<td>28.6 mW</td>
<td>27.2 mW</td>
<td>- 5%</td>
</tr>
<tr>
<td>Area</td>
<td>0.94 mm²</td>
<td>1.14 mm²</td>
<td>+ 21%</td>
</tr>
</tbody>
</table>
Pipelined DSP applications

- This has not been the primary target for Handshake Technology …
  - Activation of datapath in pipelines is data-driven
  - Activation of registers is typically data-independent
  - Energy consumed per data-sample passing through pipeline more or less independent of how these registers are clocked

- … still we have encountered a lot of interest from this domain
  - Different frequencies per stage complicate clock distribution
  - Clock distribution getting more complicated (more energy) in smaller geometries
  - Clock signals lead to interference with RF/analog at chip/system level
Audio processing

- Design competition from specification in Simulink
  - Synchronous: creation of RTL Verilog and clock-gating
  - Asynchronous: creation of Haste from scratch

<table>
<thead>
<tr>
<th></th>
<th>Synchronous</th>
<th>Asynchronous</th>
<th>Effort</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area pre-routed</td>
<td>333,583 geq</td>
<td>383,070 geq</td>
<td>cts to be done</td>
</tr>
<tr>
<td>Area post-layout</td>
<td>465,630 geq</td>
<td>502,200 geq</td>
<td>&lt; 8% overhead</td>
</tr>
<tr>
<td>Power</td>
<td>6.98 mW</td>
<td>1.37mW</td>
<td>&gt; 70% saving</td>
</tr>
<tr>
<td>Effort</td>
<td>8pm</td>
<td>3pm</td>
<td>&gt; 2x gained</td>
</tr>
</tbody>
</table>
More information

If you would like more info on:
– HT80C51/MX
– Design Tools (TiDE)
– Haste (Language Manual)
– Academic program
– Job opportunities
– ...

Visit our web site: www.handshakesolutions.com,
or contact me: arjan.bink@handshakesolutions.com
Handshake Solutions

Thank You

www.handshakesolutions.com