Low Power and Reliable Interconnection with Self-Corrected Green Coding Scheme for Network-on-Chip

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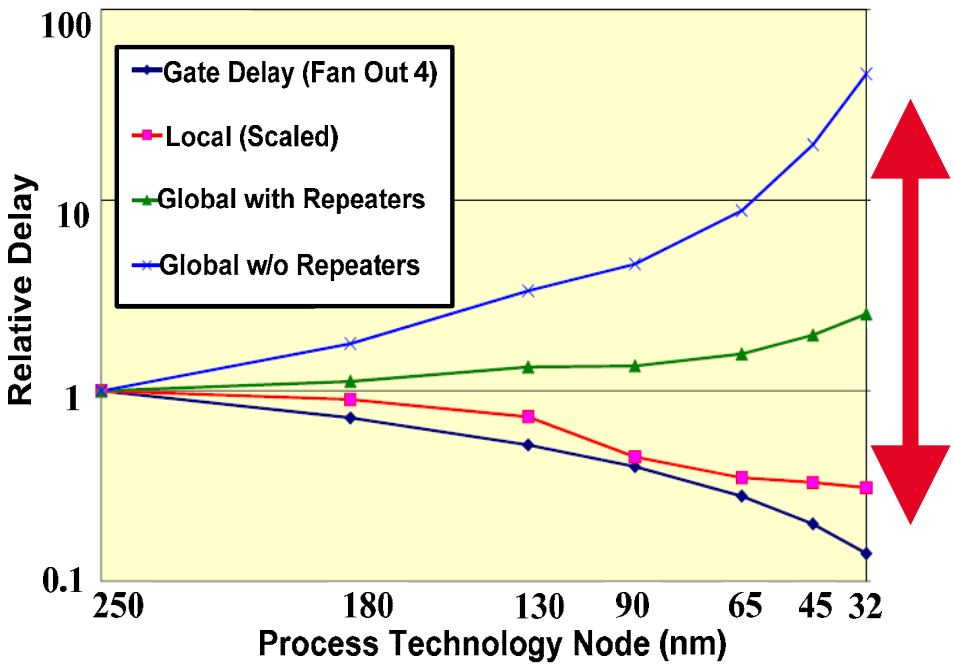
Outline

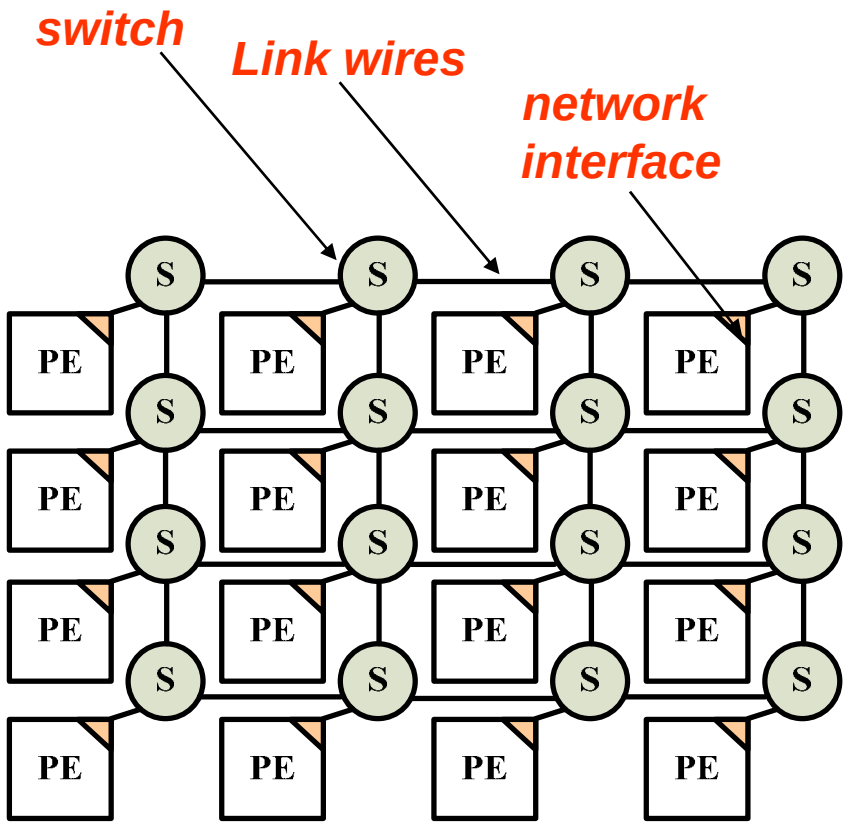
- Introduction
- Low power joint bus/error correction coding concept
- Self-corrected green coding scheme
  - Triplication error correction coding stage
  - Green bus coding stage
- Simulation Results
- Conclusions

Motivation

- Network-on-chip : an effective solution to integrate multi-core system and a process independent interconnection architecture.



Physical design of NoC



Introduction

- Three critical issues for on-chip communication
  - Delay – coupling capacitances
  - Power – parasitic and coupling capacitances
  - Reliability – degrading due to noises
- Novel design techniques are proposed to overcome the crosstalk effect and further provides a reliability bound for on-chip interconnection.
  - Joint bus and error correction coding schemes

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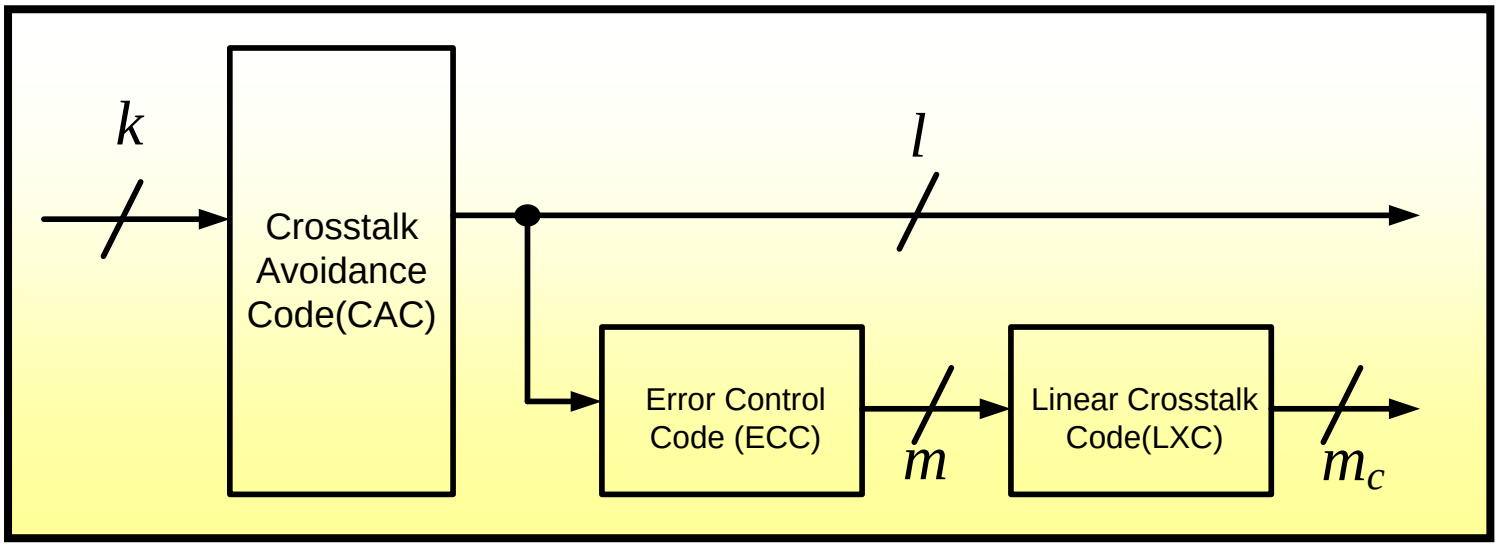
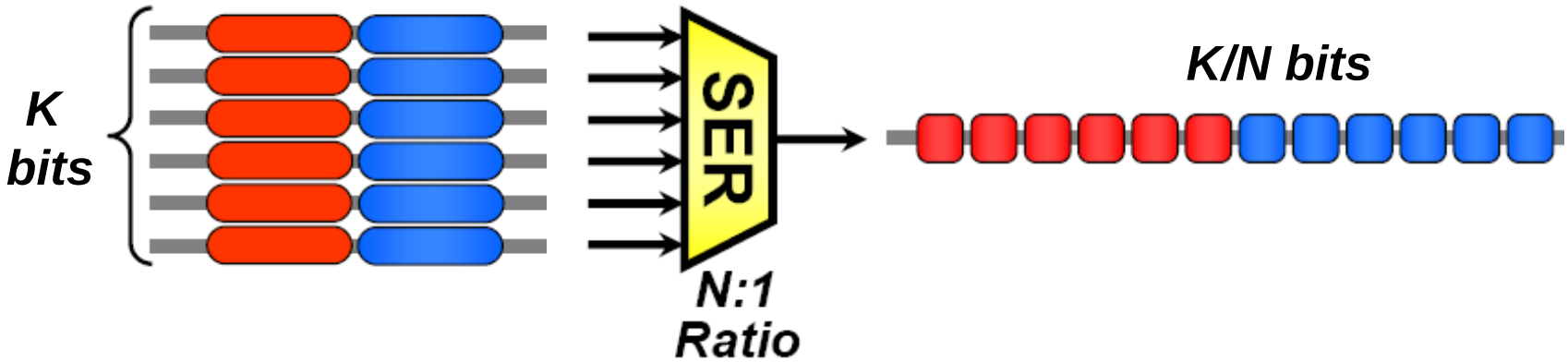
A unified framework of coding in SoC



- Crosstalk avoidance codes (CAC)
  - Avoid specific code patterns or code transitions to reduce delay and power dissipation.
- Error control codes (ECC)
  - Detect and correct the error bits
- Linear crosstalk code (LXC)
  - Shielding link wires, duplicated bits

Serialization technique for link wires

K-to-N serialization



physical transfer unit (phit)

the data which is divided and transmitted through micro-network

Area Cost ↓ ($1/N^2$) → Switch delay ↓

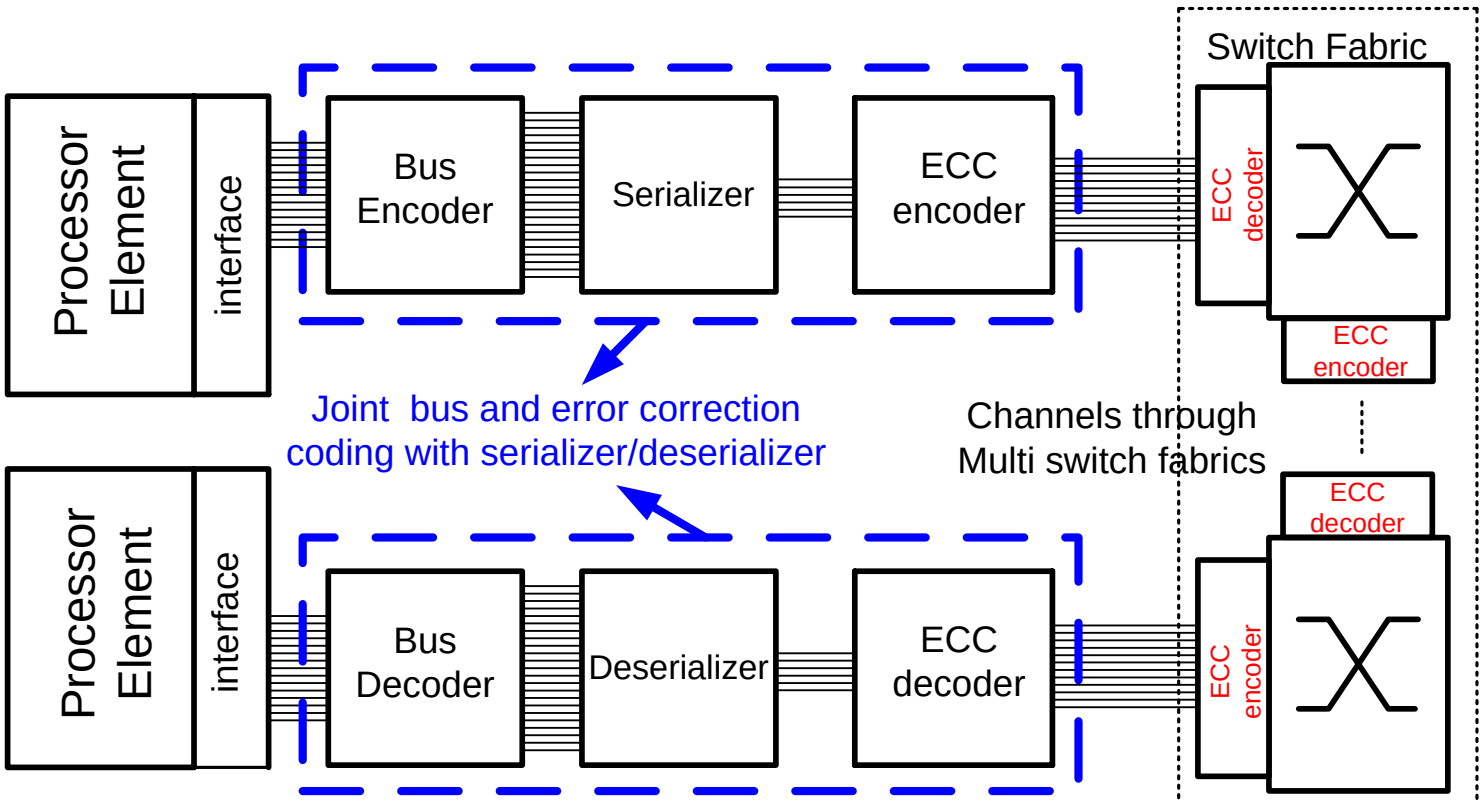
Crosstalk ↓ , signal-to signal skew ↓

Signaling Rate ↑

-> predefined well-structured link

Self-corrected green coding scheme

- Self-corrected green coding scheme
  - triplication error correction coding stage, green bus coding stage
  - Shorter delay for ECC, more energy reduction and smaller area



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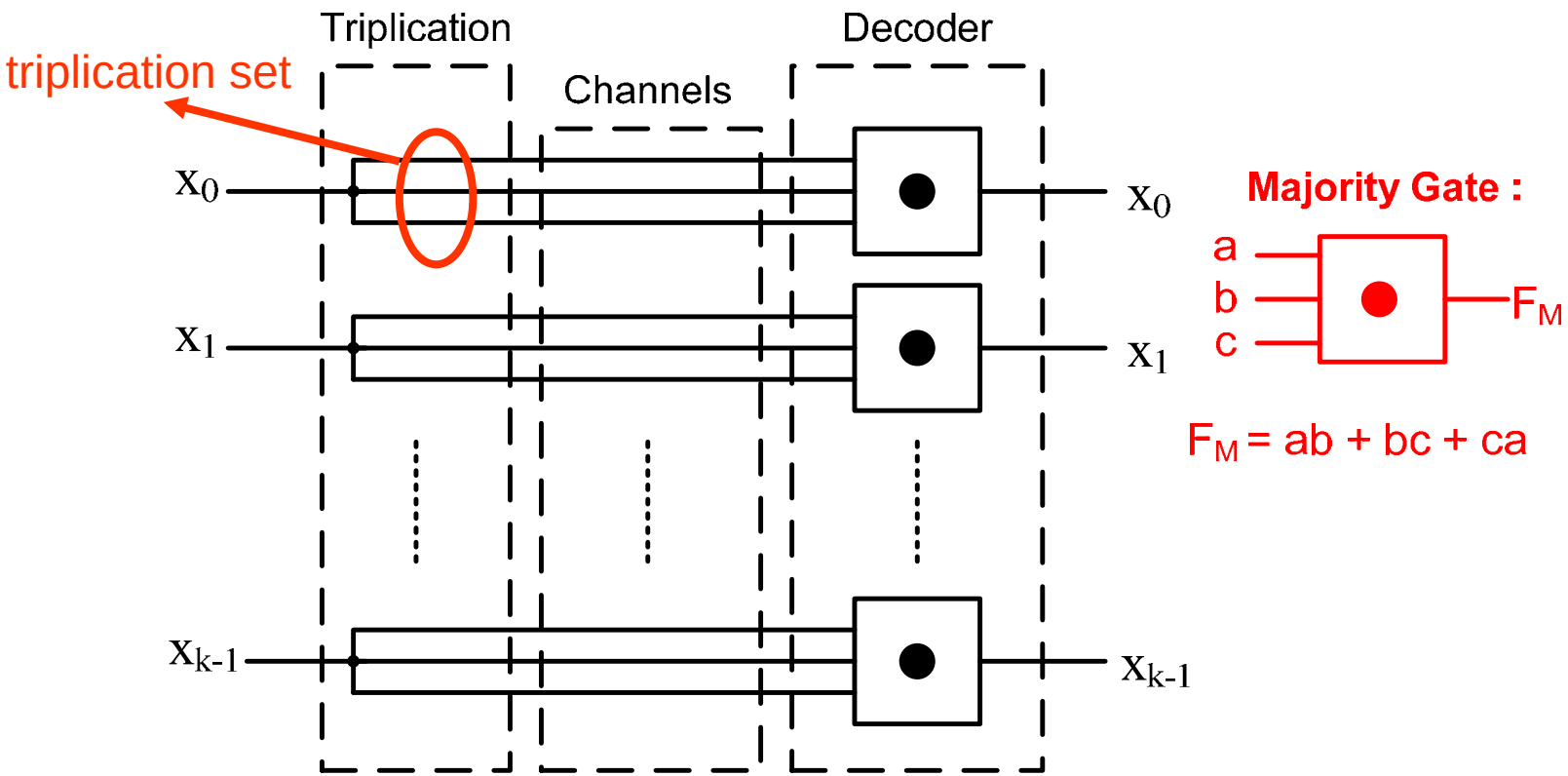
Triplication error correction coding stage



- The hamming distance of each set is equal to 3.
- A constant delay of a majority gate and much smaller than others
- Rapid correction ability by self-corrected mechanism in bit-level.

Word error probability of triplication

- Error correction mechanisms
  - Reducing supply voltage of channels without compromising the reliability of system.
- A Gaussian distributed noise voltage V_N with variance σ_N^2 is added to the signal waveform.

$$\varepsilon = Q\left(\frac{V_{dd}}{2\sigma_n}\right) \quad , \quad Q(x) = \frac{1}{\sqrt{2\pi}} \int_x^{\infty} e^{-\frac{y^2}{2}} dy$$

Word-error probability : $P_{\text{triplication}} \approx 3k\varepsilon^2 - 2k\varepsilon^3$

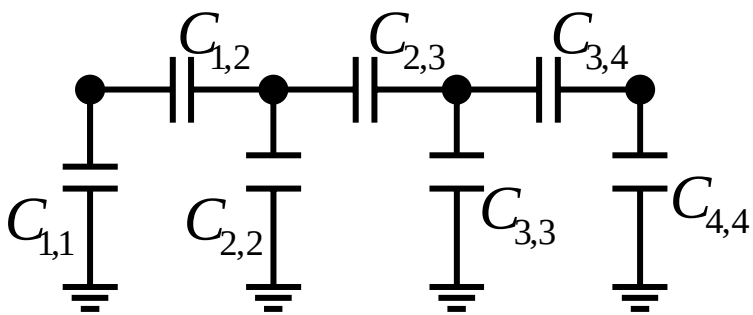
where k : the size of bit-width

ε : bit-error probability

Green Bus Coding Stage

- Green bus coding stage
  - Reducing coupling effect

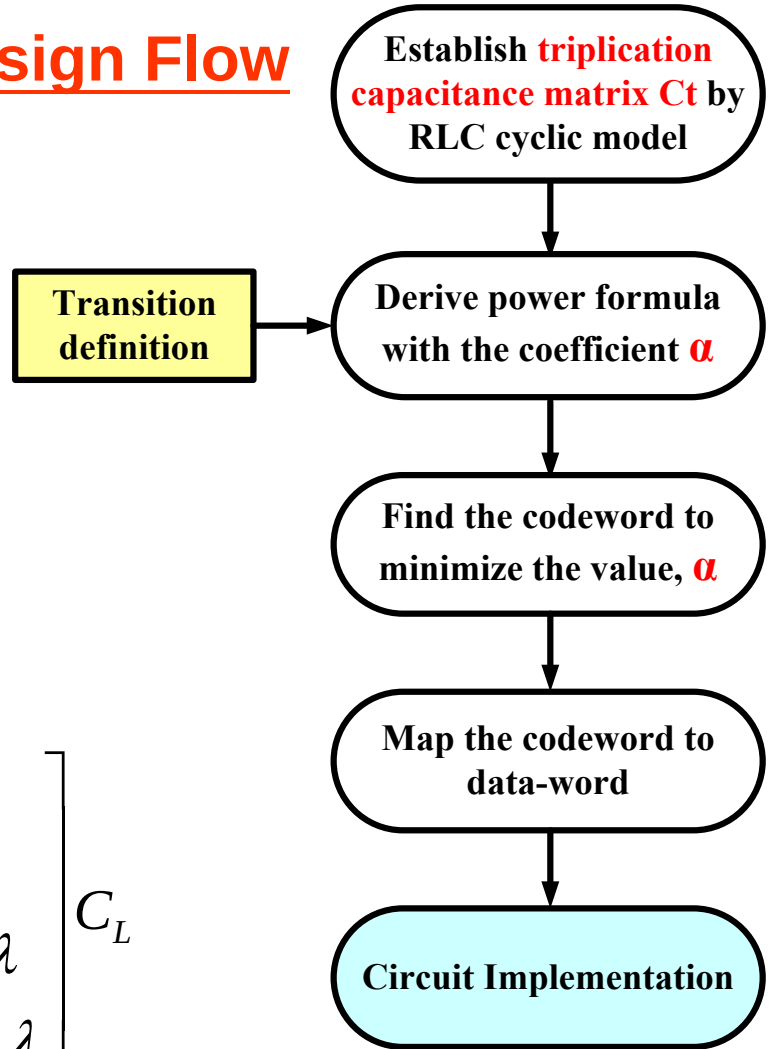
Approximate Cyclic model



Triplication capacitance matrix

$$\lambda = \frac{C_X}{C_L}, \quad C^t = \begin{bmatrix} 3+\lambda & -\lambda & 0 & 0 \\ -\lambda & 3+\lambda & -\lambda & 0 \\ 0 & -\lambda & 3+\lambda & -\lambda \\ 0 & 0 & -\lambda & 3+\lambda \end{bmatrix} C_L$$

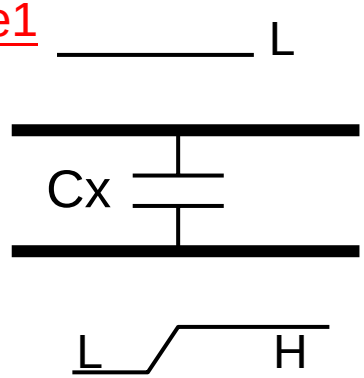
Design Flow



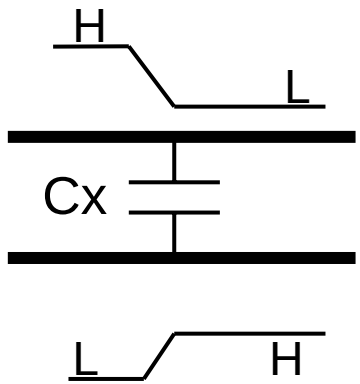
Five types of signal transitions

- Static transitions

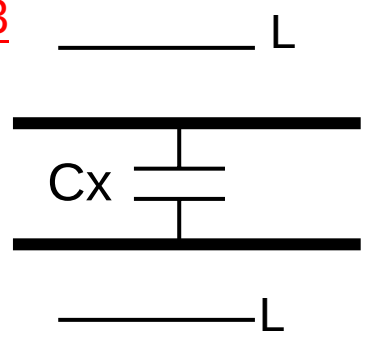
Type1



Type2



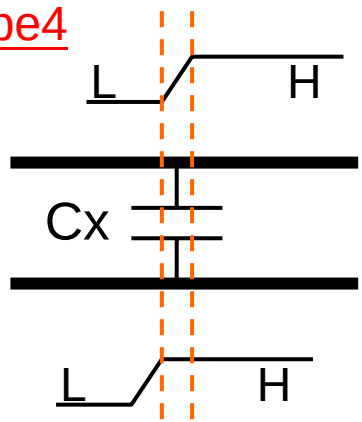
Type3



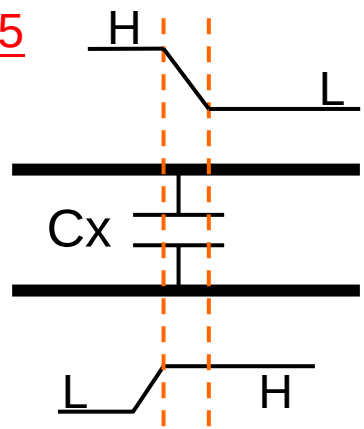
Type3 (no switching or switching in the same direction)

- Dynamic transitions

Type4



Type5



signal aliasing

Triplication Power formula

- The power consumption can be derived as follow.

$$P = f * C_L * V_{DD}^2 * \alpha$$

Type 2,5

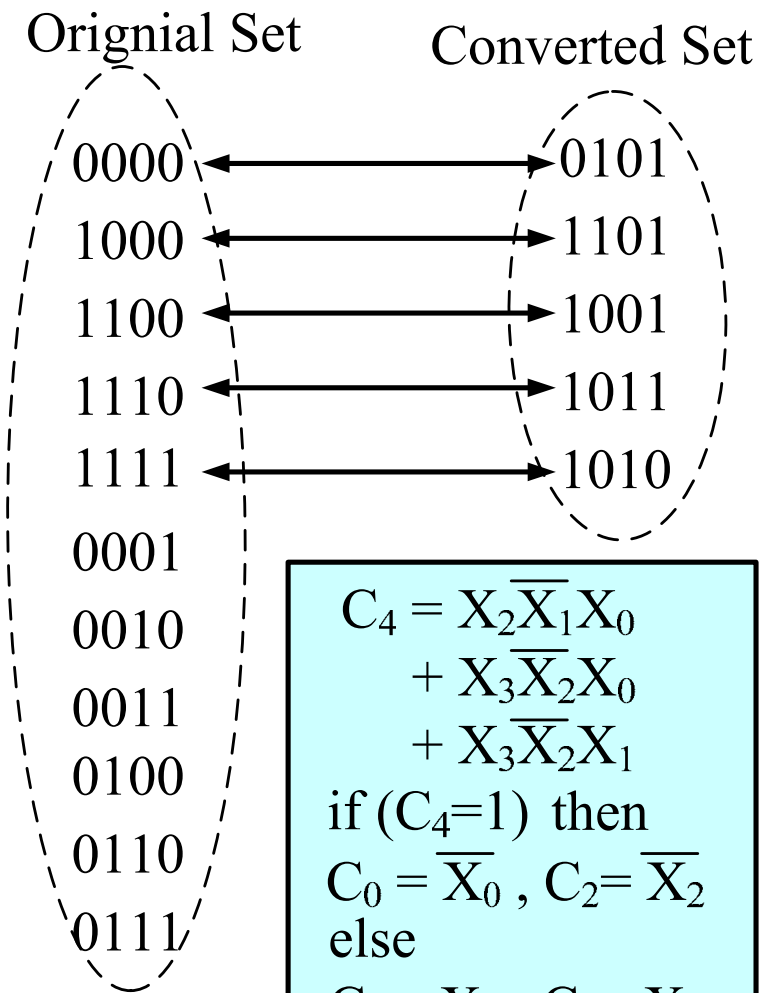
Type 1

$$\alpha = 3(r_1 + r_2 + r_3 + r_4 + r_5) + \lambda\left(r_1 \oplus r_2 + r_2 \oplus r_3 + r_3 \oplus r_4 + r_4 \oplus r_5\right)$$
$$+4\lambda\left(d_{12} + d_{23} + d_{34} + d_{45}\right)$$

α is a modified switching activity with considering coupling capacitances.

- The meaning of $\left(r_i \oplus r_j\right)$ is that only one line is changing between two lines as type 1.
- For the term of $\left(d_{ij}\right)$, it is about the two lines change in the opposite direction as type2 and type5 transitions.

Codeword of green bus coding



$C_4 = X_2\overline{X_1}X_0 + X_3\overline{X_2}X_0 + X_3\overline{X_2}X_1$

if (C_4=1) then

$C_0 = \overline{X_0}$, $C_2 = \overline{X_2}$

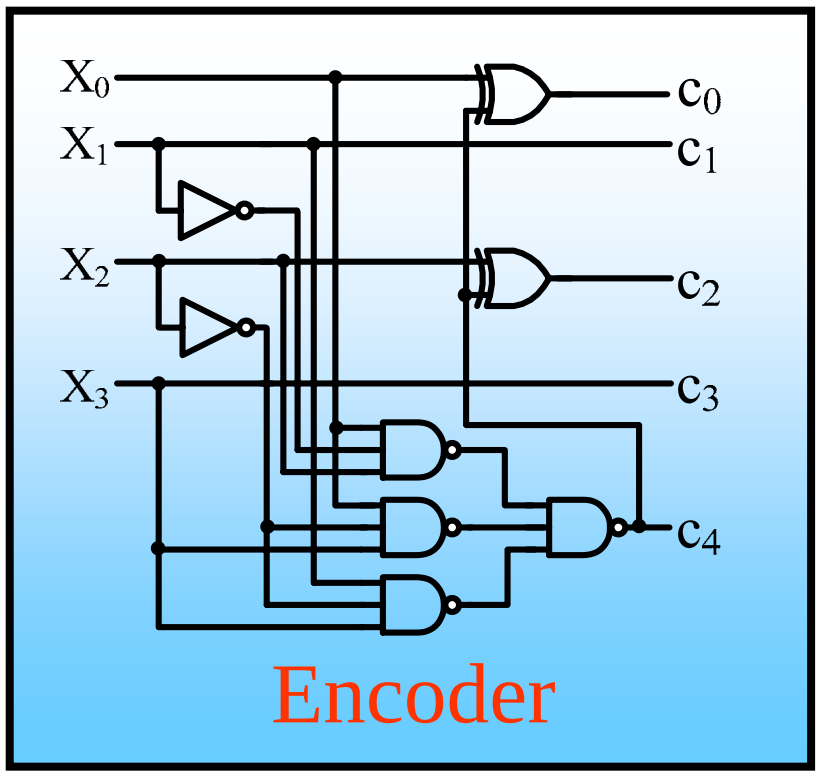
else

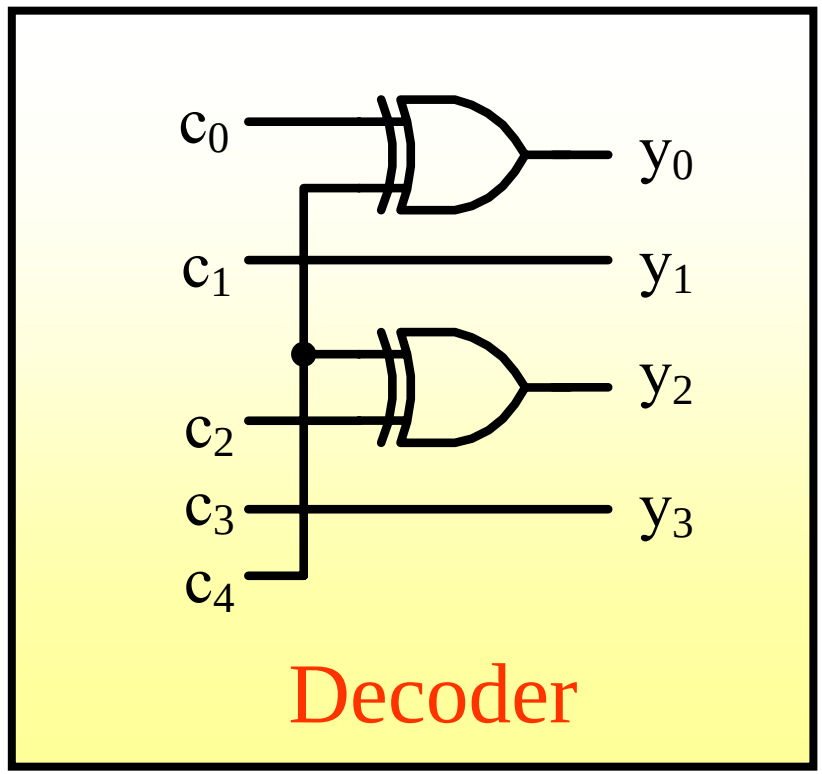
$C_0 = X_0$, $C_2 = X_2$

Dataword X_3~X_0	Codeword C_4~C_0
0 0 0 0	0 0 0 0 0
0 0 0 1	0 0 0 0 1
0 0 1 0	0 0 0 1 0
0 0 1 1	0 0 0 1 1
0 1 0 0	0 0 1 0 0
0 1 0 1	1 0 0 0 0
0 1 1 0	0 0 1 1 0
0 1 1 1	0 0 1 1 1
1 0 0 0	0 1 0 0 0
1 0 0 1	1 1 1 0 0
1 0 1 0	1 1 1 1 1
1 0 1 1	1 1 1 1 0
1 1 0 0	0 1 1 0 0
1 1 0 1	1 1 0 0 0
1 1 1 0	0 1 1 1 0
1 1 1 1	0 1 1 1 1

Encoder/decoder for green bus coding

- More simple and effective
- Avoid forbidden overlap condition (FOC) and forbidden pattern condition (FPC) and reduce forbidden transition condition (FTC)





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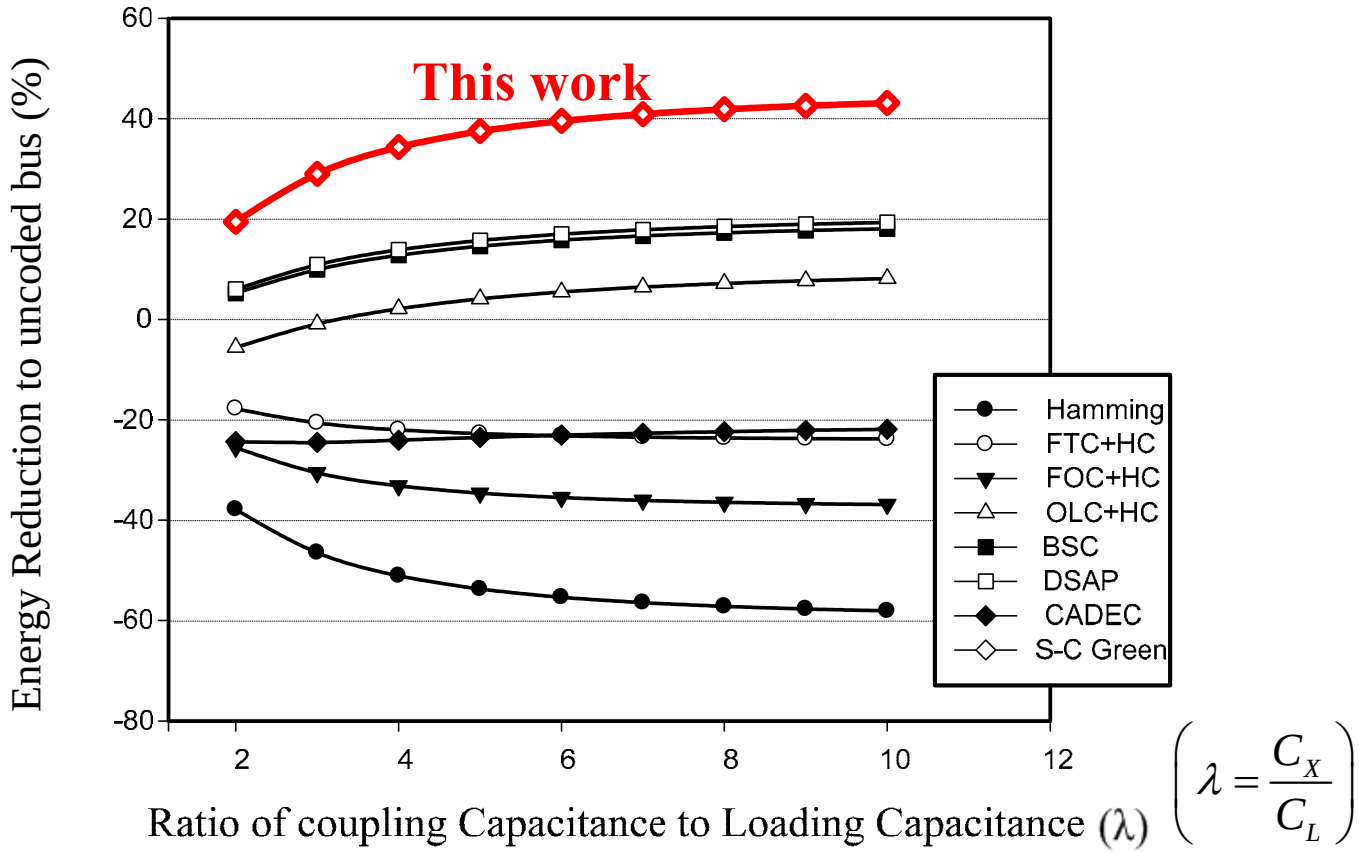
Energy reduction to un-coded code

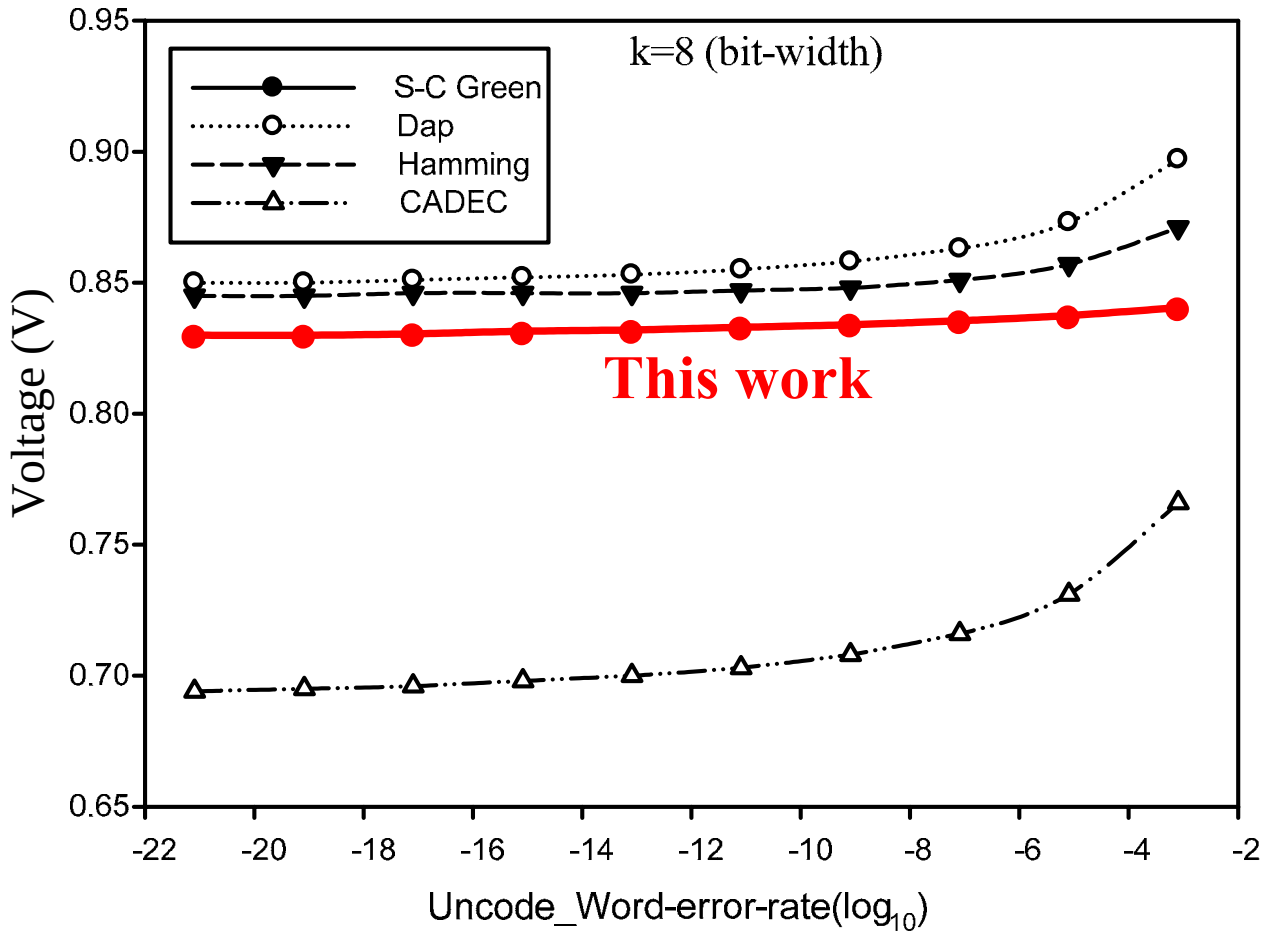
Simulation Condition :

- UMC 90nm CMOS technology
- The length of wires is set as 0.8mm of metal-4 with minimum width and spacing of 0.2um.



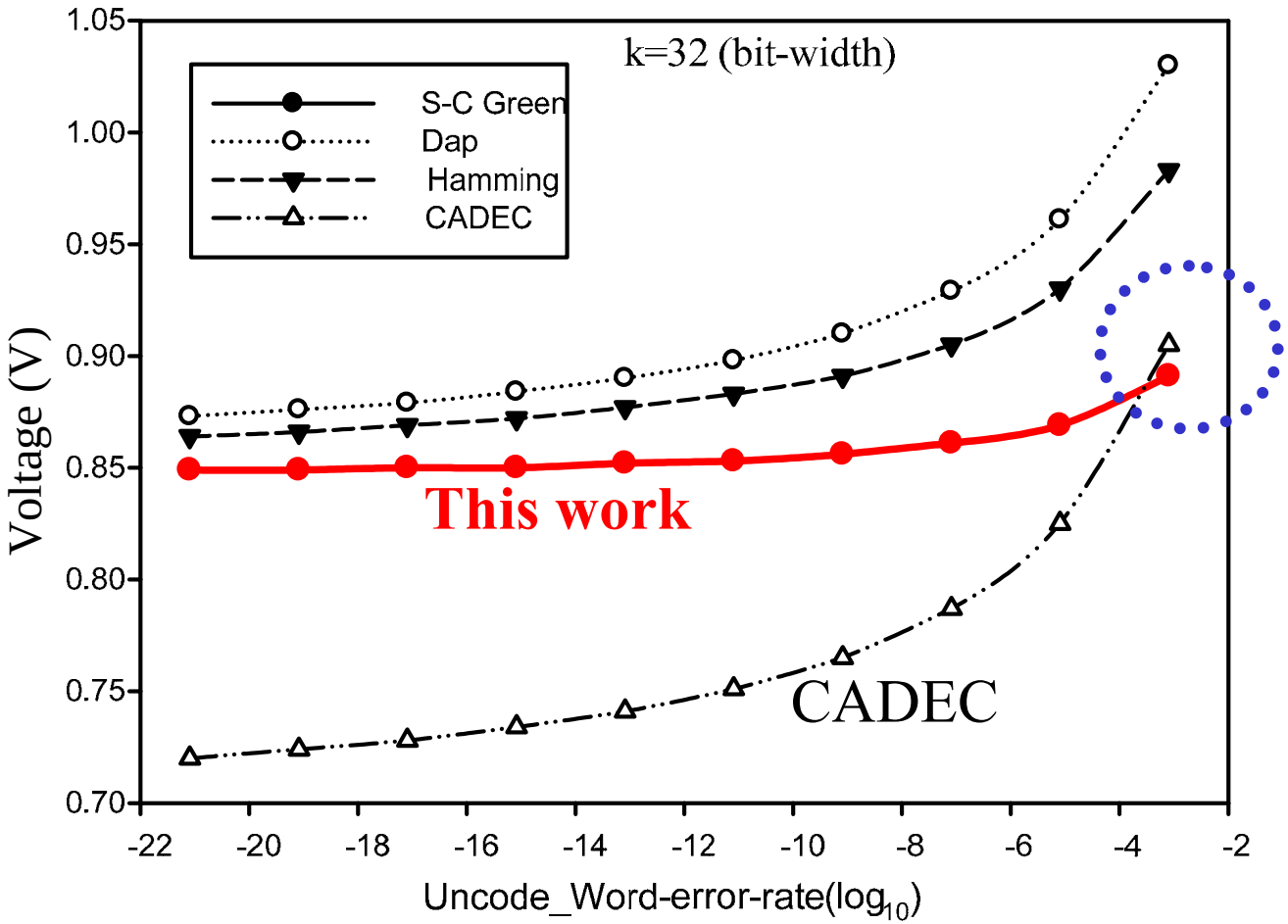
Voltage of specific error correction coding (k=8)

$$P_{\text{triplication}} \approx 3k\varepsilon^2 - 2k\varepsilon^3$$



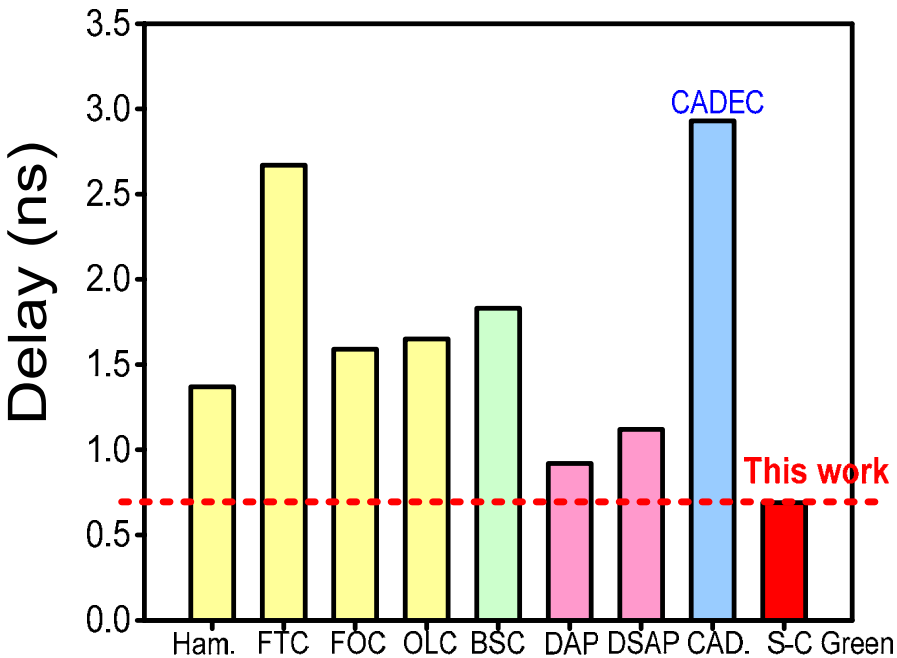
Voltage of specific error correction coding (k=32)

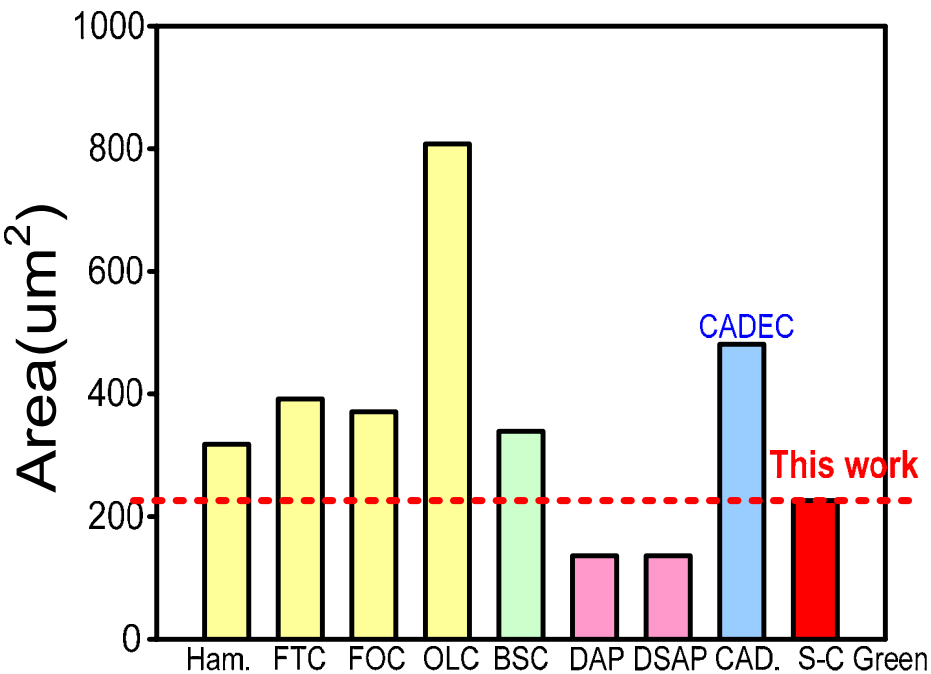
$$P_{\text{triplication}} \approx 3k\varepsilon^2 - 2k\varepsilon^3$$



Summaries of different joint coding codec

- The proposed self-corrected green coding scheme has the smallest area overhead of codec.
- For the smallest delay, it is more suitable for the network-on-chip architecture.





Summaries of different joint coding schemes

- Except for s-c green coding, DAP and DSAP, the critical delay of codec depends on the decoder, others are not appropriate for integrating into switch fabrics because of long critical delay .

Coding Scheme	Energy saving (1.2v)	Lowest supply voltage ($\varepsilon \cong 10^{-20}$)	Energy saving (Lower Voltage)	Physical transfer unit size (wire)	Physical transfer unit size (Router)
Uncoded	0	1.2 v	0	8	8
Hamming	-51.08%	0.845 v	+26.38%	12	12
FTC-HC	-22.01%	0.845 v	+40.07%	21	21
FOC-HC	-33.17%	0.845 v	+34.82%	16	16
OLC-HC	+2.12%	0.845 v	+51.46%	34	34
BSC	+12.78%	0.850 v	+55.95%	17	17
DAP	+11.92%	0.850 v	+55.54%	17	8
DSAP	+13.86%	0.850 v	+56.46%	25	17
CADEC	-24.05%	0.695 v	+58.84%	25	25
S-C Green	+34.34%	0.836 v	+67.29%	30	10

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Conclusions

- *Self-corrected green coding scheme* is presented to construct reliable and low power interconnection for NoC.
- Triplication error correction stage
  - Rapid correction ability to reduce the physical transfer unit size
  - Self-corrected in bit level
- Green bus coding stage
  - More energy reduction by a joint triplication bus power model
- Based on UMC 90um CMOS technology, compared to un-coded code, self-corrected green coding can achieve 34.4% and 67.3% energy saving at voltage 1.2v and 0.84v, respectively.

Thanks for your attention!!