Impact of Process and Temperature Variations on Network-on-Chip Design Exploration

Bin Li, Li-Shiuan Peh, Priyadarsan Patra*

Princeton University
{binl, peh}@princeton.edu

*Intel Corporation
priyadarsan.patra@intel.com

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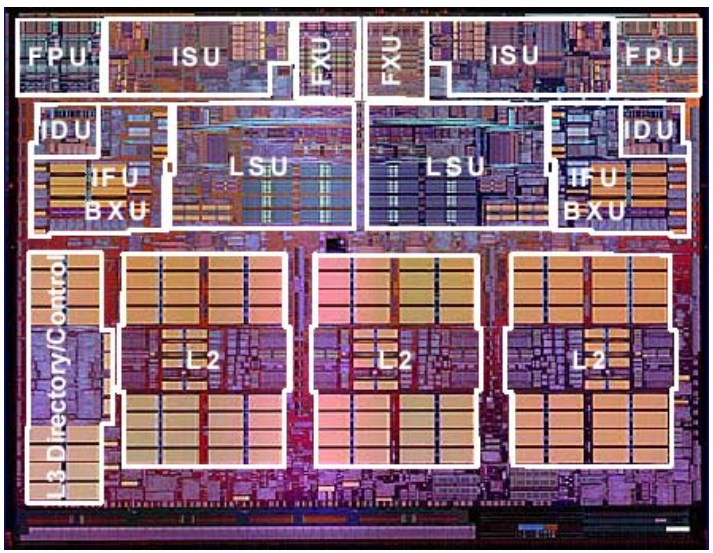
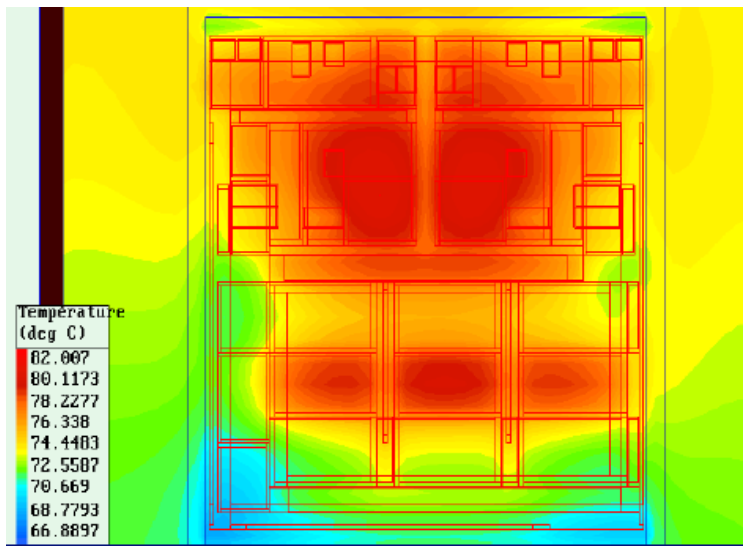
Process and Temperature Variations

- Process variation has higher impact on sub-100 nm CMOS
  - Transistor dimension variation : Sub-wavelength lithography
  - Transistor characteristic variation: Dopant density fluctuation etc
- Temperature variations: caused by workload variation



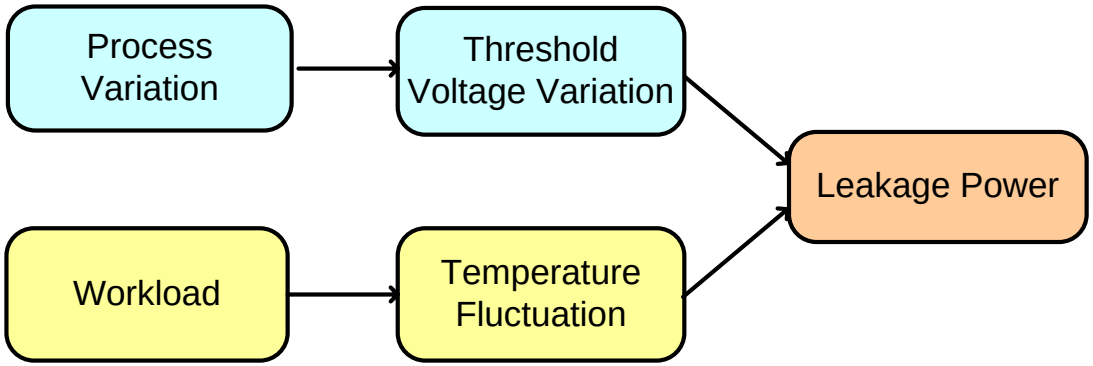
Power 4 Server Chip floorplan

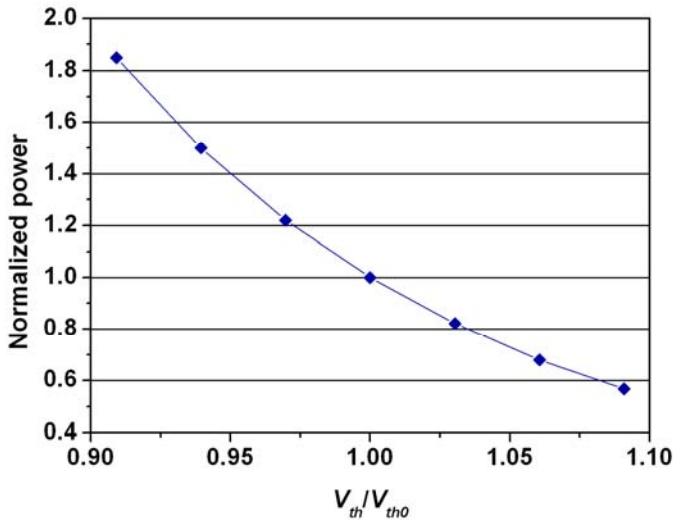


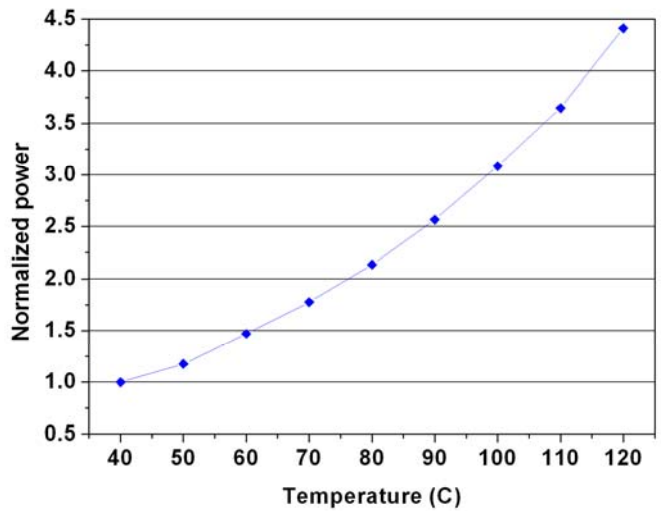
Chip thermal profile

[IBM research, Austin]

Impact on Power Consumption



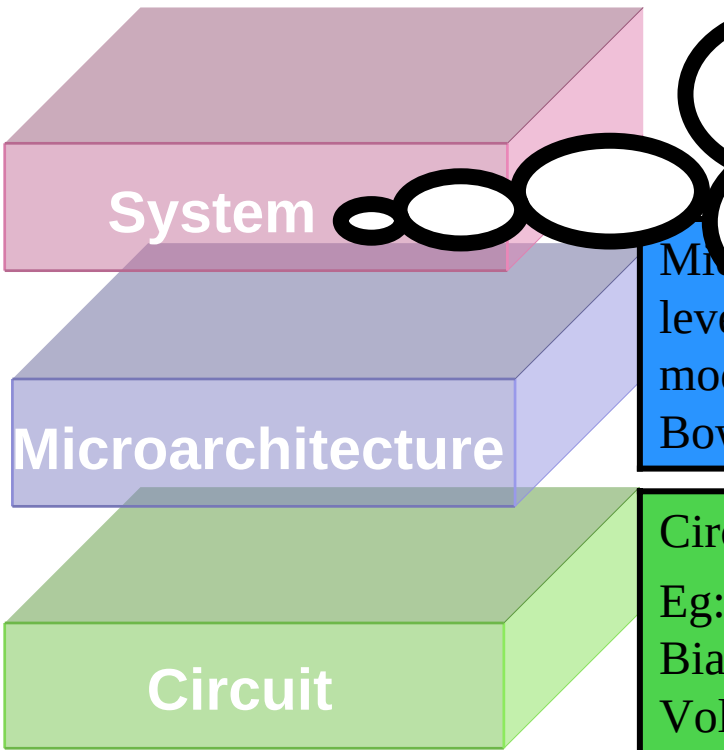




Need to consider process variation for leakage

Need to consider within-die temperature variation for leakage

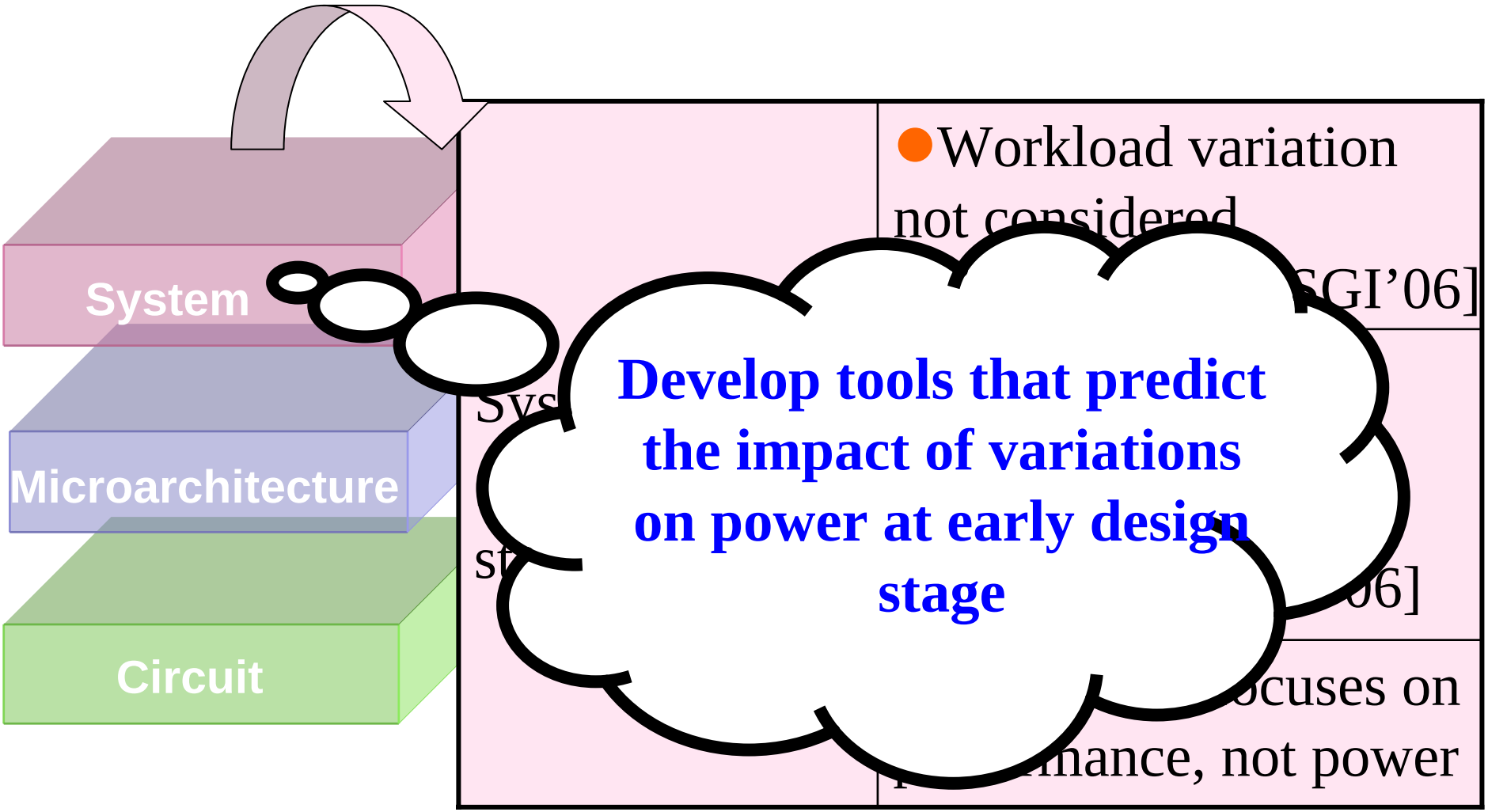
Current Approaches



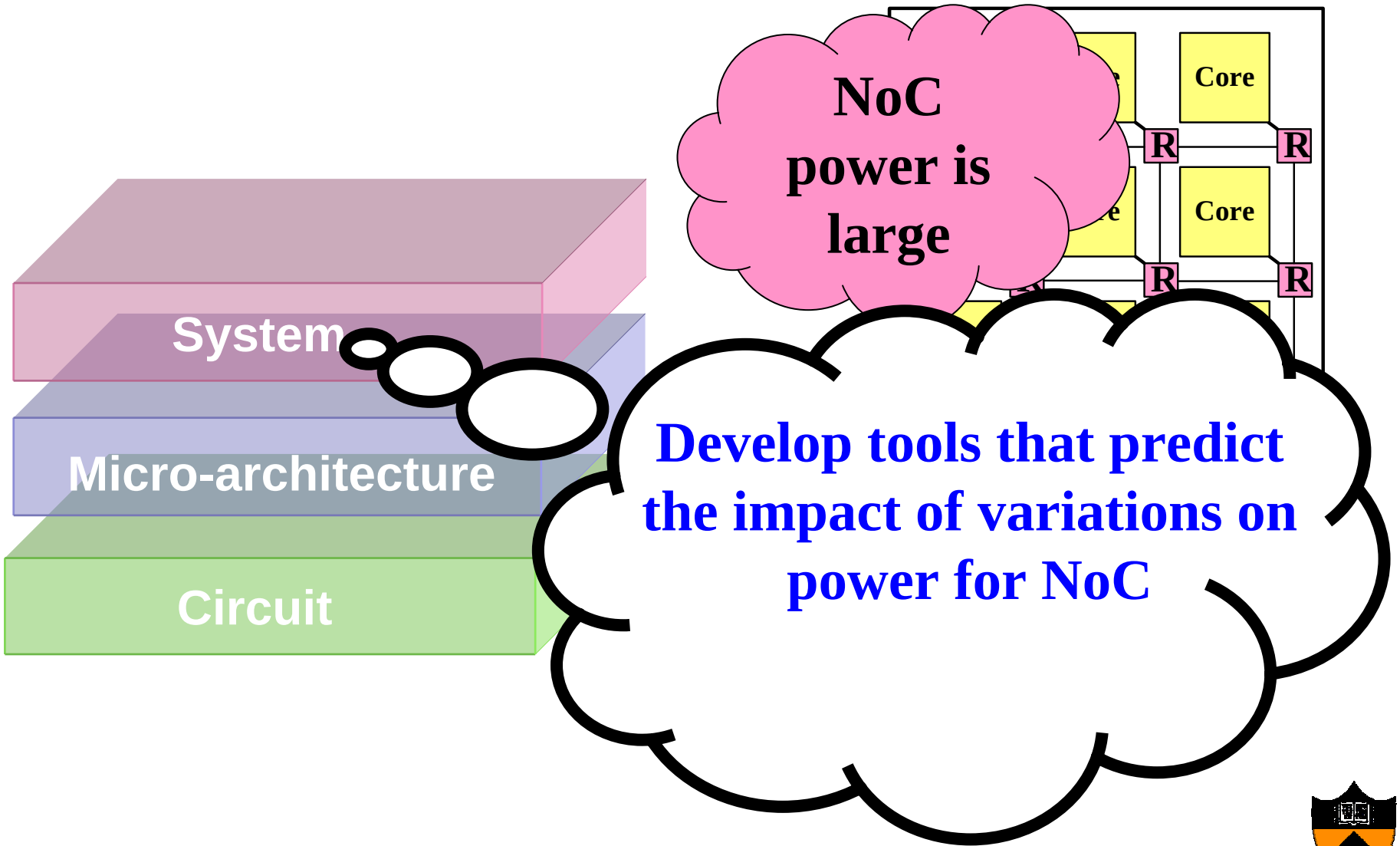
Need tools that predict the impact of variations on design metrics at early design stage

Mi… level: An… modeling [eg. Bowman, JSSE'02]	
Circuit level: Eg: Adaptive Body Biasing, Adaptive Voltage Scaling [Tschanz, JSSC'02]	Expensive to implement Often too late for changes

Current Approaches



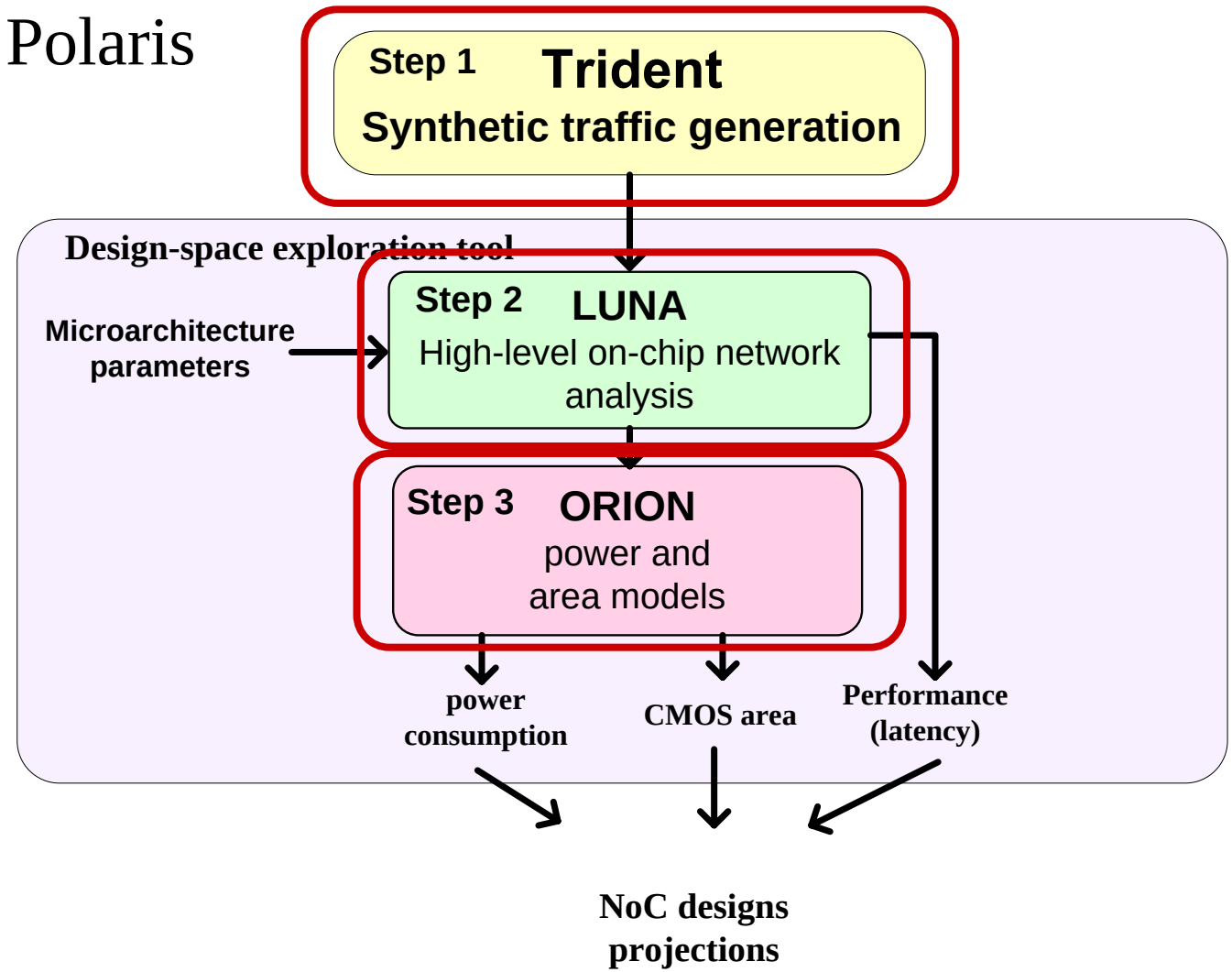
Network-on-Chip (NoC) for CMP



Outline

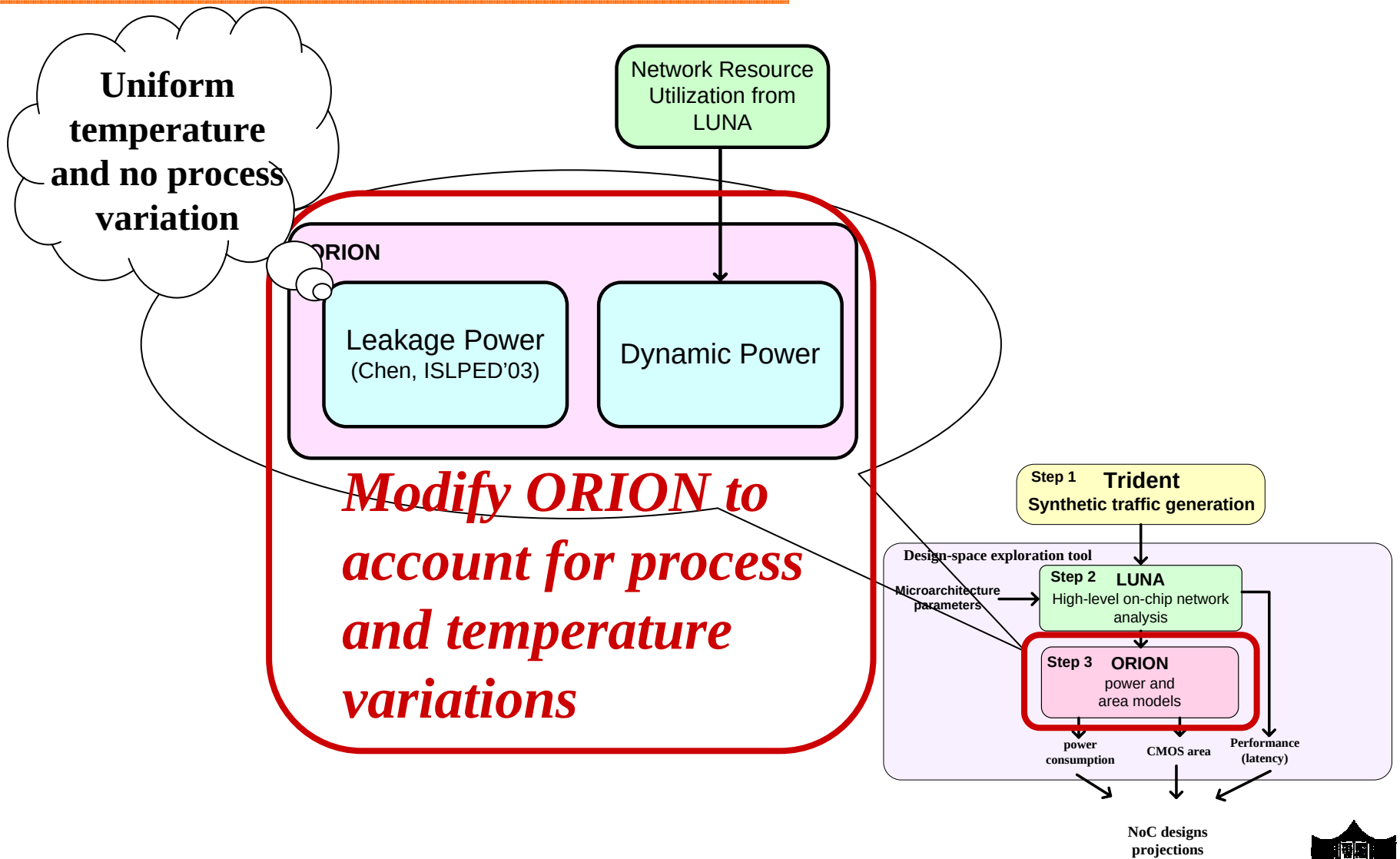
- Introduction and Motivation
- Methodology and Tool Development
- Case Study
- Conclusions and Future Work

Leverage Polaris Toolchain for Variations

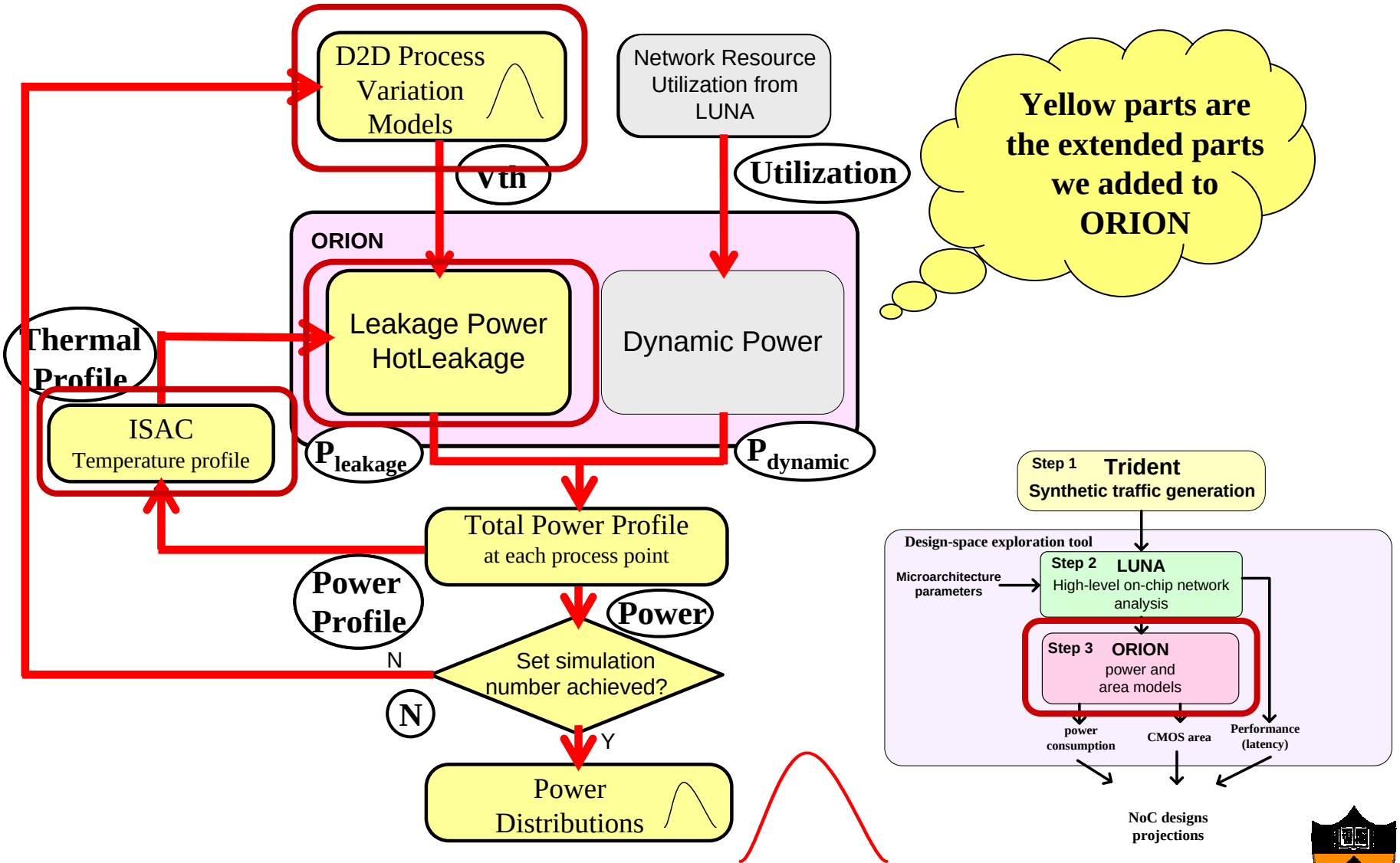


V. Soteriou, N. Eisley, H. Wang, B. Li, L.S. Peh, TVLSI'07

Polaris: ORION Power Model



New ORION Model (Process and Temperature Aware)



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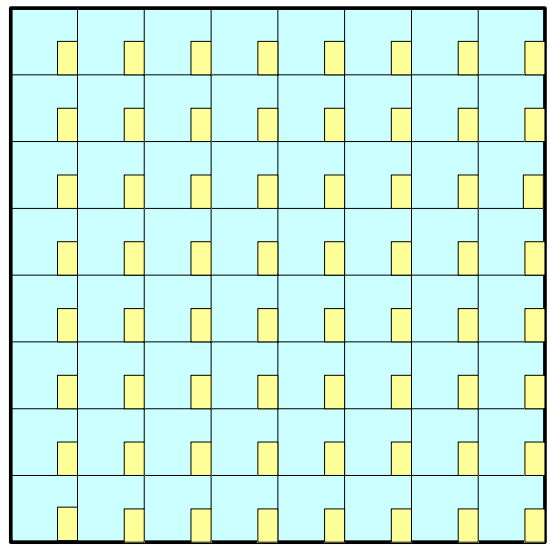
Experimental setup

- Technology
  - 64-node chip
  - 65nm technology
  - Supply voltage : 1.2V
  - Frequency: 3.8GHz
  - Threshold voltage:
    - mean=0.25 V
    - standard deviation= 6%
  - Die size:14.4mm x 14.4mm x 0.6mm



Design Space Explored

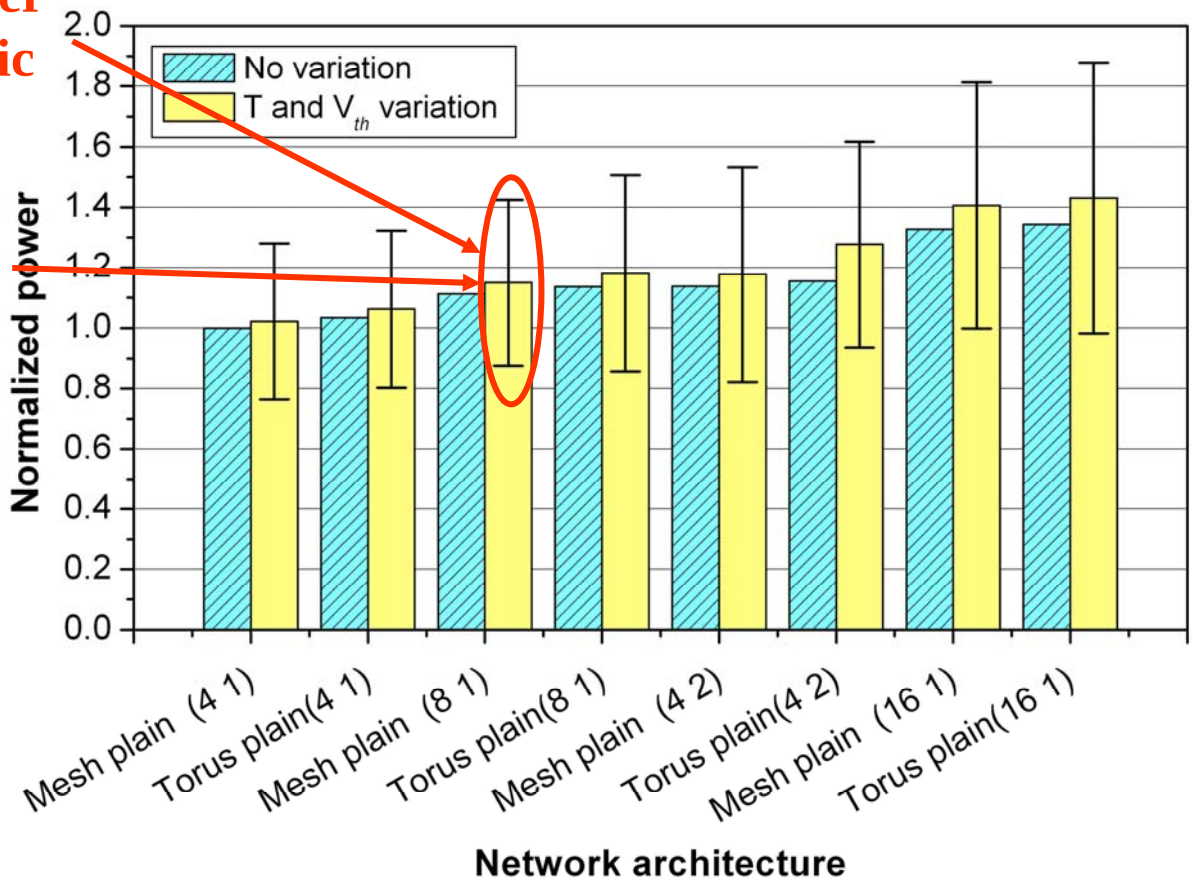
Topology	2D mesh plain
	2D mesh with express cub
	2D mesh with hierarchica
	2D torus plain
	cube interval 2, 4
	ical link interval 2,3,4
Buffer size (64-bit flits)	
Virtual channels per link	
Routing	Deterministic routing (X-Y)
Traffic	Long distance, moderately bursty, hot-spot traffi

What is the optimal on-chip network architecture for my application?

Effects of Process and Temperature Variations on Power

Distribution rather than deterministic

Average power increases



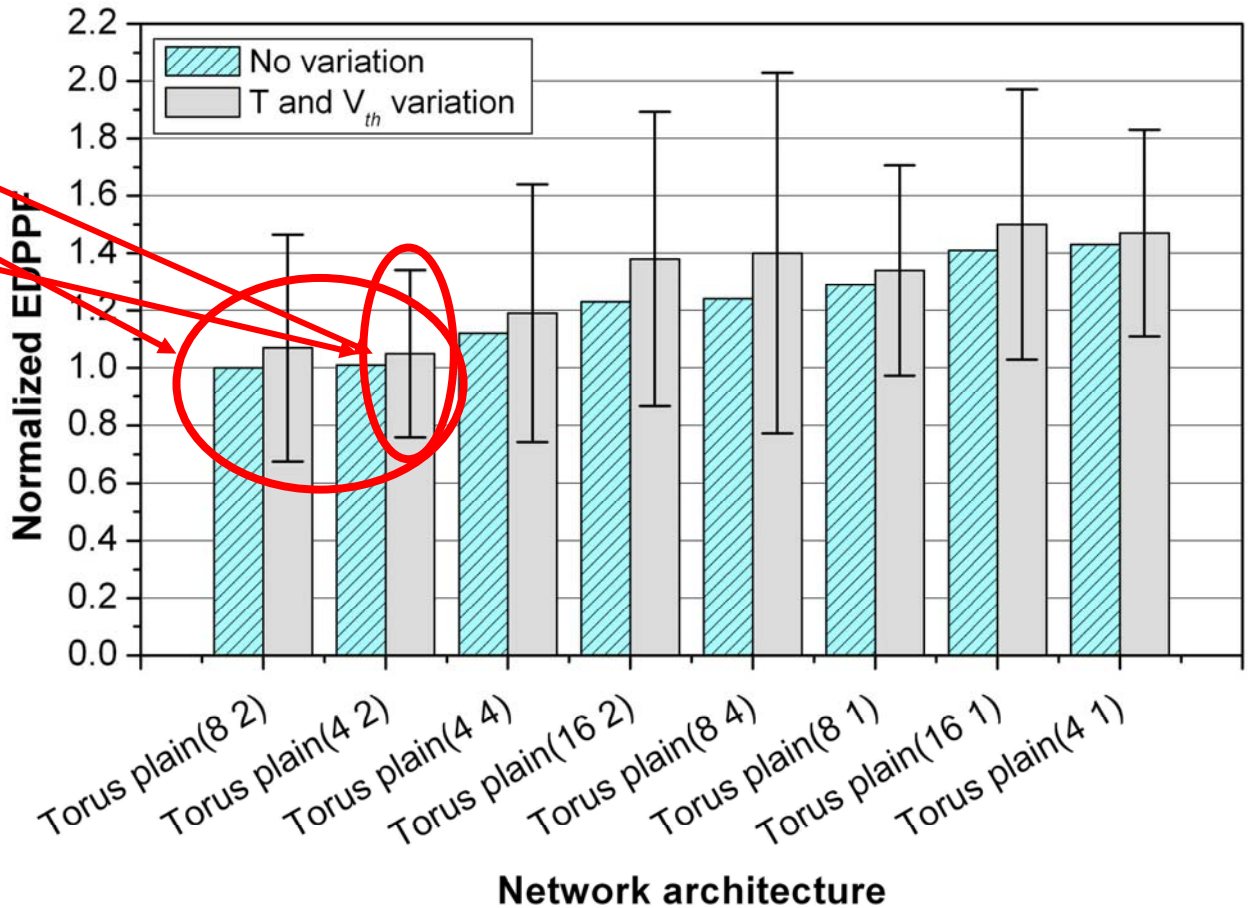
x axis format: topology variant (buffer size, number of virtual channels)

Process and temperature variations affect power consumption

Effects of Process and Temperature Variations on EDPPF

- Average smaller
- Distribution change smaller

Decision might



x axis format: topology variant (buffer size, number of virtual channels)

Early design exploration quantify effects of variations

Other Aspects not Covered

- Sensitivity analysis
  - Only consider temperature variation
  - Only consider process variation
- Mean x standard-deviation metrics

Conclusions

- Early design stage tool that accounts for process and temperature variations
- Process and temperature variation strongly impacts power
  - Influence design choices
  - Need to be considered together

Future Work

- Study how within die process variations affect the network power consumption
- Studying process and temperature variation effects on network operating frequency

Thank you !