The Effects of BTI Aging on the susceptibility of On-Chip Communication Schemes to Soft Errors in Nano-Scale CMOS Technologies

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This work is done in celebration of the 60th Birthday of Professor Alex Yakovlev, my mentor and my friend. Happy Birthday Alex ☺

Abstract. The continuous scaling of semiconductor devices has introduced new circuit failure mechanisms such as bias temperature instability, and made existing reliability problems more severe such as single event transients (SET), variability and crosstalk. This work provides a frame work to quantify the soft errors induced by crosstalk and radiation hits in on-chip communication schemes and investigates the effects of aging on the susceptibility of on-chip communication to these transient failures. It also provides a comprehensive comparison between synchronous and asynchronous communication methods in terms of their robustness against soft errors. Our results based on SPICE level simulations in 90 nm technologies indicate that BTI aging increases the probability of delay-induced soft errors but mitigate the effect of glitches-triggered errors.

1. Introduction

One of the major challenges facing the SoC designers of dependable and/or safety critical systems is the intrinsic unreliability of the communication infrastructure in Nano scale CMOS technologies [1, 2]. There are number physical mechanisms which may cause soft errors in on-chip communication links, examples include: crosstalk and radiation, and power bounce [3]. Such problems are further worsened by Variability and CMOS aging. The former refers to the inaccuracies in manufacturing pro-

cesses and within-die voltage-temperature variations that lead to fluctuations in circuit performance and power consumption. It arises from scaling very large-scale integrated (VLSI) circuit technologies beyond the ability to control specific performance-dependent and power-dependent parameters [4, 5]. Variability has become a first order limitation to continued scaling. At deep submicron technology nodes, the achievement of parameter precision becomes exponentially more difficult due to the limitations imposed by quantum mechanics. The various intrinsic sources of variability such as random dopant distribution cannot be reduced by better process control and their effect is generally random, this is shown by atomistic modelling in [6, 7]. Therefore, the impact of variability is expected to be significant in future technologies [5, 8], making variations an unavoidable characteristic of future VLSI circuits.

CMOS aging is another major concern for modern VLSI designers, It refers to a slow progressive degradation in the performance of MOS transistors; it is caused by several failure mechanisms; namely: Bias Temperature Instability (BTI); Hot Carrier Injection (HCI); and Time- Dependent Dielectric Breakdown (TDDB) [9, 10]. BTI is often cited as the primary reliability concern in modern processes [11]. Negative bias temperature instability (NBTI) in PMOS transistors is more dominant than positive bias temperature instability in NMOS transistors in the latest process technology especially after the introduction of nitrogen into gate stacks, which reduces boron penetration and gate leakage, but leads to worse NBTI degradation [12]. This mechanism is characterized by a positive shift in the absolute value of the threshold voltage of the PMOS device, such a shift is typically attributed to hole trapping in the dielectric bulk and the breakage of Si-H bonds at the gate dielectric interface [13]. Positive bias temperature instability (PBTI) in NMOS transistors also has the same effect but is only considered crucial in devices which use high K-dielectrics. BTI aging causes delay to increase, which can eventually lead to timing errors and system failure [9, 10, 14]. The effects of aging on the performance and reliability of systems on chips have been extensively addressed in the literature [15-20]. In addition, there are extensive works in the literature in the area of reliability enhancement techniques for soft errors. The authors of [21] proposed a data-redundancy-based fault tolerance method for self-timed phase-encoded channels in order to mitigate the effect of crosstalk-related errors. In [22] Lin et al proposed a radiation hardened register design for protecting microprocessors pipelines from alpha particles hits. The use of error correction and detection codes has also been proposed to enhance the reliability of on-chip communication [23, 24]. However to the best of our knowledge, there are no previous studies on the effects of BTI aging on the susceptibility of on-chip communication schemes to soft errors. The contributions of this work are as follows:

1) It provides a framework to quantify the soft errors induced by crosstalk and radiation hits in on-chip communication schemes.
2) It investigates the effects of aging on the susceptibility of on-chip communication to soft errors.
3) It provides a comprehensive comparison between synchronous and asynchronous communication methods in terms of their robustness against transient failure mechanisms.

The rest of the paper is organized as follows. Section 2 and 3 outline the computation of closed form expression to quantify the soft error caused by crosstalk and radiation hits respectively. The experimental setups and the analysis methodology are explained in section 4. Simulation results are presented and discussed in section 5. Conclusions are drawn in section 6.

2. Computation of Crosstalk-Induced Error Rate

The soft errors caused by crosstalk can be classified into two types, namely:

1. Glitch-induced soft errors: these are caused by static noise pulses induced on a quiet victim net due to switching of neighbouring aggressors. If such a pulse propagates through logic gates and reaches storage elements, it can mistakenly be considered as a valid data item
2. Delay-induced soft errors: these are due to violations in the timing constraints which occur when the timing of a stage (i.e. gate and interconnect) becomes uncertain due to coupling from the switching activity of neighbouring stages (i.e. Miller effect). This results in a change in the total capacitance of the wire, hence dynamic delay.

The following two subsections provide closed form expressions that can be used to compute the probability of crosstalk-induced soft errors in synchronous and asynchronous channels, respectively.

2.1. Crosstalk Error Rate in Synchronous Links

Synchronous design methodologies globally distribute a timing signal (a clock) to all parts of the circuit. Transitions (rising and/or falling depending on the design) on this clock line indicate moments at which the data signals are stable and therefore ready to be sampled. In synchronous links, crosstalk can cause both delay and/or glitch-induced soft errors; this depends on the data transition state on the bus.

To illustrate crosstalk effects on a synchronous communication channel, consider the link shown in figure 1, it is a typical D-flip-flop (DFF) pipelining stage. Data is

normally transmitted every clock cycle where the latches are triggered at the clock rising edge.

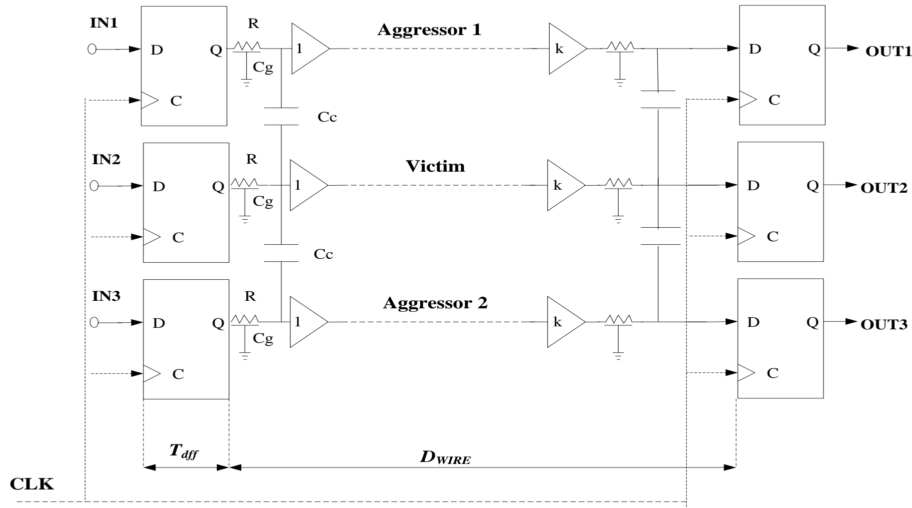

Figure 1: A Synchronous Communication Link

To ensure correct data transmission, intermediate values of logic signals or glitches must settle down before the next clock edge such that there is a stable logic value at the input of each register. Crosstalk-Delay-induced soft errors can only occur on a victim wire during a data transition event (0=> 1 or 1=>0), whereas glitch-induced soft error occurs on a victim wire when the data on it is stable and there are transitions on neighbouring lines. For example in a three-wire link as shown in figure 1, each wire has four possible transition states (UP (0=> 1), Down (1=>0), Stable(1), Stable(0)), so there are (4^3 =64) possible transition states. In 32 of which, the middle line is vulnerable to crosstalk delay errors. In 14 of which are, the middle line is vulnerable to crosstalk glitch errors. In the remaining 18 state, the middle line is not vulnerable to any crosstalk-induced soft errors.

The average probability of a crosstalk delay soft error (CDSE) on a victim line per transmission cycle (i.e. per clock cycle in this case) can be computed as follows:

$$CDSE = \sum_{I=1}^{SD} TER_i * Oi \quad (1)$$

The average probability of a crosstalk glitch soft error (CGSE) on a victim line per transmission cycle can be computed as follows

$$CGSE = \sum_{j=1}^{SG} GER * Oj \quad (2)$$

Where:

TERi is the probability of crosstalk-delay induced soft error during a bus transition state i

GERj is the probability of crosstalk-delay induced soft error during a bus transition state j

SD is the number of transition states on the bus in which delay errors are possible

SG is the number of transition states on the bus in which glitch errors are possible

Oi is the occurrence probability of a transition state i

Detailed closed form expressions to compute *TER* and GER are provided in our previous work [25].

2.2. Crosstalk Error Rate in Delay-Insensitive Asynchronous Links

Asynchronous methodologies typically encode the timing information in the data line activity itself, therefore there is no need for a separate timing signal [26, 27]. Delay-insensitive channels are an important class of asynchronous communication scheme, these channels are self-timed, and hence, insensitive to signal propagation delays, in other words, they have no timing constraints. Therefore, they are inherently resilient to crosstalk-delay soft errors. However, they are still prone to crosstalk glitch soft errors. There are many possible delay insensitive coding methods such as M-out-of-N, Burger, and Knuth codes [26, 27]. The average probability of a cross-talk-glitch soft error (CGSE) per transmission cycle can be computed using equation 2 above.

3. Computation of Radiation Hits-Induced Error Rate

The probability of a radiation-induced soft error is the product of two factors, namely: the probability of energetic radiation hits and the probability of a functional failure caused by such a strike. The first factor depends on the environment under which the circuit is operating, and is independent of the architecture and the design of the circuit; therefore, it is not relevant in a comparative analysis of various design techniques, and it is not going to be addressed in this work. On the other hand; the

probability of a radiation-induced glitch turning into a soft error is a function of the circuit architecture and fabrication technology; therefore, it can be used as a metric to estimate the susceptibility of an on-chip communication schemes to radiation-induced soft errors. The following two subsections provide closed form expressions that can be used to compute the probability of a radiation glitch soft error (RGSE) for both synchronous and asynchronous channels:

3.1. Radiation Error Rate in Synchronous Links

A radiation-induced glitch at the input of an edge triggered flip flop can cause a functional failure if it is erroneously sampled or if it forces the devise to go into metastability state. The occurrence time of the glitch and its width determine whether or not it generates an error. Consider the case of a synchronous link in figure 1, assume a glitch is generated by a repeater due to a radiation hit. In order for this glitch propagate to cause an error, it has to satisfy the following three conditions:

1) Glitch amplitude Condition (GA): the amplitude of the glitch should exceed the threshold voltage of the receiving flip-flop
2) Glitch Timing condition(GT): The glitch should coincide with the sampling clock in order for it to be latched
3) Glitch Width Condition (GW): it should be sufficiently wide i.e. (its amplitude should remain higher than the threshold voltage while the flip-flop input is being sampled.)

Therefore, given a radiation hit has actually happened, the probability of a soft error caused by such the radiation-induced transient pulse in synchronous links is given as follows:

$$RGSE = GA * GT * GW \tag{3}$$

Detailed closed form expressions to compute *GA*, *GT,* and *GW* are provided in our previous work [28].

3.2. Radiation Error Rate in Delay-Insensitive Asynchronous Links

In this type of links, a radiation-induced glitch can lead to the generation of illegal code words, for example in (1-of-4) based channel, a code word (0001) can be received as (0011). Depending on the design of the receiver, this erroneous data symbol can be disregarded or wrongly interpreted as a different symbol. In order for this a radiation-induced transient to cause such a failure, it should only satisfy the glitch

amplitude condition (ga). This is because data can be sampled at any time in delay insensitive links, so there is a high probability for a glitch to cause an error if it exceeds the threshold voltage of the logic gates. Therefore, the probability of a soft error caused by a radiation glitch in asynchronous links is given as follows:

Therefore, given a radiation hit has actually happened, the probability of a soft error caused by such the radiation-induced transient pulse in Asynchronous delay insensitive links is given as follows:

$$RGSE = GA \tag{4}$$

4. Analysis Method and Experimental Setups

In this section we first outline the aging model we have used, and then summarize our analysis method and experimental setups

4.1. Bias Temperature Instability Model

BTI consists of Negative Bias Temperature Instability (NBTI) in pMOS transistors and Positive Bias Temperature Instability (PBTI) in nMOS transistors. The reaction diffusion model has been developed in [29] to allow designers to estimate the drift of Vth (ΔVth) induced by BTI effects as a function of technology parameters, operating conditions and time. However, the drift of Vth does not depend on the frequency of input signals, but only on the total amount of the stress time, therefore a closed form analytical model has recently been proposed which allow designers to estimate long term threshold voltage shift as follows [30, 31] :

$$\Delta V_{th} = \chi K \sqrt{C_{ox}(Vdd - Vth)} \exp\left(\frac{E_a}{k_B T_A}\right) (\alpha t)^{1/6} \tag{5}$$

C_{ox} is the oxide capacitance;

t: is the operating time;

α: is the fraction of the operating time during which a MOS transistor is under a stress condition. It has a value between 0 and 1. α = 0 if the MOS transistor is always OFF (recovery phase), while α = 1 if it is always ON (stress phase);

E_a: is the activation energy ($E_a \cong 0.1$eV);

k_B: is the Boltzmann constant;

T_A: is the aging temperature;

χ: is a coefficient to distinguish between PBTI and NBTI. Particularly, χ equals 0.5 for PBTI, and 1 for NBTI;

K: lumps technology and environmental parameters.

4.2. Analysis Methodology

In order to estimate the impact of BTI aging on the susceptibility of on-chip links to soft errors, we have adopted the following approach:
First, we have considered a synchronous communication link as shown in figure 1. We have also considered three delay-insensitive channels: (1-of-4), (3-of-6) and (2-of-7). The physical layouts of all communication schemes considered are the same in all experiments. Second, we estimated the soft error rate induced by crosstalk and radiation hits expression provided in equations (1), (2), (3) and (4) based on SPICE level simulations in 90nm technology. Third, in order to estimate the impact of BTI aging, we computed the degradation in electrical parameter of transistors based on the model presented in Section 4.1 The ΔVth value obtained for each considered operating time interval was then utilized to customize the SPICE device model and simulate the communication link with the proper BTI degradation. Particularly, we have considered three operation points after 1 day, 1 year, and 5 years. Fourth, we estimated the soft error rate induced by crosstalk and radiation hits have been estimated again using circuits with degraded electrical parameters.

4.3. Experimental Setups

The communication medium considered in this study is top metal layer in the 90nm technology. The interconnect structure used is three signal lines between two grounded shields as shown in figure 1. Each wire is modelled as a distributed RC network with four Π-model segments. The resistive and capacitive parasitic elements of the wires are calculated using equations from [32]. To model process variations, we have considered seven sources of variations, namely: wire width (w), metal thickness (t), interlayer dielectric thickness (h), metal resistivity (ρ), gate length (Leff), supply voltage (Vdd) and temperature (T). The variability of these parameters are assumed to be Gaussian and mutually independent. We have also assumed that

wire width (w) and spacing(s) are perfectly negatively correlated, letting w to be the independent variable. Table 1 summarises the mean and variations for each of these parameters. It is worth mentioning that the wire width shown in Table 1 is the minimum wire width in the considered technology.

Table 1: The Nominal Values and Variations of Circuit Parameters

Parameter	Nominal Value	Variations
Interlayer Dielectric height	0.94 *um*	20%
Metal resistivity	21.8 *nΩ.m*	20%
Wire thickness	0.81 *um*	20%
Wire Width	0.56 *um*	20%
Transistor length	90 *nm*	10%
Power Supply	1.2 *V*	10%
Temperature	27 ^{o}C	12 – 43 ^{o}C

In all of our simulations we have considered a channel with a 10 mm wire length, each line has four equally spaced and minimally sized repeaters. We used a clock frequency of 1.5 GHz for simulating the synchronous link.

For crosstalk error rate commutation of synchronous links, the delay of the victim wire has been estimated using spice-level simulation for all possible transition activities. The amplitude and the width of the induced crosstalk glitch the victim line glitch have also been estimated in the same manner. To estimate the impact of variability on the delay and glitch characteristics, we have employed the DoE statistical analysis approach to device a set of experiments in order to estimate the mean value and statistical distributions of measured parameters as shown in our previous work[33]. The above experiments are then repeated using circuits with degraded electrical parameters according to the aging model explained in section 4.1 For the estimation of crosstalk error of delay-insensitive links we followed the same approach above using the code [34]. The recorded values from each simulation are used to compute the crosstalk error rate according to the equations presented in section 2. For the computation of radiation errors, the single event transient (SET) values for 90nm technology presented in [35]. The mean and standard variation of the SET width is 500 and 150 ps respectively. The mean and standard variation of the SET amplitude is 0.1v and 0.32v respectively , these values are in agreement with the statistical distributions of the SET characteristics presented in [36].

5. Results and Discussions

5.1. The Impact of Aging on Crosstalk Error Rate

The results shown in figure 2 indicate the BTI aging leads to an increase in the susceptibility of synchronous links to crosstalk –induced delay errors. In this case the probability of a soft error is 10^{-8} which mean, every 100 million clock cycle we expect to have one soft error. After five years of operation the probability of a soft error is $3* 10^{-5}$ which is there order of magnitude larger. This sever degradation can be attributed to the induced delay degradation of the repeaters and flip-flops due to BTI aging in these links, which increases the probability of violating the timing constraints. On the other hand, the results shown in figure 3 indicate that the effect of crosstalk glitches on the reliability of synchronous links become less pronounced with aging, because the latter leads to an increase in the threshold voltages of CMOS transistors, therefore some of the crosstalk glitches will no longer be able to propagate and cause soft errors. A similar trend is also observed for asynchronous delay insensitive links as shown in figure 4. One interesting observation from figure 4 is the fact that some delay-insensitive code are more susceptible to crosstalk errors, this is because crosstalk errors are dependent on the transition activities and the data patterns on the bus, both of these factors are affected by the choice of a delay insensitive code. In particular 2-of-7 links are most prone to crosstalk-related errors at any time, so any glitch that exceeds the threshold voltage of a logic gate can propagate

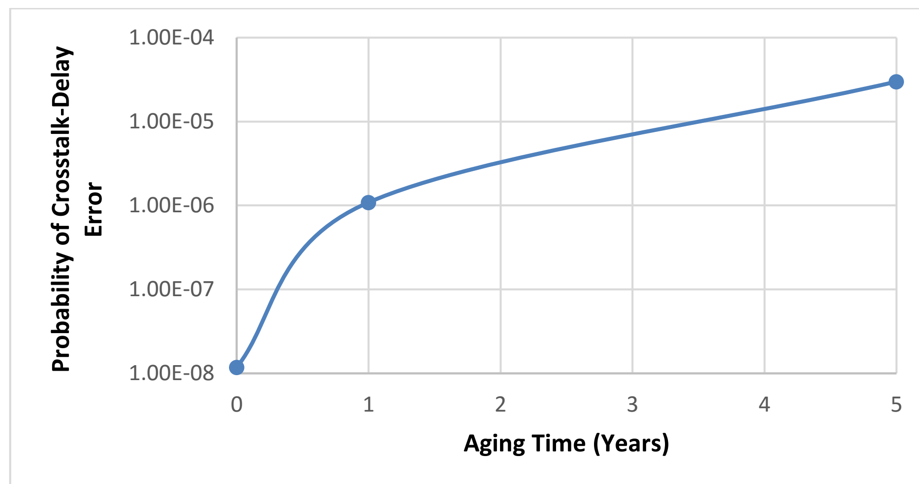

Figure 2: The Impact of BTI Aging on the Rate of Crosstalk-Induced Delay Errors in Synchronous Links

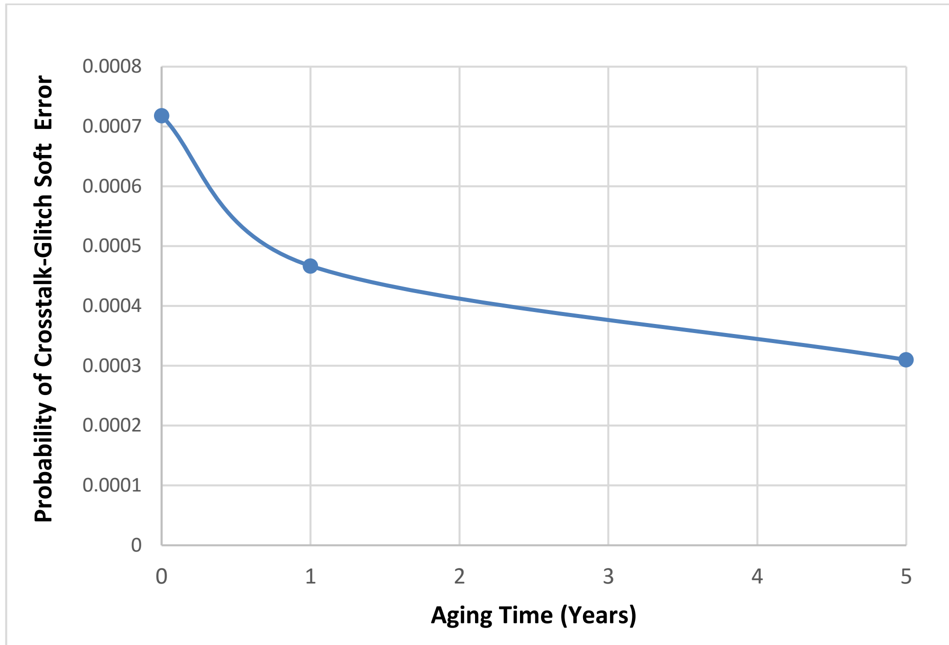

Figure 3: The Impact of BTI Aging on the Rate of Crosstalk-Induced Glitch Errors In Synchronous Links

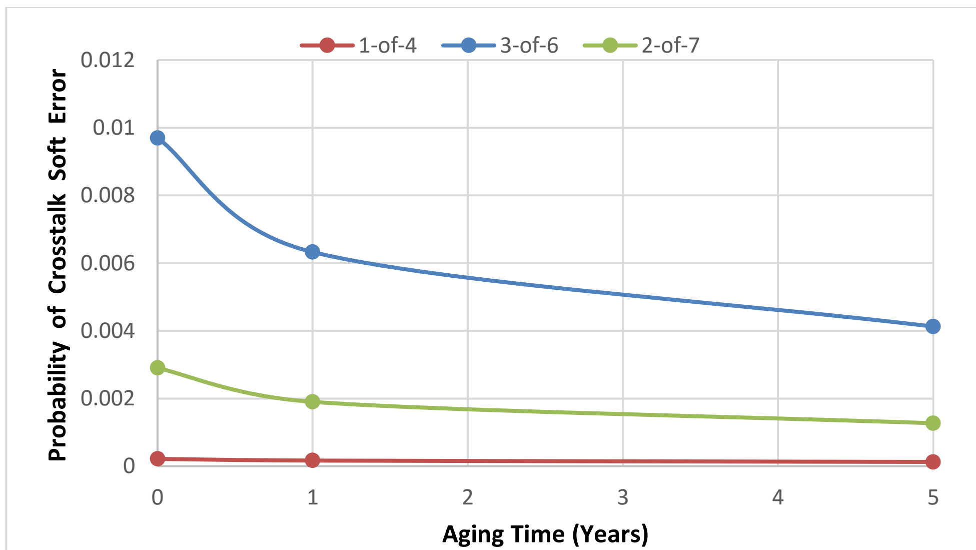

Figure 4: The Impact of BTI Aging on the Rate of total Crosstalk Errors in Asynchronous Links

5.2. The Impact of Aging on SET Error Rate

Figure 5 indicates that the effect of radiation-induced SET on the reliability of communication links become less pronounced with aging, this is mainly due to the fact that aging lead to an increase in the threshold voltages of CMOS transistors, therefore some of the SET glitches will no longer be able to propagate and cause a soft error. Again, asynchronous links seems be more vulnerable to this type of soft errors than synchronous channels due to their inherent nature of sampling logic values

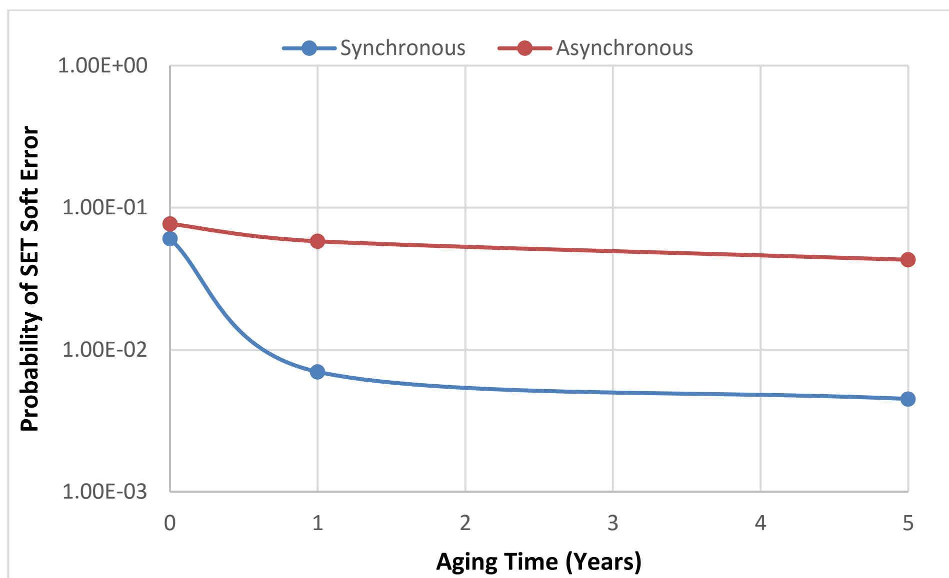

Figure 5: A Comparison of Single Transition Event Errors-Susceptibility (Synchronous vs. Asynchronous Links)

6. Conclusions

BTI CMOS aging is major concern for modern VLSI designers, It refers to a slow progressive degradation in the performance of MOS transistors; this mechanism is characterized by a positive shift in the absolute value of the threshold voltage of the PMOS device, such a shift is typically attributed to hole trapping in the dielectric bulk and the breakage of Si-H bonds at the gate dielectric interface. This work shows that aging can significantly affect the susceptibility of on-communication schemes to soft errors caused by crosstalk and/or radiation hits. In particular, BTI aging can lead to sharp increase in the rate of delay-induced soft errors; this is a major concern for synchronous

links. On the other hand, aging seems to mitigate the probability of a soft error caused by a noise pulse (due to crosstalk or SET), this means the robustness of asynchronous communication schemes against may become better as the circuit ages. On the other hand, Synchronous communication links seem to become more prone to delay-induced soft errors with aging but better protected against glitches and noise pulses.

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8. References

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