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Computational Heterogeneously Timed Networks (COHERENT)

http://async.org.uk/coherent/

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1 Background/Context

There is a consensus among the international research community that asynchrony is becoming an increasingly important issue at all levels because of rapid advances in complexity and feature-size-reduction of integrated electronic circuits and advances in distributed multiple computer systems for many real-time applications. (cf. the findings of ITRS-2003 and the CDS Panel http://public.itrs.net/Files/2003ITRS/Home2003.htm and http://www.cds.caltech.edu/~murray/cdspanel/). This prevalence of asynchrony and distribution provides the background to our work in concurrent, asynchronous and distributed real-time computational networks.

The research in COHERENT was a natural progression from the successful EPSRC project COMFORT (GR/L92471 at King's College London – KCL – and GR/L93775 at Newcastle University – NU), along the line of investigating data communication between computational units with heterogeneous timing. Like COMFORT, this project is a collaborative effort between two teams, one at NU and the other initially at KCL and then at Kingston University (KU).

At NU, this investigation is part of our long-term involvement in asynchronous hardware research and is supported by and related to such EPSRC projects as HADES (GR/K70175), BESST (GR/R16754) and STELLA (GR/S12036). At KU, this work is closely associated with our long-term research in the areas of vision and sensor networks and in intelligent CCTV surveillance. Our industrial partner in this project, MBDA (formerly known as BAe Dynamics, then Matra BAe), has a long-standing interest in real-time computational networks using Real-Time Network techniques including asynchronous data communication mechanisms (ACMs), and a continuing track-record of research and product development in this area.

COHERENT focussed on a number of new problems and in directions pointed out by the work of COMFORT. These include

- the systematic synthesis of ACMs,
- further analyses of ACM properties,
- overall architecture issues of computational networks with heterogeneously timed components connected through ACMs, using Real-Time Network (RTN) methods derived from MASCOT techniques,
- design of application systems, especially intelligent CCTV surveillance and distributed control systems,
- development of a Real-Time Network on Chip (RTNoC) technology.

2 Key advances and supporting methodology

The project's target area was the modelling, design and verification of concurrent, distributed, and asynchronous real-time computational networks. The emphasis was on heterogeneous timing among the components of such networks. At the start of COHERENT, it was observed that a gap existed between system design, modelling and verification methods based solidly on synchronous assumptions and the natural heterogeneous timing of distributed systems. The need for a more mature Real-Time Network method, including component and system design/synthesis, modelling and analysis/verification, was quite clear.

COHERENT set out to deal with this problem through research dedicated to Real-Time Networks at all levels of detail, from further in-depth studies of classes of components, especially the data communication components (ACMs), to exploring architecture-level strategies. The objectives of this project were

(a) Development of an architecture for RTNoC
(b) Development of design flow for RTNoC systems
(c) Development of a parameterized library of ACMs
(d) Testing the RTNoC technology with real application system examples
(e) Development of tools in support of (a) – (d)

We believe the project made significant advances in all these objectives. In particular, new contributions were made in the areas of developing Real-Time Network component models for use in application systems (using Matlab and Network Simulator), designing example vision network systems and distributed control systems using Real-Time Network methods, automatic synthesis of ACMs, gaining further insights into ACMs (such as their functional aspects and the logical organization of individual types) and developing a number of software tools in support of ACM and Real-Time Network design. We also made significant progress in a number of related sub-problems within the project. One of these is the successful fabrication of hardware used in testing timing and metastability related properties in circuits through a collaboration with Sun Microsystems.

2.1. Development of an architecture for RTNoC

Initially, our work concentrated on investigations of existing network architectures related to real-time, distributed systems with asynchrony, especially current and future wireless technologies [1, 2]. It was noted that all existing networking technologies ultimately rely on some form of synchronization between computational components and this reliance can be reduced or eliminated by using Real-Time Network systems.

We also investigated various forms that a proposed architecture for RTNoC might take. The conclusion was that the best option is to make use of the existing method of connecting computational nodes with passive data storage/communication components found in MASCOT [3, 4]. This method was then proposed in a number of publications [e.g. 5 ~ 15] and then used in all our application design work later [e.g. 16 ~ 21]. The advantages of this approach include the use of ACMs to separate mutually asynchronous timing domains and the existence of a highly organised methodology of design based on data requirements within the system. Isolating asynchrony to ACMs makes it possible for system designers to incorporate computational IPs with ease, and concentrating on data requirements at particular points of a network is much more "demand side" oriented than the current approach of assuming synchrony first and only later dealing with asynchrony by tolerating QoS reductions [13]. The proposed architecture for RTNoC and related in-depth high-level investigations completed this objective.

The project includes other work in this area. We investigated Petri nets and timing and metastability issues in asynchronous circuits [22 ~ 24] and studied similar application problems using related methods [25 ~ 27].

2.2. Development of design flow for RTNoC systems

This objective included two issues: The overall design flow for an RTNoC system and the design flows for components of an RTNoC system. We achieved significant results in both these aspects.

For the overall design flow for an RTNoC system, results from the research indicate that it is best to follow the MASCOT tradition [3, 4, 9, 13] and follow a top-down hierarchical approach, at each state starting from the point of data requirements at an ACM node. This conclusion is further reinforced by example systems [e.g. 18 ~ 21] and comparisons with other methods found in Real-Time Network design [28, 29].

For the design flows for components of an RTNoC system, our work concentrated on the data communication components (ACMs). This is because, like in general MASCOT systems, these form the basic framework of a Real-Time Network and are the closest related to data requirements at all levels of detail.

There were two aspects to this part of the research. One was fundamental research into general asynchronous systems and circuits synthesis [30 ~ 37]. This is a particularly important part of ACM hardware synthesis because turning ACM algorithms into hardware has been proven in COMFORT to be a non-trivial problem. One method, the direct mapping from Petri Net specification models to circuits based on David Cells, is the best suitable for ACMs. This is because on the one hand, for ACMs in a Real-Time Network, even in an on-chip setting, semiconductor real estate in the control part is unimportant because of the existence of much larger data paths. On the other hand the optimisations in standard logic synthesis methods tend to turn out unpredictable and irregular circuits [31, 33, 34].

The other aspect of this part of the research was the synthesis of ACM algorithms from functional specifications. We explored three different methods. One is the state space search technique where an entire set of statements are used to assemble a very large set of possible algorithms randomly. The set is then reduced by a process of elimination through a number of qualitative criteria and finally vigorous verification. This method used large amounts of computing power, which KU kindly provided without additional cost to the project budget. The result of this exercise was successful in that it did find all known working algorithms for a particular type of ACM. This work, proposed and carried out by D.A. Fraser at KU, is in the process of being formally reported and at present only generally introduced in [13].

The second method makes use of the Role Model technique developed by H.R. Simpson of MBDA who joined the project at KU. The advantages of the Role Model method include a saving of state space traversal efforts, which helps to clarify the picture in both ACM design and analysis. This synthesis method combines informed intuition with computerised steps and is most suitable for experts of ACMs [8, 38, 39].

The final method is the synthesis of ACM algorithms using Petri net based techniques. This method is highly systematic constituting a concrete set of algorithmic steps. Its needs for computation power and mid-process human interaction are relatively low. Therefore it is more suitable for system designers who are not familiar with the techniques employed inside ACMs [5, 6, 40 ~ 41, 42].

2.3. Development of a parameterized library of ACMs

A large proportion of our work was dedicated to this objective, which concentrated on enriching the knowledge of ACMs, from classification to functional specification [5, 6, 8, 39], from synthesis to verification to testing methods [6, 8, 43, 44, etc.], and from detailed hardware studies [34] to models and behavioural representations in application systems [19 ~ 21]. Although we also obtained a significant number of sound ACM algorithms [6, 8, 11, 15, 41, 45], this research achieved a much more comprehensive set of results than just a library of ACMs.

One component of this objective much expanded from what was anticipated in the project proposal was the development of novel hardware testing methods and time measurement techniques. This started with Dr O. Maevsky joining the project as a visiting research fellow, and culminated in Dr M.A. Abas' degree thesis work. With additional support and participation from Sun Microsystems the methods and techniques developed in this

part were proven using fabricated hardware devices [43, 44, 46 ~ 50]. Properties of ACM hardware include timing and metastability, previously non-testable after fabrication. This research resulted in the development of easy to use and reliable techniques for timing measurements. It also has significant application potential in the general field of asynchronous hardware testing, outside the immediate area of interest of this project.

The work again further expanded on the results from COMFORT in the area of ACM analysis and verification. Our methods of verification, based on intelligent state space traversals, have seen further development and maturation during COHERENT, and many previously unproved ACM algorithms were shown to be correct, and previously unknown behaviour details were found [6, 8, 38, 39, 45].

A parameterized library of ACMs for application system designers need to include high-level models. Project Postgraduate Student F. Hao developed systematic and algorithmic techniques whereby behaviour models of ACMs can be derived for the Matlab/Simulink environment. The results of this work successfully demonstrates that these techniques were suitable for finding usable and reliable Matlab/Simulink models of ACMs. Case studies have exposed previously unknown high-level behaviour of certain ACMs in a distributed control system environment [12, 15, 20, 21]. An MSc student working under the project, G.Y. Luo, developed techniques whereby ACMs models can be developed for use in the Network Simulator environment, thus pointing out the potential of supplying ACM libraries to computing network designers [17, 19].

2.4. Testing the RTNoC technology on real application system examples

This objective includes two related parts. At KU, project Ph.D. student M. Valera investigated applying Real-Time Network technology in vision surveillance systems and networks. At NU, F. Hao looked into applying Real-Time Network technology and hardware in real-time distributed control systems, at a lower, on-chip, level.

At KU, extensive work was carried out under COHERENT in designing security monitoring vision networks using Real-Time Network and MASCOT principles and methods. The result of this work demonstrated the advantages of the Real-Time Network approach by comparing it with previous system designs based on assumptions of synchrony as embedded in popular object-oriented approaches. For instance, at each data connection, instead of obligatory QoS compromises caused by unavoidable asynchrony, system designers using the Real-Time Network approach can provide the appropriate service starting from the point of view of data requirements [4, 9, 16, 18, 26, 51].

At NU, similar work in applying Real-Time Network principles and ACM-related techniques in distributed control systems resulted in confident predictions that certain types of ACMs provide the best approximation of an analogue wire [15, 20, 21]. We believe this is a significant result, pointing towards a potential direction of research in response to the CDS Panel's predictions about global asynchrony in future control systems.

2.5. Supporting tools development

A number of software tools were developed during the course of this project. Some of these resulted from the requirements of some of the other objectives. Some turned out to have relevance outside the immediate areas of interest of COHERENT. Others were more general purpose tools whose development the project helped with case study examples.

- **PN2DCS** is a general purpose software for designing and synthesizing asynchronous control circuits from Petri net specifications. This tool was first developed using an ACM as an example system, and has turned out to be particularly useful in deriving good ACM hardware from an algorithmic specification [34].
- **Petrify** is a popular synthesis tool for speed independent circuits from a Petri net based specification. It was shown to be not suitable for deriving ACM hardware in [34]. We have, however, through collaboration between NU and UPC (Barcelona), developed a modified version of Petrify targeting the synthesis of ACM algorithm Petri net models from a state-space specification [42]. This new modification of Petrify may turn out to be significant in deriving the algorithmic form models of sets of independent processes communicating through shared variable referencing.
- **Jabuti** is also the result of the NU/UPC collaboration. This tool complements the ACM targeting Petrify by deriving automatically a state-space behaviour model from a functional behaviour specification. Used together, these two tools will derive automatically an algorithm-like Petri net model for an ACM given a functional specification [42].
- **ACME** is software that generates candidate ACM algorithms from a description of available data storage and usable algorithm commands then tests and evaluate them to obtain a list of valid choices. It consists of a collection of modules developed at KU, and can be used in combination with the ACM2PN and Reach tools to automatically find usable and correct ACM algorithms.
- **ACM2PN** and **Reach** target the automatic verification of ACM algorithms based on Petri net modelling and analysis techniques. They now incorporate Role Model related state space visualization.

2.6. Research Output

Overall, the project has resulted in contributions to 15 journal papers, three book chapters, 30 conference papers, of which 23 were peer-reviewed and nine were in major IEEE conferences such as ASYNC, DATE, ACSD, etc., three Ph.D theses (not counting the two Ph.D. theses by the project students M. Valera and F. Hao, which are in the writing-up stage), two tutorials, four invited lectures, two technical reports, and six tools.

3 Management, organisation and collaboration

The overall management method followed the one successfully adopted for COMFORT. Meetings of the KU and NU teams were held alternately in Kingston and Newcastle on a regular basis, and attended by the two industry partners from MBDA (H.R. Simpson, E. Campbell). These meetings were used both as progress and planning meetings and as a forum for technical presentations. Other, more "impromptu", meetings were organized between the teams and industry partners when technical issues needed to be discussed.

Two events outside the control of the research teams occurred near the start of the research. 'Restructuring' of Electronic Engineering at KCL led to the whole team there (with various other researchers) moving to the Digital Imaging Research Centre (DIRC) at KU in month three, and at NU, the team (and others) were transferred from the Department of Computing Science to the School of Electrical, Electronic and Computer Engineering. The application to CCTV surveillance part of the work was substantially strengthened as a result of the move to KU, because of existing work and interests of DIRC.

The project Post Graduate student at KU (M. Valera Espina) focussed her research on design methods for distributed CCTV surveillance systems (a major research interest of DIRC at KU). She received substantial supervision from one of the industry partners (H.R. Simpson, who was appointed Visiting Professor at KU and continued to be Visiting Professor at NU during the project), and she was also given access to MBDA proprietary software tools which support system design by the MASCOT method. The project Post Graduate student at NU (F. Hao) investigated the application of RTNoC technology to distributed control systems and received valuable guidance from both MBDA industry partners.

MBDA participated actively throughout the project. Technical discussions between the academic and industrial partners benefited both significantly. H.R. Simpson's high-quality journal publications are just a part of the significant contributions made to this project by the MBDA colleagues. This collaboration has laid the foundations for future cooperation, with MBDA continuing to be a formal partner of Next Generation Of Interconnection Technology For Multiprocessor SoC (EP/C512812/1) at NU.

NU provided a university visiting research fellowship (funded by the university) for Dr O. Maevsky to work within COHERENT for six months. This fruitful collaboration resulted in several project publications and formed the basis of the collaboration with Sun Microsystems (below). Future close collaboration in this area with Dr Maevsky, who is now with Intel Labs Moscow, is envisioned.

Sun Microsystems were very kind to provide material help and technical expertise, at no cost to the project, in the fabrication of hardware related to this project's keen interest in the area of metastability and timing in asynchronous systems. This allowed us to develop novel ways of measuring timing in asynchronous hardware and also benefited Sun in their quest in the area of asynchrony.

S.A. Velastin at KU conceived, organised and chaired the IEE's International Symposium on Distributed Surveillance Systems (IDSS-03 and IDSS-04), through which the ideas on the suitability of asynchrony for surveillance systems were disseminated and potential collaborative links within the EU identified.

The KU PI (A.C. Davies) had several additional opportunities for discussions with the NU team, as a result of visiting NU for other reasons (lecturing to MSc students, PhD examining, and committee meetings for the EPSRC PREP conference).

The NU and KU teams worked very closely throughout the project. I.G. Clark worked at both sites and F. Xia, a member of the NU team, was sponsored by the KU side to attend ACSD 2004. Numerous project publications are co-authored by members of both teams.

NU's collaborations with Prof J. Cortadella's group at UPC (Barcelona) produced significant developments to the Petrify tool to suit ACM-type systems and the development of the new tool Jabuti. NU hosted a week-long academic visit by UPC Ph.D. student K. Gorgonio during this work.

Both project Ph.D. students have produced high-quality research work, as shown by their contributions to numerous publications, including journal and peer-reviewed international conference papers. Apart from their nominal supervisors, other members of the teams also provided frequent help towards their training. Several MSc students at NU also made contributions to the project through tool development and research publications (especially in the case of G.Y. Luo). F. Hao also gained invaluable experience from supervising the work of some of these students.

Both project RAs made contributions to COHERENT in addition to carrying out research resulting in their co-authoring many of the project publications. I.G. Clark was webmaster for the School of EECE at NU in his spare time and used his expertise to develop and maintain the group and project websites (http://async.org.uk/ and http://async.org.uk/coherent/). Both he and F. Xia conducted international lectures, tutorials and invited talks on the research of the project. F. Xia participated in teaching a number of relevant modules at MSc level at NU on asynchrony and ACM related issues. He also contributed to the supervision of Dr D. Shang's PhD work. Both RAs also co-authored a number of research project proposals, including the eventually successful Next Generation Of Interconnection Technology For Multiprocessor SoC (EP/C512812/1) at NU.

4 Explanation of expenditure

The expenditure plans in the original proposal have been followed without significant changes. The biggest change was the reallocation, at NU, of some of the consumables budget (chip fabrication) in order to cover the shortfall on salaries and travel. We decided to spend that budget to pay the salary of our key RA, F. Xia, for

extra three months, in order to retain him until there had been an appropriate appointment made available for him within the School. During that extra period F. Xia was able to complete an important part of the COHERENT research, which resulted in a paper submitted to ACSD'05. The extra travel costs were necessary to support our high conference activity, for example to support Mr. G.Y. Luo and Dr. O. Maevsky, whose contributions to this project were highly beneficial and whose main funding came from alternative sources. On the other hand, during the course of the project we received a kind offer from Sun Microsystems to fabricate without charge our demonstrator chip for time measurement, which made the above reallocation a cost-effective measure.

Project publications (a complete list can be found at http://async.org.uk/coherent/)

[1] A.C. Davies. "An overview of Bluetooth Wireless Technology™ and some competing LAN Standards", Invited Plenary Lecture, Proc. of 1st IEEE International Conference on Circuits and Systems for Communications, St Petersburg, Russia, 26-28 June 2002. pp 206-211.

[2] A.C. Davies, "Bluetooth, Zigbee and other low-cost WLAN standards", Invited Tutorial, EUNICE Summer School, Balatonfured, Hungary. Sept. 2003.

[3] Rosa del Carmen Munoz-Calanchie. "Using LOTOS for the Analysis of MASCOT Designs". Ph.D. Thesis, University of London, King's College London, June 2002.

[4] M. Valera, S.A. Velastin. "An approach for designing a real-time intelligent distributed surveillance system". IEE Symp. on Intelligent Distributed Surveillance Systems., 26th February 2003 London.

[5] Fei Xia, Alex V. Yakovlev, Ian G. Clark, Delong Shang. "Data Communication in Systems with Heterogeneous Timing", MPCS'02, Euromicro, 10-12 April 2002, Ischia, Italy.

[6] Fei Xia, Alex V. Yakovlev, Ian G. Clark, Delong Shang. "Data Communication in Systems with Heterogeneous Timing", IEEE Micro, Vol. 22, Part 6 (2002), pp. 58-69.

[7] Ian G. Clark, Fei Xia, Alex V. Yakovlev, Delong Shang. "Data Communication Mechanisms for Systems with Heterogeneous Timing". Invited paper at the 2003 Heterogeneous Computer Systems Workshop, University of South Australia, Adelaide. 27th February 2003.

[8] H.R. Simpson, "Protocols for process interaction". Proc. IEE on CDT, 150, (3), pp 157-182, May 2003.

[9] M. Valera, S.A. Velastin. "Real-time Architecture for Large Distributed Surveillance Systems", IEE Intelligent Distributed Surveillance Systems, IEE, February 2004, IEE Savoy Place, London. pp. 41-45.

[10] Fei Xia, "Asynchronous Data Communication Mechanisms", invited lecture, Tsinghua University, Beijing, April 2004.

[11] H. Simpson, E. Campbell, F. Xia, I. Clark, A. Yakovlev, D. Shang. "Further discussions on the classification and high-level models of ACMs", NCL-EECE-MSD-TR-2004-102, Microelectronic System Design Group, School of EECE, University of Newcastle upon Tyne, June 2004.

[12] Fei Xia, Fei Hao, Ian G. Clark, Alex Yakovlev, E. Graeme Chester. "Buffered Asynchronous Communication Mechanisms", ACSD 2004, Hamilton, Ontario, Canada, 16-18 June 2004, pp.36-46.

[13] F. Xia, I. Clark, A. Yakovlev, "Asynchronous Data Communication Mechanisms", half day tutorial, REASON (Research and Training Action for Systems on Chip Design) Tutorial Day on Systems on Chip Design, DSD'2004, Rennes, France, August 2004.

[14] Anthony C. Davies. "Communications Protocols and Mechanisms for Distributed Digital Systems", Jubilee Conference 1879-2004, Budapest Tech Polytechnical Institution, pp. 343-350, Budapest September 2004.

[15] Fei Xia, Fei Hao, Ian G. Clark, Alex Yakovlev, Graeme Chester. "Buffered Asynchronous Communication Mechanisms", Invited paper, submitted, Fundamenta Informaticae, IOS Press.

[16] Maria Valera Espina, Sergio Velastin. "Design method for real-time intelligent distributed wide-area surveillance system", PREP 2004, Poster presentation, University of Hertfordshire, 5-7 April 2004.

[17] G.Y. Luo, I.G. Clark, F. Xia, A.M. Koelmans, A.V. Yakovlev. "Simulating Hets in NS for developing an ACM transport protocol for Networks-on-Chip", PREP 2004, University of Hertfordshire, 5-7 April 2004.

[18] M. Valera, S.A. Velastin. "Real-Time Networks to design a distributed architecture for large real time surveillance systems", SCI2004, Florida, US, 18-21 July 2004

[19] G.Y. Luo, F. Xia, I.G. Clark, A.M. Koelmans, A.V. Yakovlev. "Simulating Heterogeneously Timed Networks in Network Simulator NS", CSNDSP 2004, University of Newcastle, UK, 20-22 July 2004.

[20] F. Hao, F. Xia, E.G. Chester, A. Yakovlev, I.G. Clark. "MATLAB Models of ACMs in Control Systems", ICINCO-2004, INSTICC Press, pp. 54-61, Volume 3, Setubal, Portugal, 25-28 August 2004.

[21] Fei Hao, Fei Xia, Graeme Chester, Alex Yakovlev. "An ACM Application in Broom Balancer", 1st UK Embedded Forum, ESS, NEC, Birmingham, UK, 13-14 October 2004.

[22] A. Yakovlev. "Is the Die Cast for the Token Game?", Invited paper, ICATPN 2002, Adelaide, Australia, 24-28 June 2002. LNCS 2360, pp70-79, Springer Verlag.

[23] D.J. Kinniment and A.V. Yakovlev. "Low latency synchronisation through speculation", In E. Macii, O.G. Koufopavlou, V. Paliouras (Eds.): Integrated Circuit and System Design, Power and Timing Modeling, Optimization and Simulation; PATMOS 2004, Santorini, Sept. 2004, LNCS 3254, Springer, pp. 278-288.

[24] David Kinniment. "Synchronizers and Arbiters OR 1000 years of indecision". 14th UK Asynchronous Forum, Newcastle upon Tyne, 30th June and 1st July 2003.

[25] A. Yakovlev, S. Furber, R. Krenz, A. Bystrov. "Design and Analysis of a Self-timed Duplex Communication System", IEEE Transactions on Computers, Vol. 53, No.7, pp. 798-814, July 2004.
[26] S.A. Velastin, B. Boghossian, B. Lo, J. Sun, M.A. Vicencio-Silva. "PRISMATICA: Toward Ambient Intelligence in Public Transport Environments", IEEE Trans. on SMC, Part A, Vol. 35, Issue 1, pp 164-182, January 2005.
[27] S. Dasgupta, A. Yakovlev. "Modelling and verification of globally asynchronous and locally synchronous ring architectures", to appear in DATE 2005, Munich, March 2005.
[28] M. Valera, S A Velastin. "Intelligent distributed surveillance systems: A Review", Spec. Issue on Int. Distributed Surveillance Systems, Proc IEE on Vision, Image, and Signal Processing (to appear in 2005).
[29] M. Valera, S. Velastin. "A Review of The State-of-The-Art in Distributed Surveillance Systems" in Intelligent Distributed Surveillance Systems, S.A. Velastin and P Remagnino (Eds), IEE Publications (to be printed in 2005)
[30] Delong Shang, Fei Xia, Alex Yakovlev. "Asynchronous Circuit Synthesis via Direct Translation: New Developments", Technical Report No. CS-TR-748, Dept. Compt. Sci., Newcastle University. October 2001.
[31] A. Yakovlev, F. Burns, A. Bystrov, A. Koelmans, R. Krenz, D. Shang. "Behavioural synthesis of asynchronous controllers: a case study with a self-timed communication channel", 2nd ACiD-WG Workshop, European Commission's Framework 5 Programme, Munich, Germany, 28-29 January 2002.
[32] J. Cortadella, M.Kishinevsky, S.M. Burns, K.S. Stevens, A. Kondratyev, L. Lavagno, A. Taubin, A. Yakovlev. "Lazy Transition Systems and Asynchronous Circuit Synthesis with Relative Timing Assumptions". IEEE Trans. on CAD, Vol. 21, No. 2, Feb. 2002, pages 109-130.
[33] Delong Shang, Fei Xia, Alex Yakovlev. "Asynchronous Circuit Synthesis via Direct Translation", ISCAS 2002, IEEE Int. Symp. on Circuits and Systems, Scottsdale, Arizona. 26-29 May 2002. Vol. 3, pp. 369-372.
[34] D. Shang, "Asynchronous Communication Circuits: Design, Test and Synthesis", Ph.D. Thesis, University of Newcastle upon Tyne, April 2003.
[35] M. Renaudin and A. Yakovlev. "From Hardware Processes to Asynchronous Circuits via Petri Nets: an Application to Arbiter Design", Proc. Workshop on Token Based Computing (ToBaCo2004), satellite to 25th Int. Conf. on Appl. and Theory of Petri nets, Bologna, Italy, 22 June 2004, pp. 59-66.
[36] D. Sokolov, A. Yakovlev. "Clock-less circuits and system synthesis", Proc IEE on CDT, to appear in 2005.
[37] D. Shang, F., Burns, A. Koelmans, A. Yakovlev, F. Xia, "Asynchronous system synthesis based on direct mapping using VHDL and Petri nets", Proc IEE on CDT, Vol.151, No.5, May 2004, pp.209-220.
[38] H.R. Simpson, "Freshness specification for a class of asynchronous communication mechanisms". Proc IEE on CDT, 151, (2), pp 110-118, March 2004.
[39] H.R. Simpson. "Data Transfer Analysis for a Pair of Asynchronous Communication Algorithms", Proc IEE on CDT, Accepted for publication.
[40] A. Yakovlev, F. Xia. "Towards Synthesis of Asynchronous Communication Algorithms", in 'Synthesis and control of discrete event systems', part I: Decentralized systems & control. Eds. Benoit Caillaud, Philippe Darondean, Luciano Lavagno, Xiaolan Xie. Kluwer Academic Publishers, Boston, January 2002. pp 57-75.
[41] F. Hao, A. Yakovlev, E.G. Chester, F. Xia, I.G. Clark, D. Shang. "Implementation of a three-slot signal ACM". Poster presentation at PREP 2003 - Postgraduate Research Conference in Electronics, Photonics, Communications and Software. 14-16 April 2003, University of Exeter.
[42] Jordi Cortadella, Kyller Gorgonio, Fei Xia and Alex Yakovlev, "Automating Synthesis of Asynchronous Communication Mechanisms", submitted to ACSD 2005.
[43] D.J. Kinniment, O.V. Maevsky, A. Bystrov, G. Russell, A.V. Yakovlev. "On-chip test for timing conditions", Second ACiD-WG Workshop of the European Commission's Fifth Framework Programme, Munich, Germany, 28-29 January 2002.
[44] D.J.Kinniment, A. Bystrov, A.V. Yakovlev. "Synchronization Circuit Performance", IEEE Journal of Solid-State Circuits, vol. 37, no. 2, Feb. 2002, pp. 202-209.
[45] Fei Xia, Ian Clark. "Algorithms for Signal and Message Asynchronous Communication Mechanisms and their Analysis", Volume 50, Number 2 (2002), pp.205-222, Fundamenta Informaticae, IOS Press.
[46] D.J. Kinniment, O. Maevsky, A. Bystrov, G. Russell, A. Yakovlev. "On-chip Structures for Timing Measurements and Test", Proc. ASYNC'02, Manchester, April 2002, IEEE CS Press. pp.190-197.
[47] O. Maevsky, D.J. Kinniment, A.Yakovlev, A. Bystrov. "Analysis of the oscillation problem in tri-flops", ISCAS 2002, Scottsdale, Arizona. 26-29 May 2002. Volume 1, pp. 381-384.
[48] D.J. Kinniment, E.G. Chester. "Design of an On-Chip Random Number Generator using Metastability", The 28th European Solid-State Circuits Conference (ESSCIRC) 2002, 24-26 Sept. 2002, Florence, Italy.
[49] D.J. Kinniment, O.V. Maevsky, A. Bystrov, G. Russell, A.V. Yakovlev. "On-chip structures for timing measurement and test", Microprocessors and Microsystems, Vol. 27, No. 9, October 2003, pp. 473-483.
[50] M.A. Abas, "A New Methodology of an On-Chip Time Measurement Circuit for High-Speed Digital Testing Applications", Ph.D. Thesis, University of Newcastle upon Tyne, Nov. 2003.
[51] S.A. Velastin, B.P.L. Lo and J. Sun. "A Flexible Communications Protocol For A Distributed Surveillance System", Journal of Network & Computer Applications, Elsevier, Vol. 27/4, 2004, pp 221-253.