Potential impact of emerging System-in-Package technologies on system design

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IMEC

Workshop W2 - Date2006

Future interconnects and networks on chip

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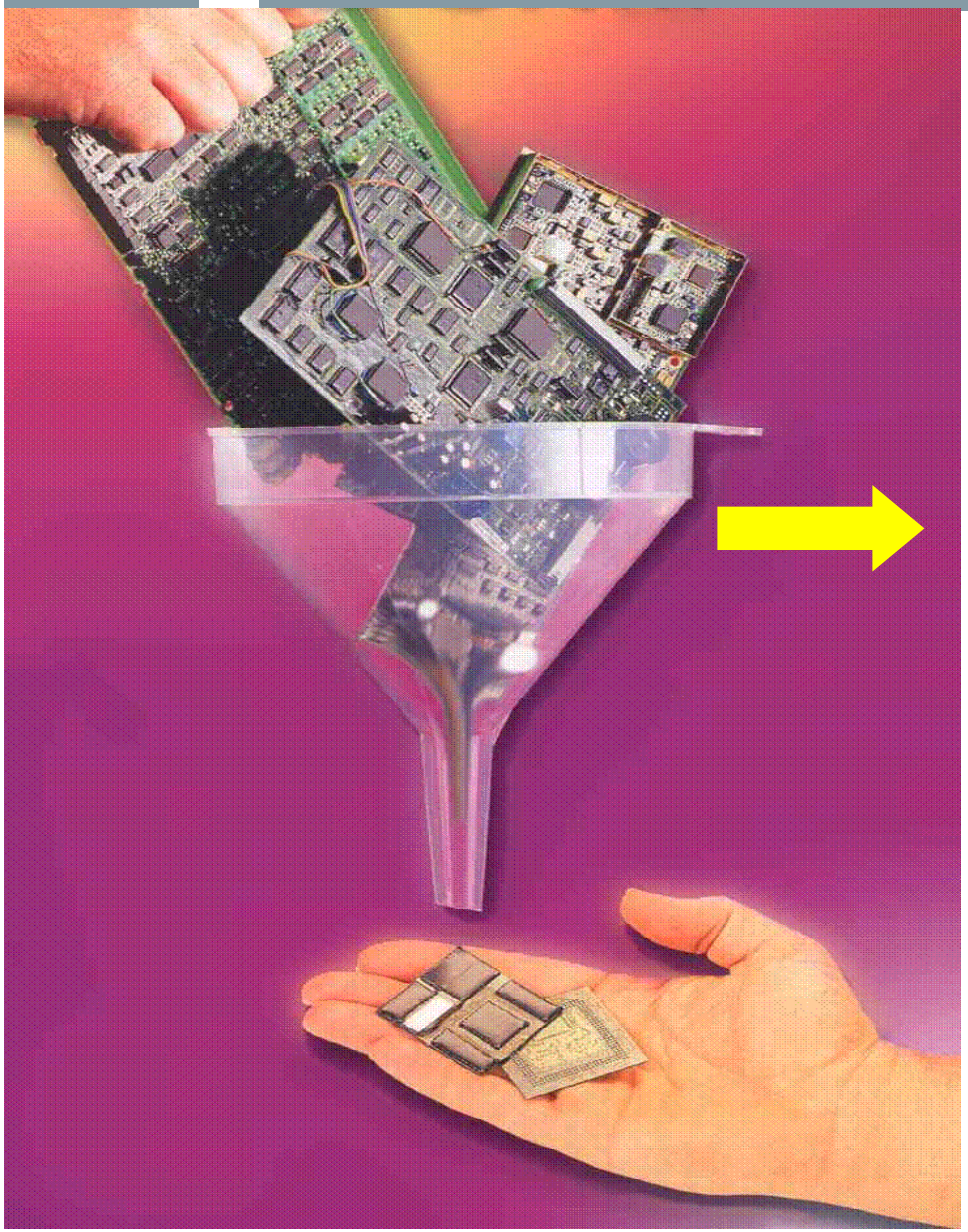
ICM Munich, Germany

Strategy drivers
High Density Interconnection and Packaging

- **IC technology roadmaps: "System on chip", SOC**
  - **"Vertical scaling" :**
    - **Density: High I/O density (more I/O's on smaller area)**
      High speed (digital & rf), high power density
    - **New materials: Cu/low k**
  - **"Horizontal scaling" : Divergence among Si-technologies :** specific technologies for Logic, Memory, mixed-signal, analog, rf, high voltage, high power,… + MEMS
- **"System roadmaps: "System-in-a-Package", SIP**
  - **One system = multiple die : "Horizontal scaling"**
  - **Systems consist of many non-silicon components :** Passives, Displays, sensors, antennas, connectors, …
  - **Need for miniaturisation :** 2D ultra thin ↕ ↘ 3D eCube

⑤ **"System-in-a-Package", SIP =** ***Multiple components on a high density interconnect substrate, realizing a (sub)-system function***

Miniaturisation of Electronic Systems



Enabling Technologies :

- Si-integration : SOC
- High Density Interconnection technologies

  SIP – “System-in-a-package”

SIP-design

Today :

"small PCB design" : adapted PCB design tools, traditional design flow. IC's and net list fully defined before the actual SIP design.

Limitations :

- No system-level optimization
- Complex wiring schemes
- Values passive components not optimum for SIP implementation
- …

SIP-design

Required :

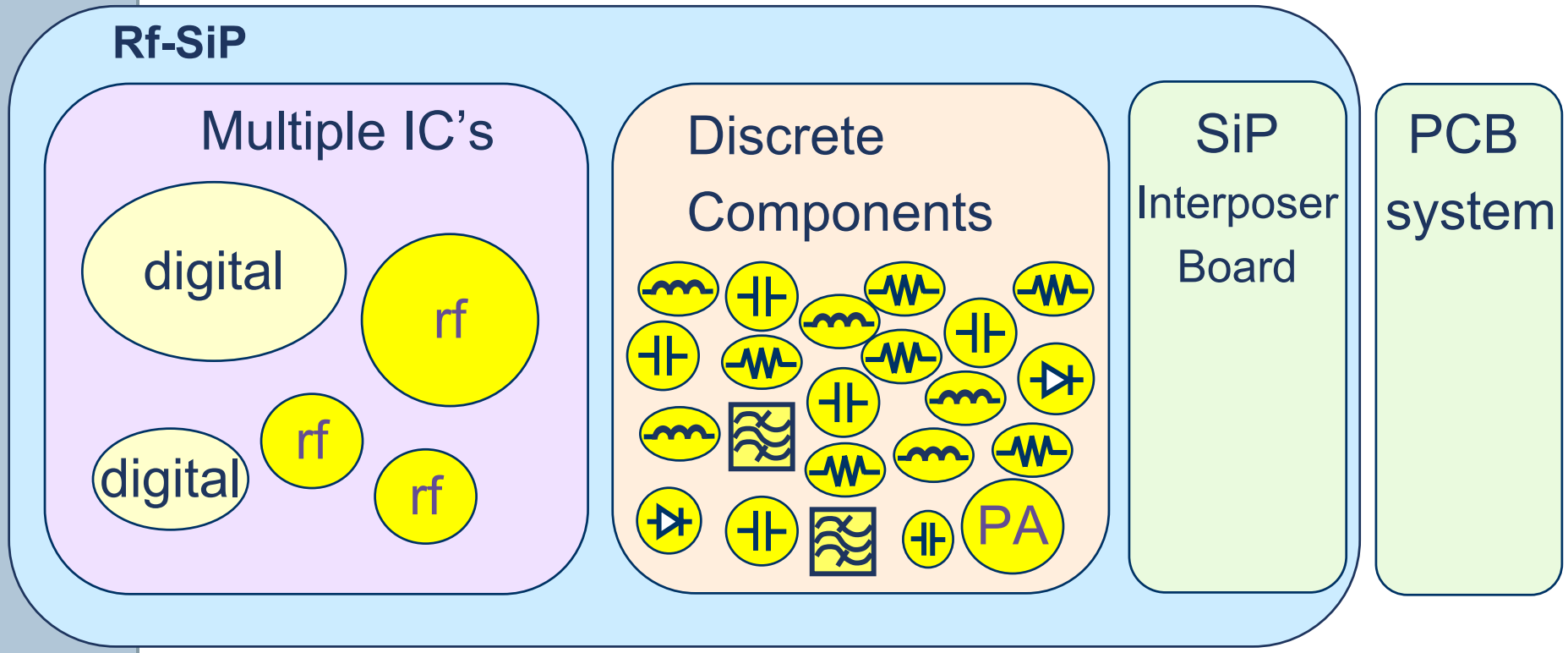
Chip-package co-design

Examples :

- rf-SIP
- 3D stacked SIP
- 3D stacked IC's

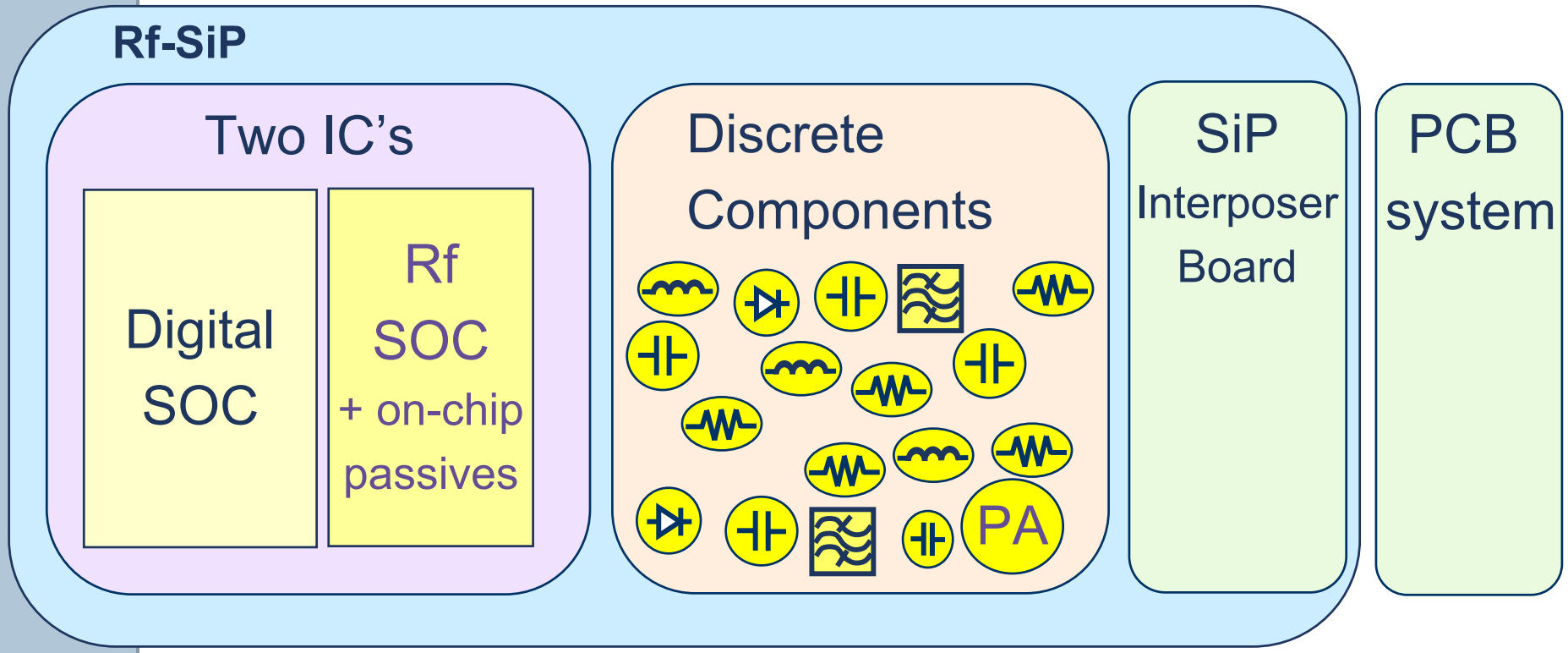
Rf integration schemes

Rf-SiP integration schemes : board level version



Rf integration schemes

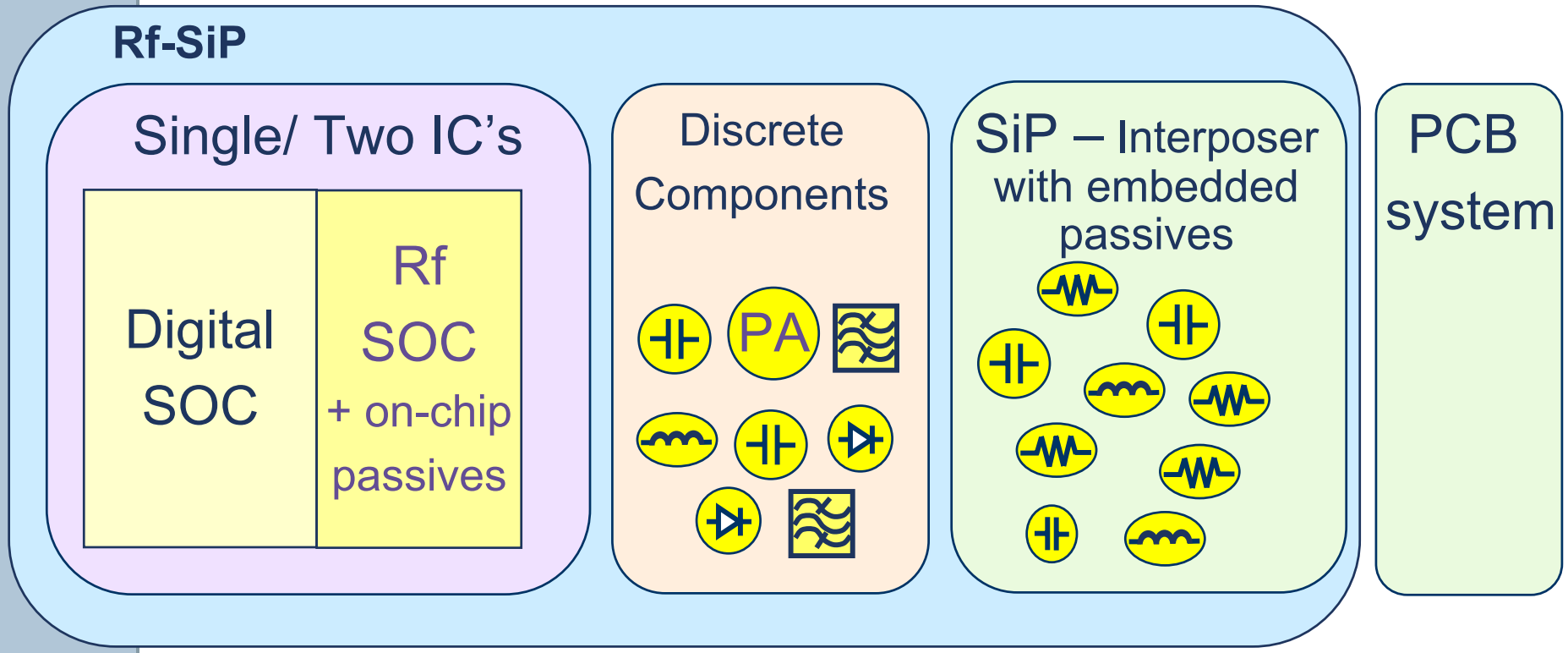
Rf-SiP integration schemes : SOC technology



Rf integration schemes

Rf-SiP integration schemes :

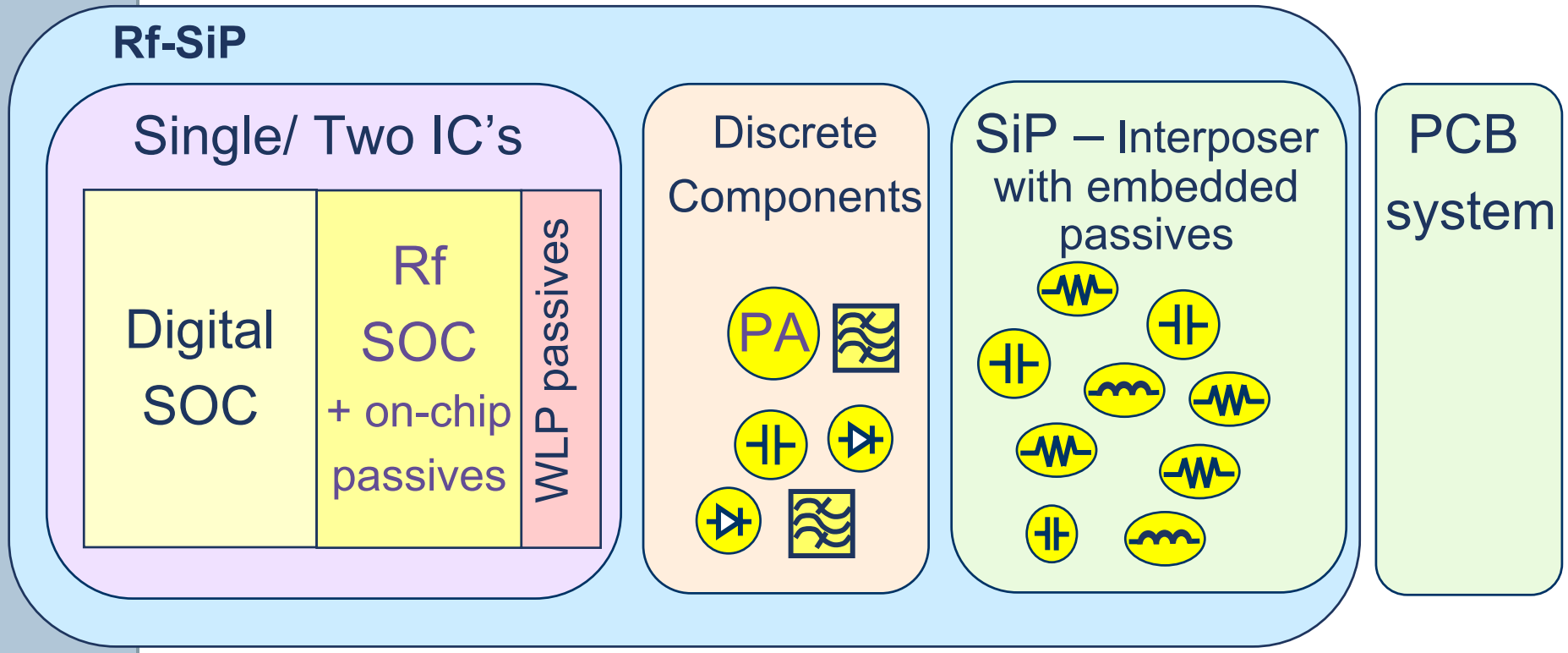
Embedded passives in interconnect Board



Rf integration schemes

Rf-SiP integration schemes :

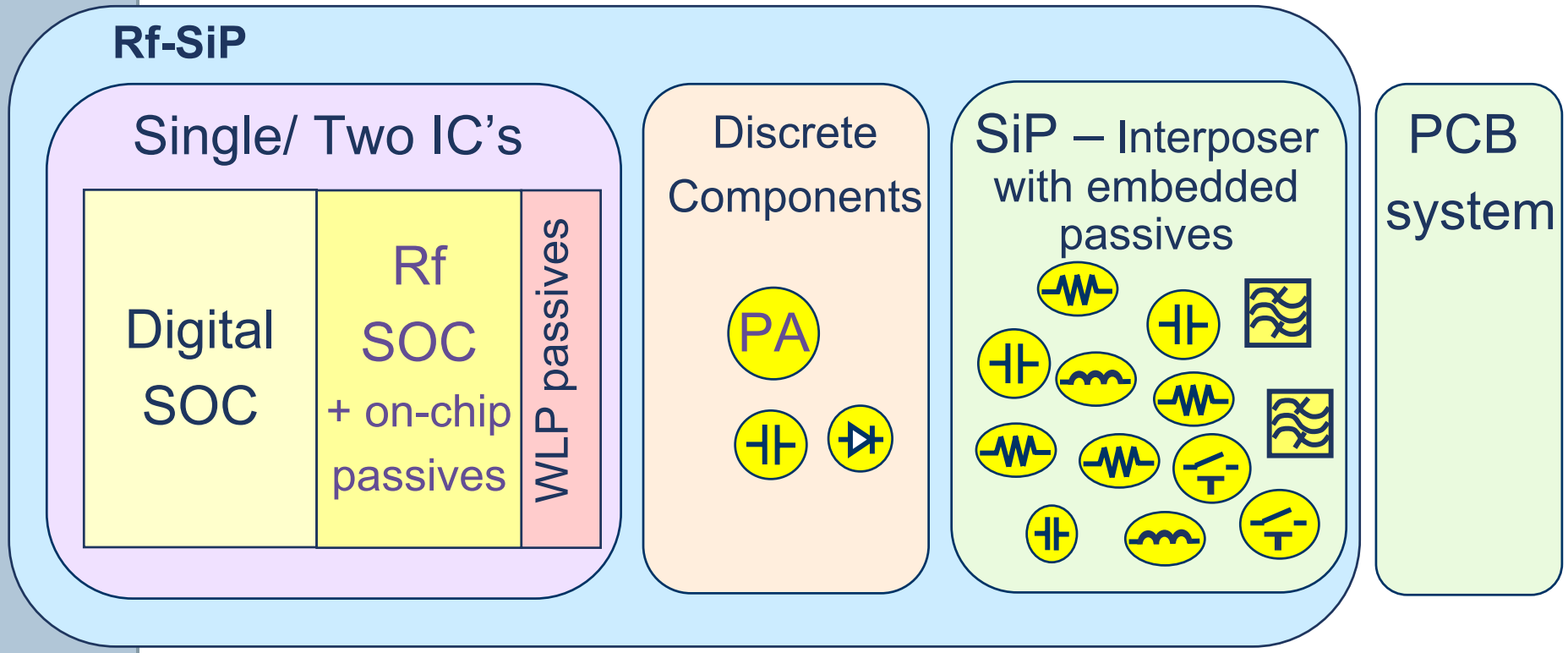
"above-IC" WLP passive integration



Rf integration schemes

Rf-SiP integration schemes :

rf-MEMS integration in embedded passives board



Technology requirements for rf-SiP

Integration of passive components in the SiP interconnect substrate

- **Which technology to choose?**
  - Laminate based : PCB, flex
  - Ceramic based, low temperature cofired ceramic, LTCC
  - Thin film lithography based
- **Use of different technologies together?**
- **Partial integration on the rf- chip?**

➘ **Partitioning of the system is key !!**

SIP Interposer Technology with Integrated Passives

Multilayer thin film offers:

- Wafer-level Processing
- Photo-lithography defined features:
  - Excellent control over lateral dimensions
  - High repeatability
  - High degree of miniaturization
- Thin film deposited resistor & dielectric layers:
  - High density
  - High precision, repeatable, small tolerances
- MMIC design style possible

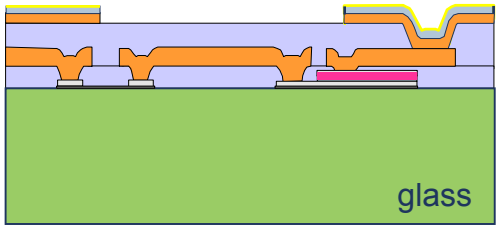
Substrate choice:

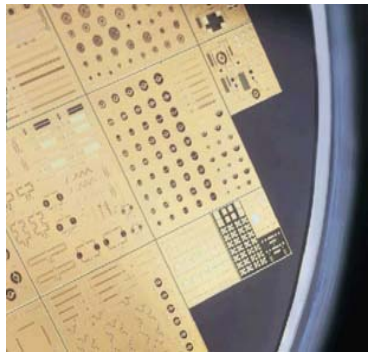
- AF45 Glass
- HR-Si : thermal advantages, Micro-machining capabilities (cavities, through-hole vias)

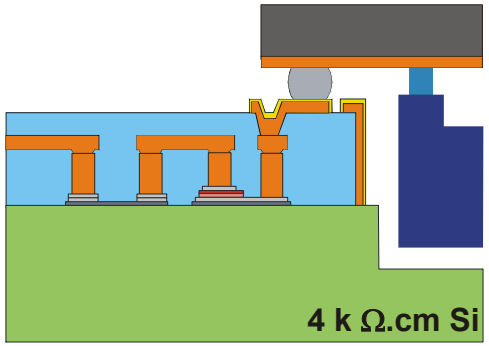
Multilayer Thin Film with Integrated Passives

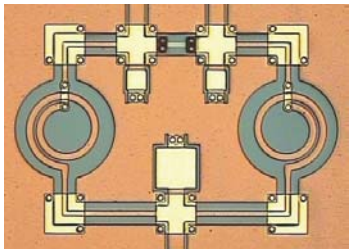
Main features :

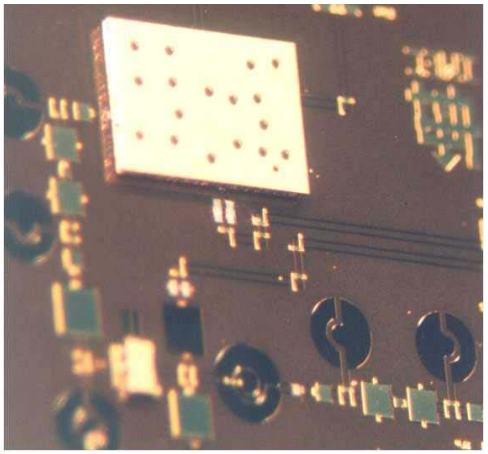
- Coplanar and microstrip lines
- Electroplated Cu lines (3-5 μm)
- BCB dielectric layers
- Resistors : TaN (25 Ω/□),
- Capacitors : Ta_2O_5 (0.72 nF/mm^2) & BCB (6.5 pF/ mm^2)
- Al resistor and capacitor contacts
- Inductors : up to 80 nH, Q : 30-150

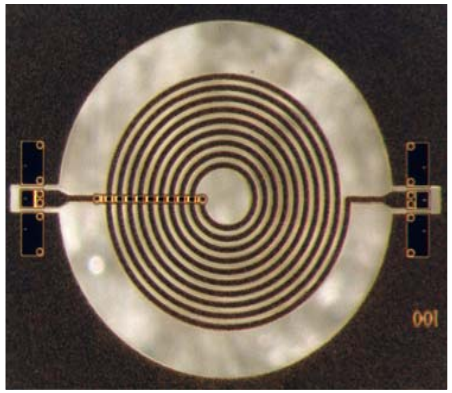


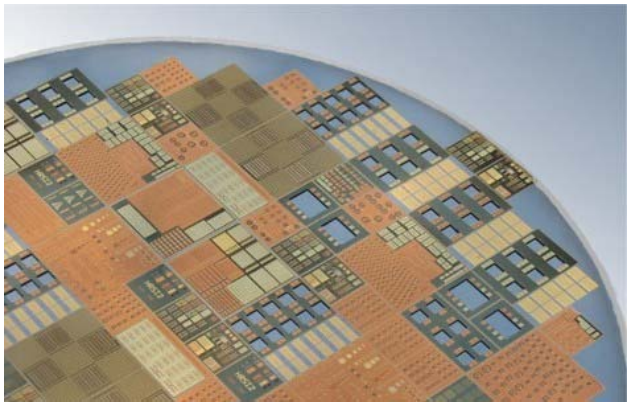




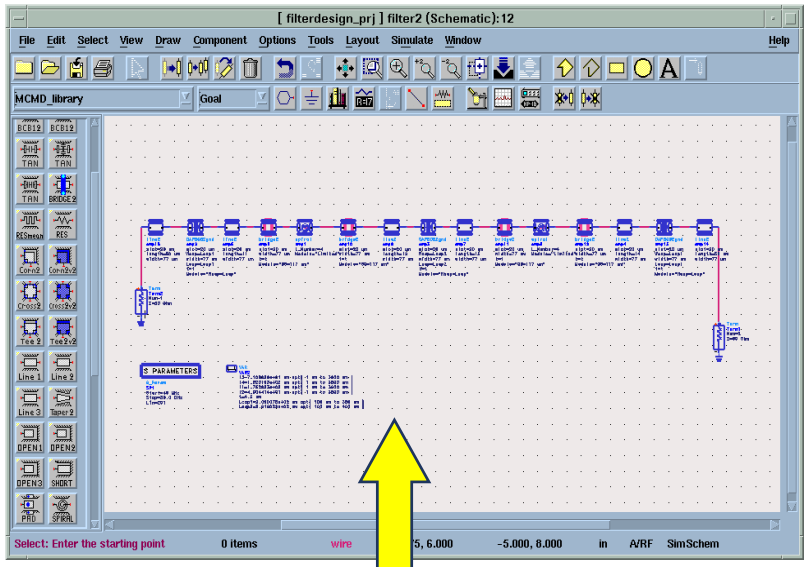


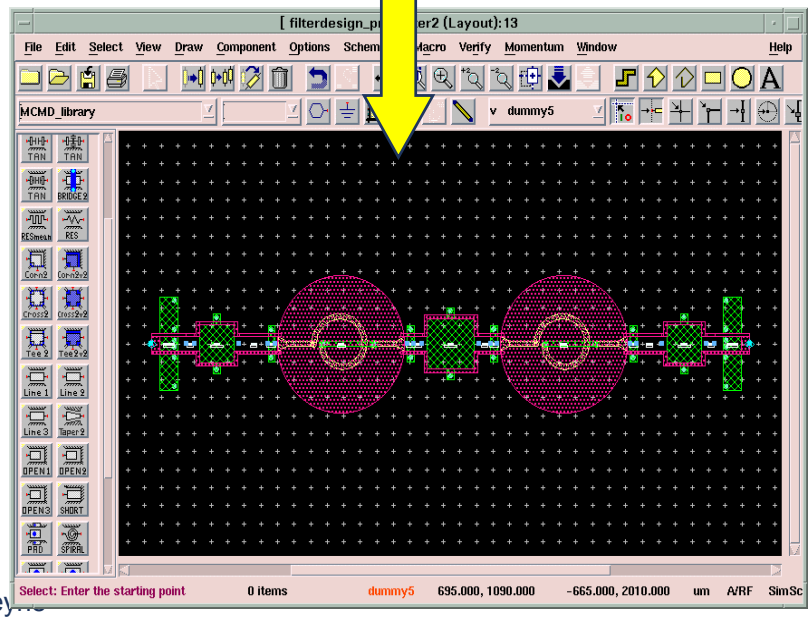


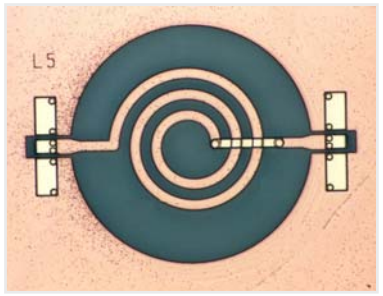


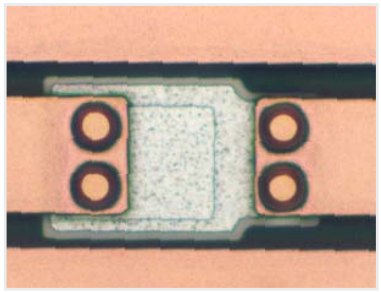


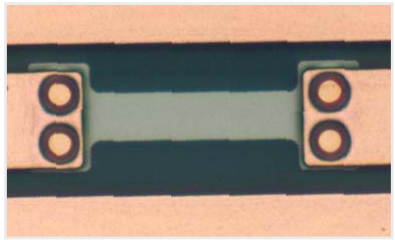
Multilayer thin film with integrated passives

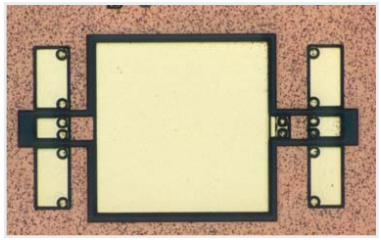


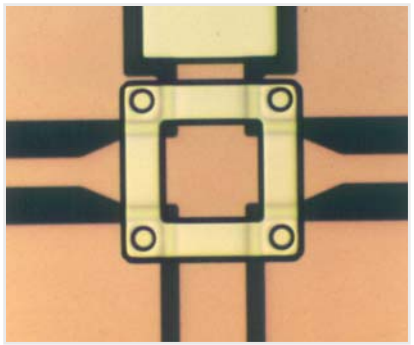




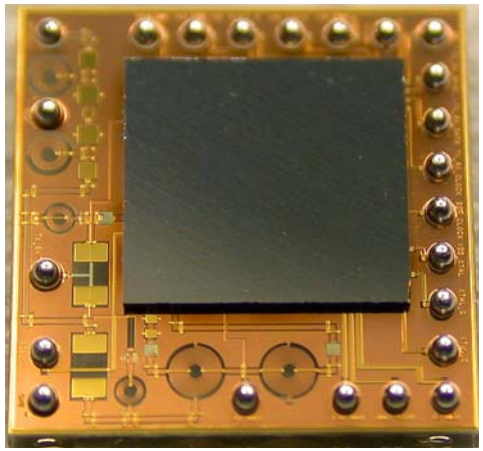




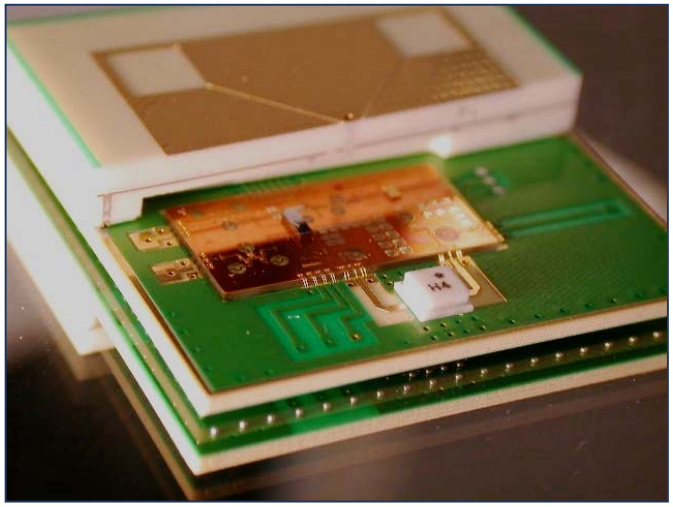




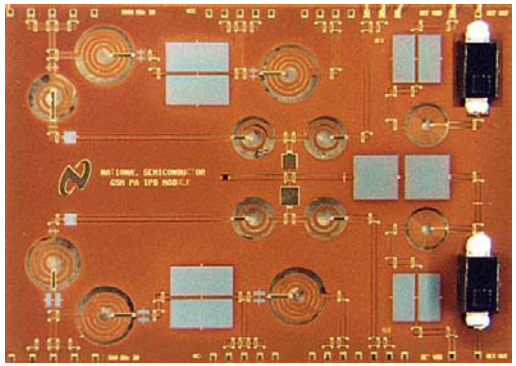
Multilayer thin film with integrated passives
Circuit implementations examples



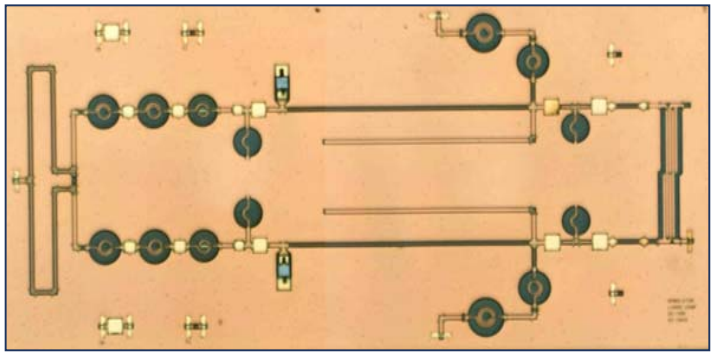
Blue-tooth Rf circuit
7x7 mm CSP package



RF section WLAN receiver - 5.2 GHz
With integrated antenna BGA package



Integrated Passive device
multiband cell phone Amplifier



Sub-harmonic QPSK modulator
LO @ 7 GHz, RF @ 14 GHz

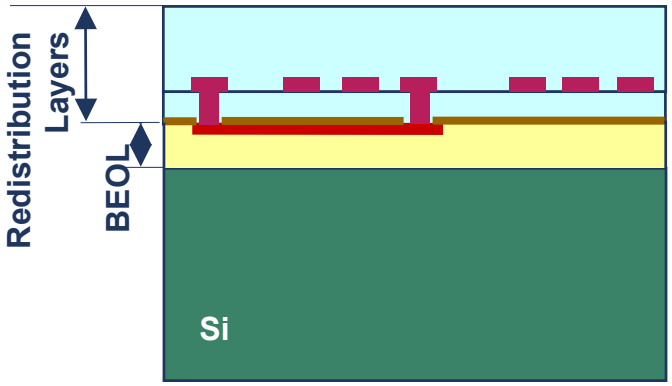
High Q on chip Inductors

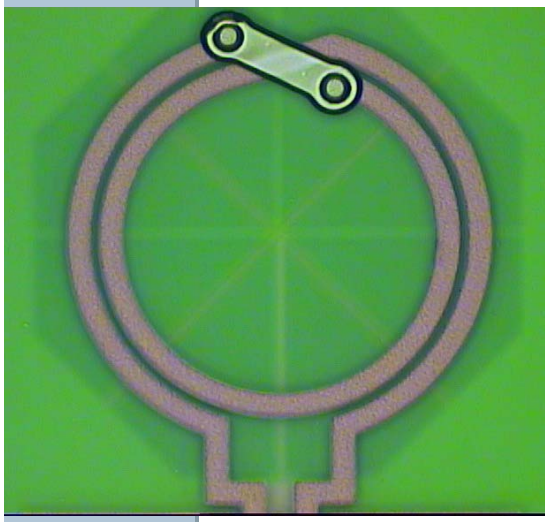
Main Limitations on chip Inductors :

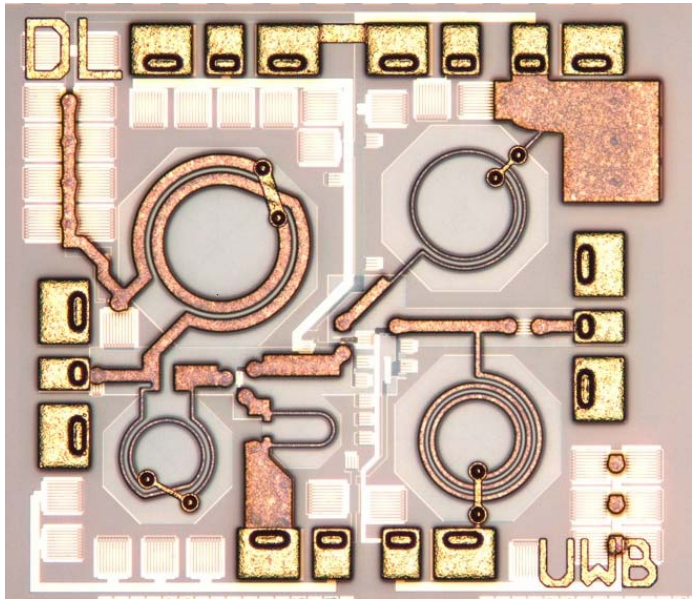
- High resistivity conductors (low L/R)
- High loss in silicon substrate

"Above-IC" processing inductors using multilayer thin film technology:

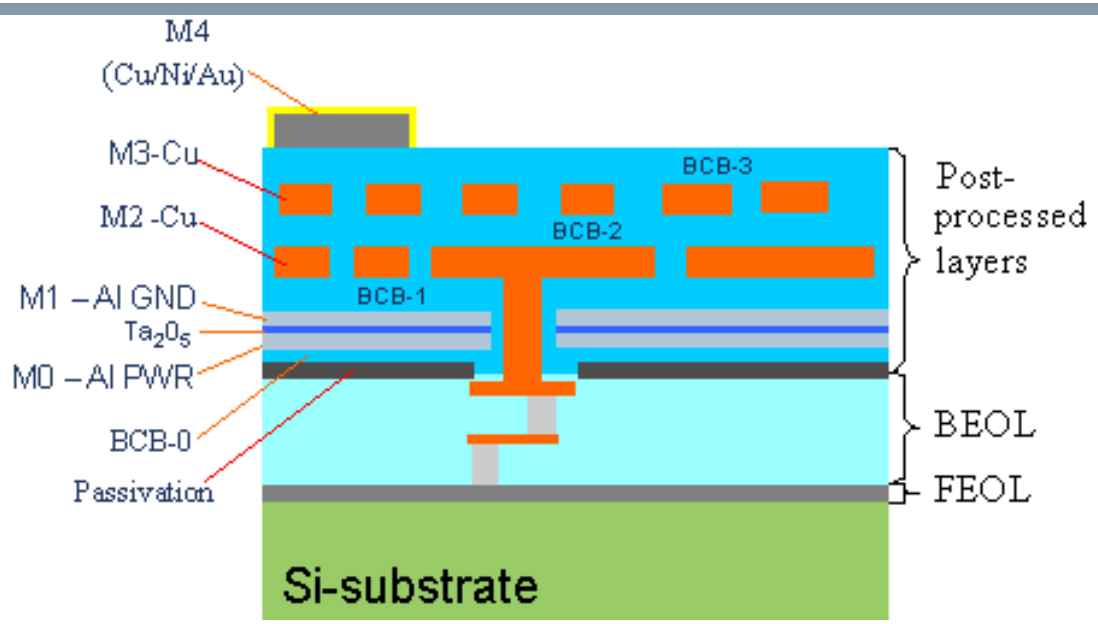
- **Thick Cu (up to 10 μm) : high L/R**
- **Larger distance to the Si-substrate: lower substrate losses and lower parasitic capacitances**





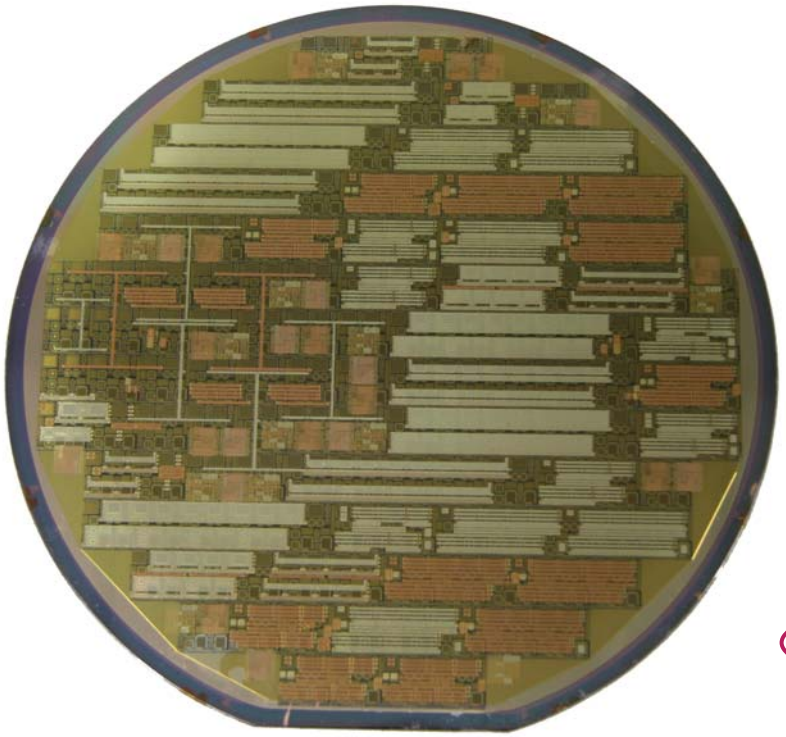


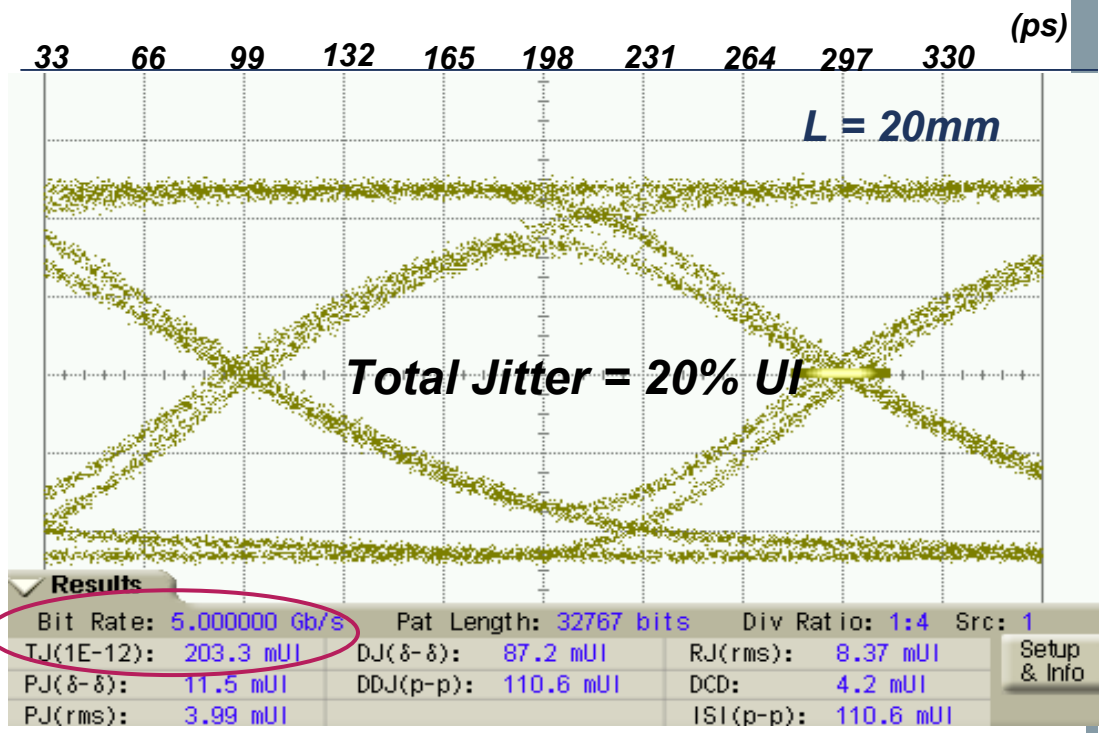
"Above IC" high speed digital interconnect routing using multilayer thin film technology



- 2 Signal routing layers : 3 μm thick Cu
  - Low-k BCB ILD (ε_r = 2.65) : 5 μm thick
  - BCB-0 only in Multi project Wafers : 1 μm thick
- Low impedance Power and Ground planes :
  - 1 μm thick Al
  - High-k dielectric Ta_2O_5 (ε_r = 25) : 100nm thick, resulting in a 1nF/mm^2 decoupling capacitor (scalable to 10nF/mm^2)
- Contact pads in M4

Differential driver-receiver achieves bit rate of 5Gbps on 0.35 µm CMOS





"above-IC" post processing
0n Europractice AMIS
0.35 µm CMOS MPC wafer

- **80% Eye opening @ 5Gbps**
- ***Low power:* 26.4mW → 5.3pJ @ 5 Gbps**
- **Similar results for microstrip and IMPS**

SIP-design

Required :

Chip-package co-design

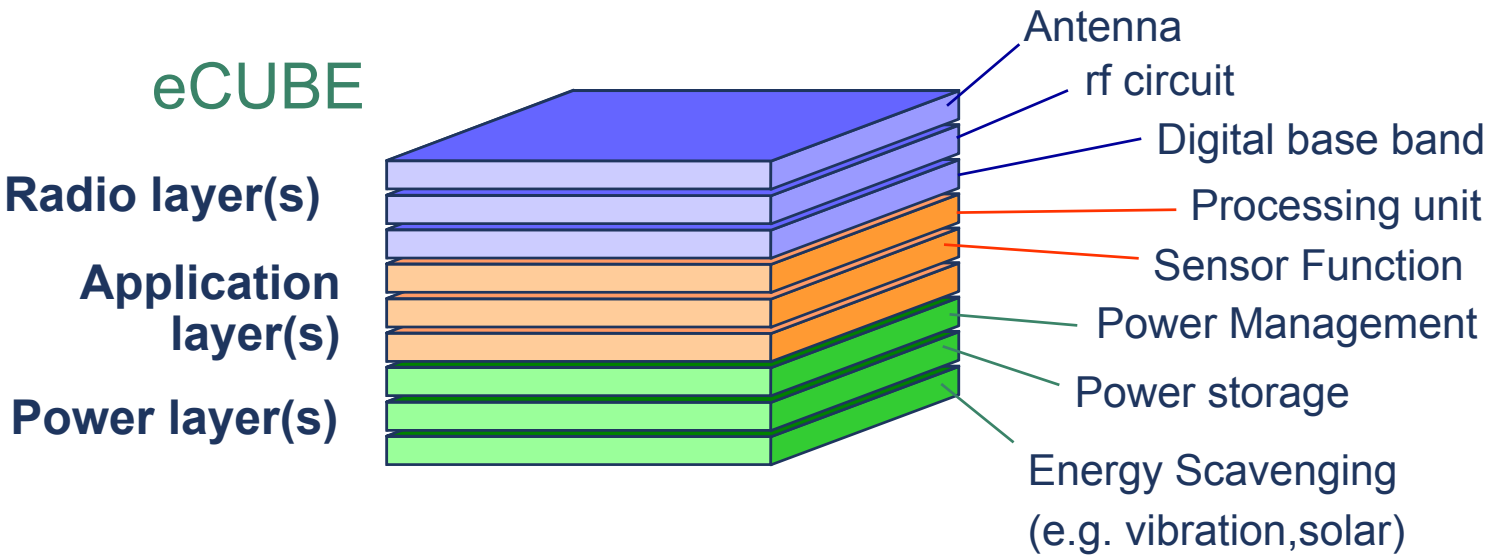
Examples :

- rf-SIP
- 3D stacked SIP
- 3D stacked IC's

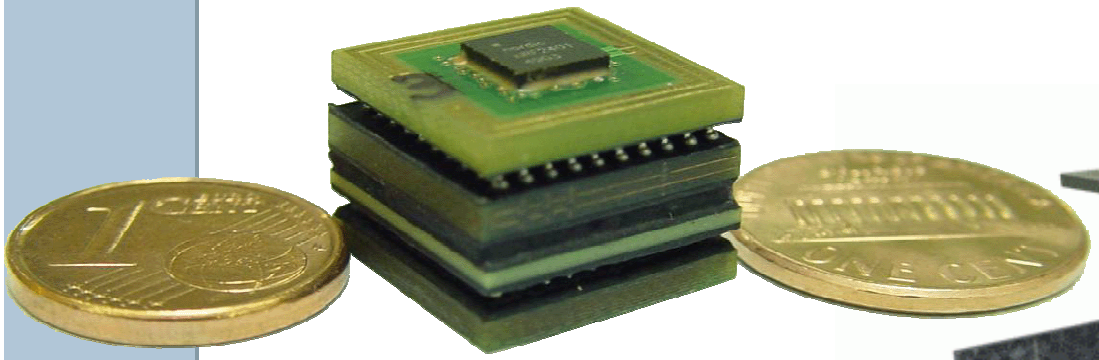
3D Integration technologies

3D-SIP

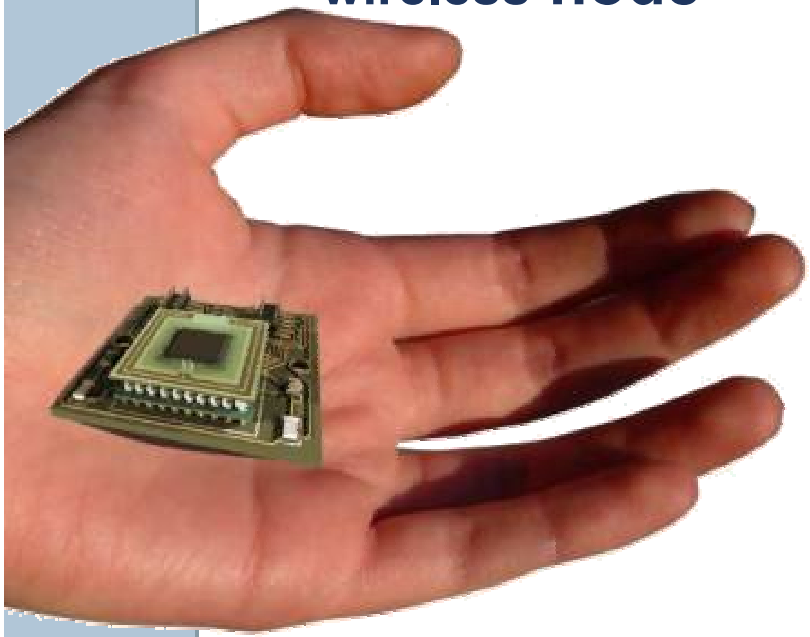
- Stacking of SIP sub-systems
- Most generic type
- Best yield and manufacturability
- Relatively low 3D interconnectivity
- Testability of separate layers
- Realisation of “e-Cubes”

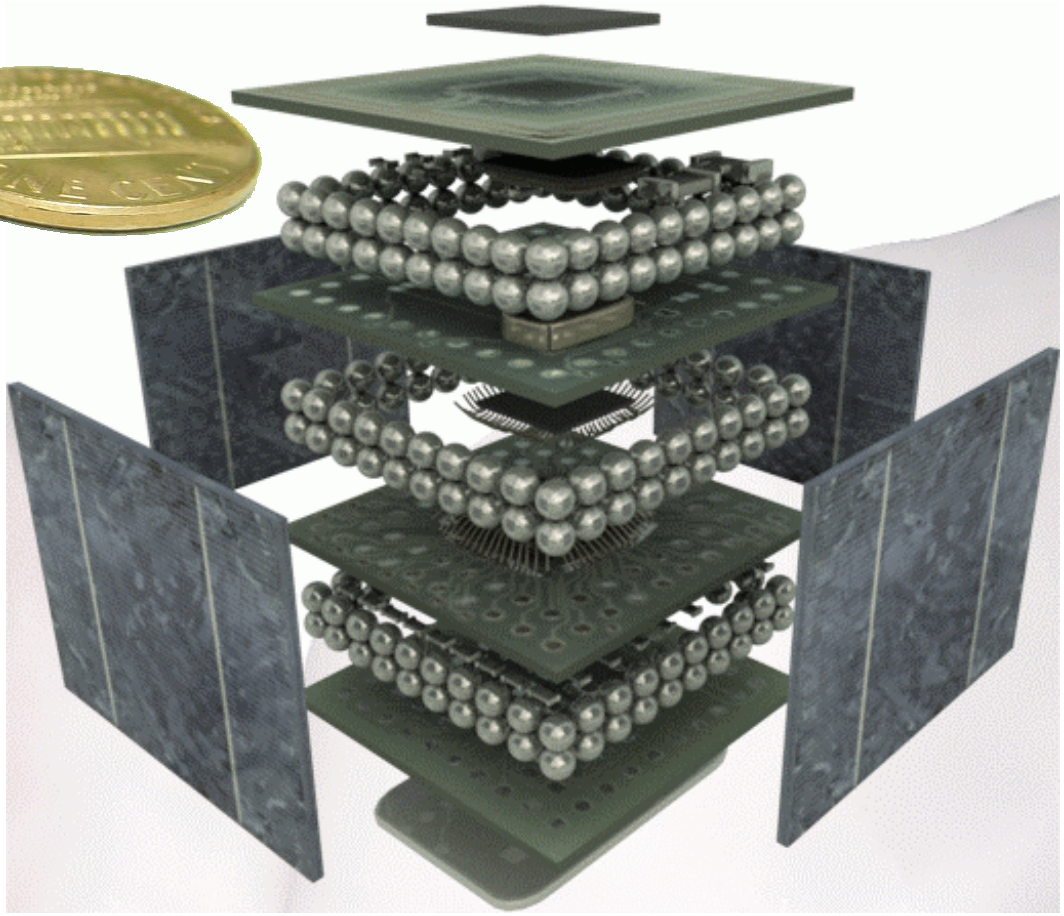


Wireless 3D Stack
IMEC'S human++ Program



14x14 mm autonomous wireless node





1cm^3 EEG/ECG SIP

SIP-design

Required :

Chip-package co-design

Examples :

- rf-SIP
- 3D stacked SIP
- 3D stacked IC's

3D packaging technology today

Stacked-die packages:

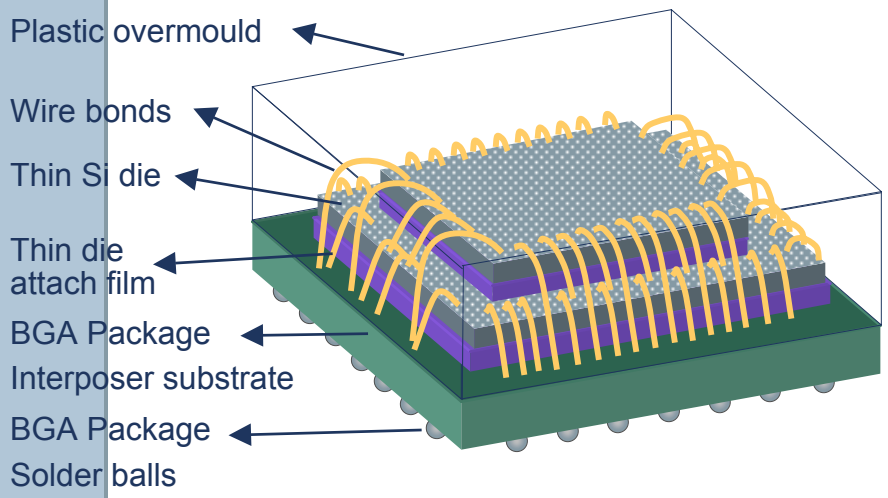
Assembly by wire bonding of stacked die in a single package

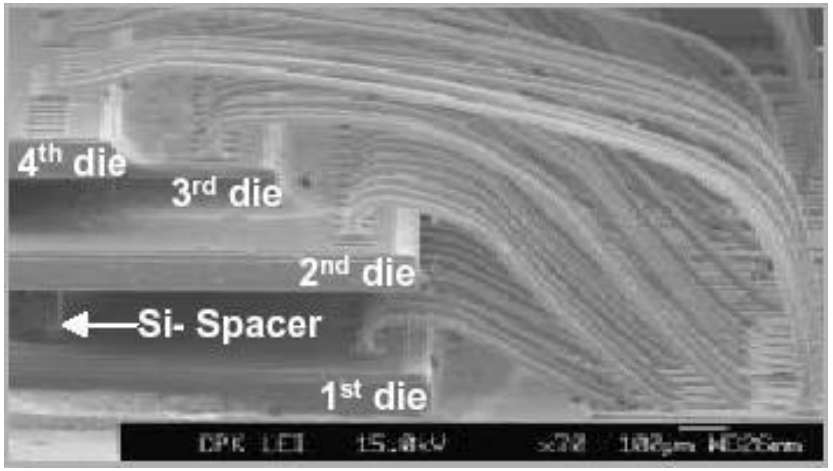
High volume, mainly: portable phone application:

various types of memory on cell-phone processor chips

Technology :

standard wire-bond packaging technology

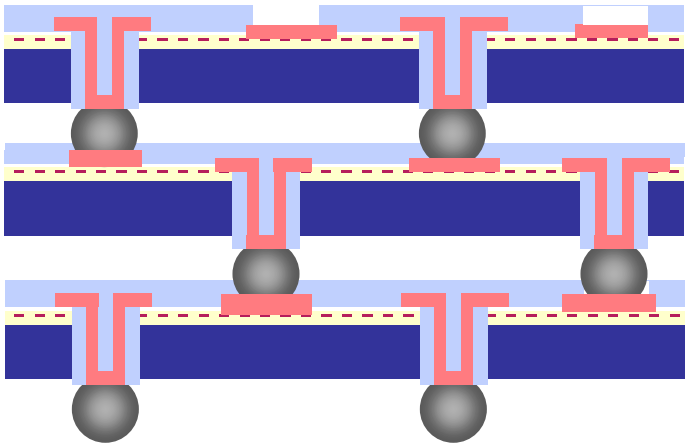


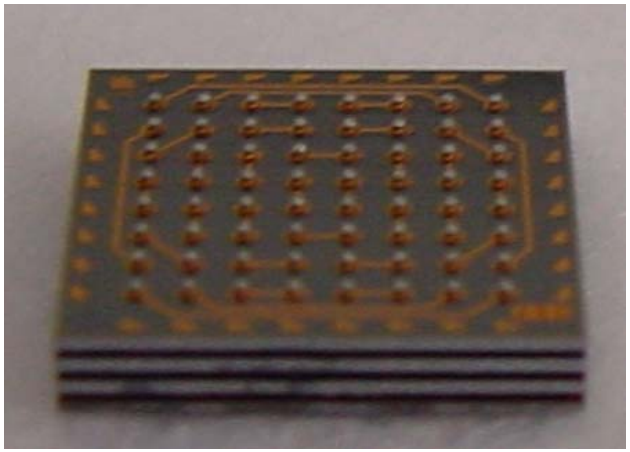


Source: ChipPac

3D-IC-stacking

Si-Through-hole and flip chip die-to-die bonding :
Interconnects between die at the bond-pad level





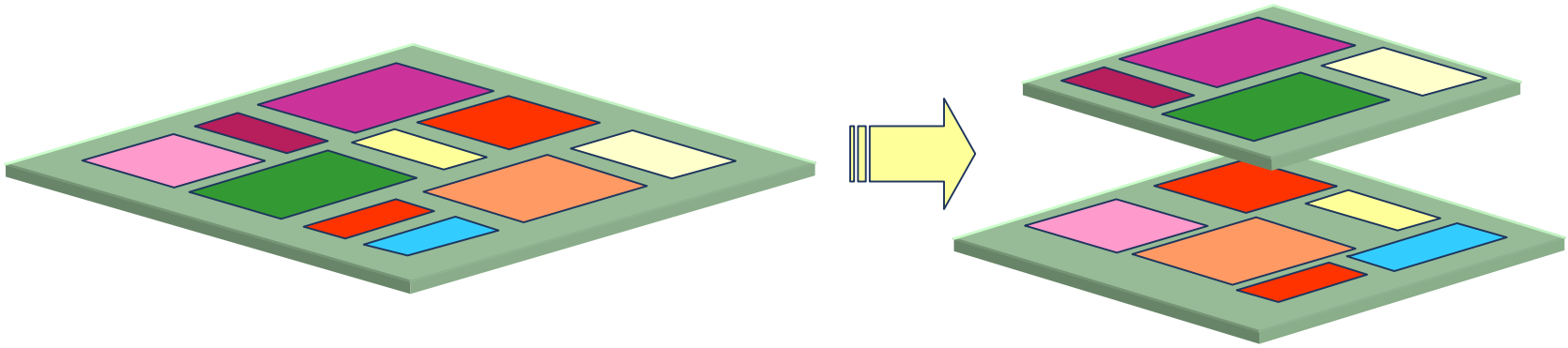
3D Die stacking needs

High density 3D-technology opportunity:

- 3D is not limited to connecting the I/O bond-pads of different die.
- It is also possibility to interconnect functional blocks (“tiles”) on a die to other tiles on other die: Interconnect at the Global on-chip interconnect level

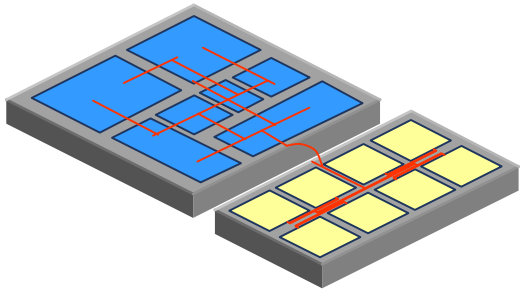
This results in a considerably higher I/O interconnect requirement

The Interconnect Bottleneck



If the functional “tiles” on the chip could be stacked in the 3rd dimensions, the chip area would be reduced, resulting in much shorter global interconnect lines.

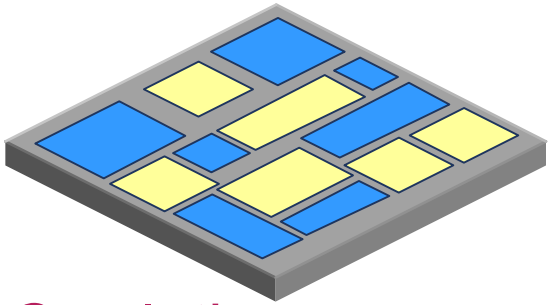
Logic & Memory



2D interconnect:

Long lines

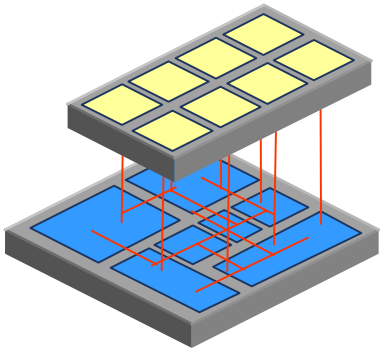
shared bus



SOC solution:

Large die

Large size Memory cells



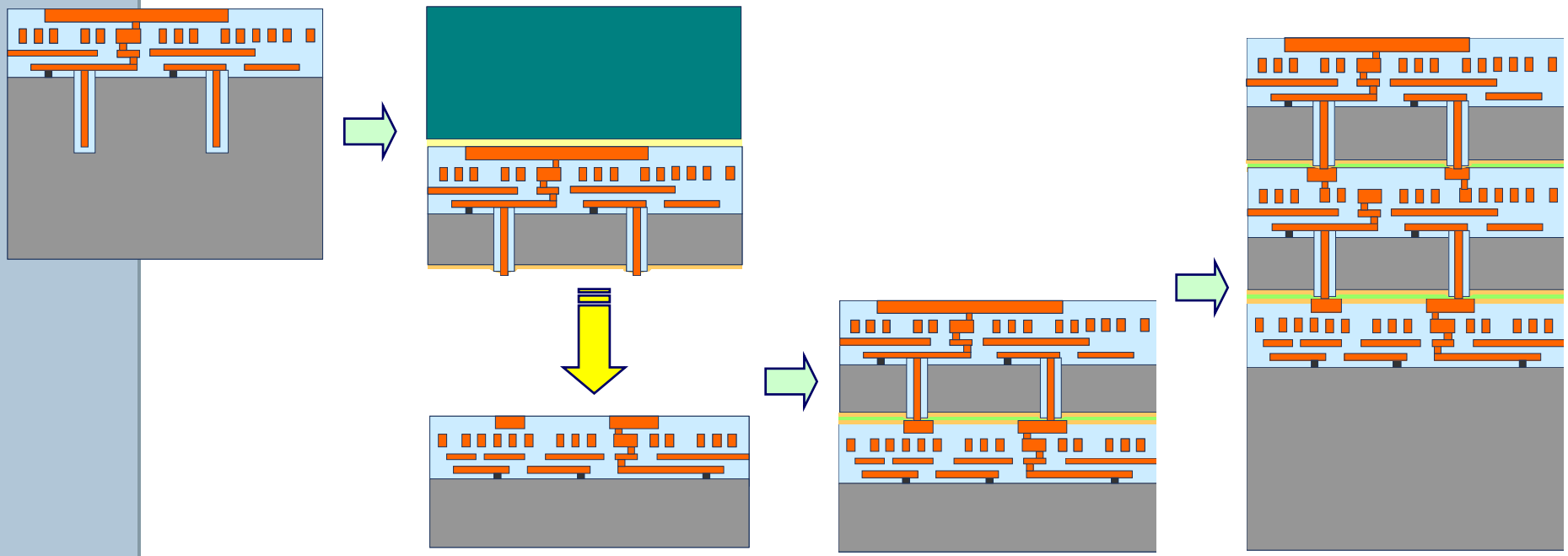
3D interconnect

Short, direct lines

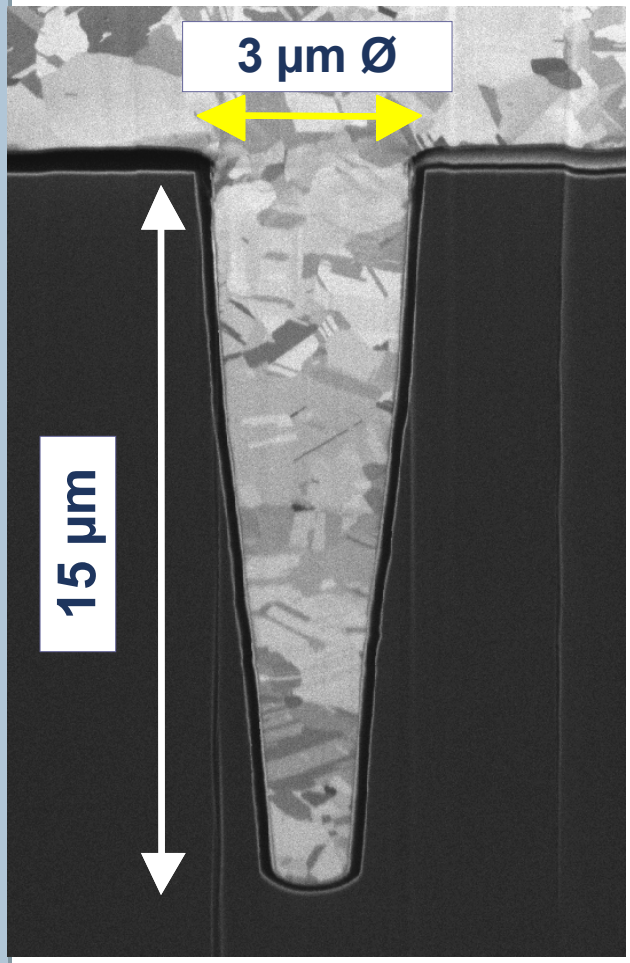
IMEC's 3D-SIC approach

IC-stacking technology at 'tile'-level:

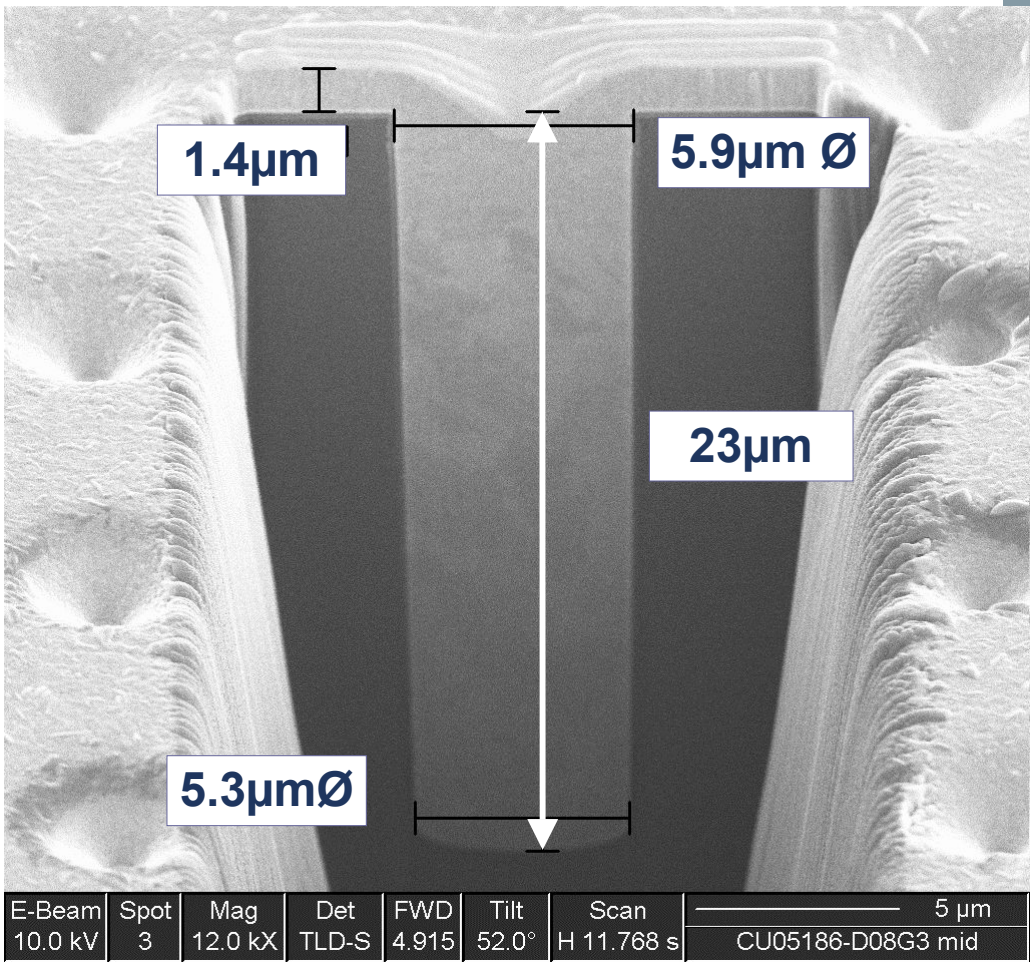
- 10 µm pitch 3D vias
- Burried "Cu-nails" between FEOL and BEOL
- No blockage of BEOL layers
- Cu-Cu thermo compression bonding
- Collective KGD Die-to-wafer bonding



3D-IC Cu nails



RIE etch



ICP-RIE 'Bosch' etch

ASM nuTool Cu fill

Technology for 3D-interconnects

- 3D interconnects may be realized at different levels of the micro-electronic system,
- Different microelectronic technologies may be used:
  - Traditional packaging & interconnection technologies: 3D-SIP
  - Wafer-level packaging technologies: 3D-WLP
  - IC-foundry technologies: 3D-SIC and 3D-IC

  ⇨ These technologies result in different 3D-interconnect densities and capabilities.
- Choice of technology depends on the interconnect requirements of a given application

Conclusion

- Trend to Increasing system complexity and system miniaturization requires SOC and SIP Technologies
- New SIP technologies allow for new design Methodologies
- Novel technology requires novel design tools to emerge from the feasibility stage

imec

SEEDS FOR TOMORROW'S WORLD **IMEC***NOLOGY*