Silíxtix

John Bainbridge

Silistix, Ltd. – John Bainbridge

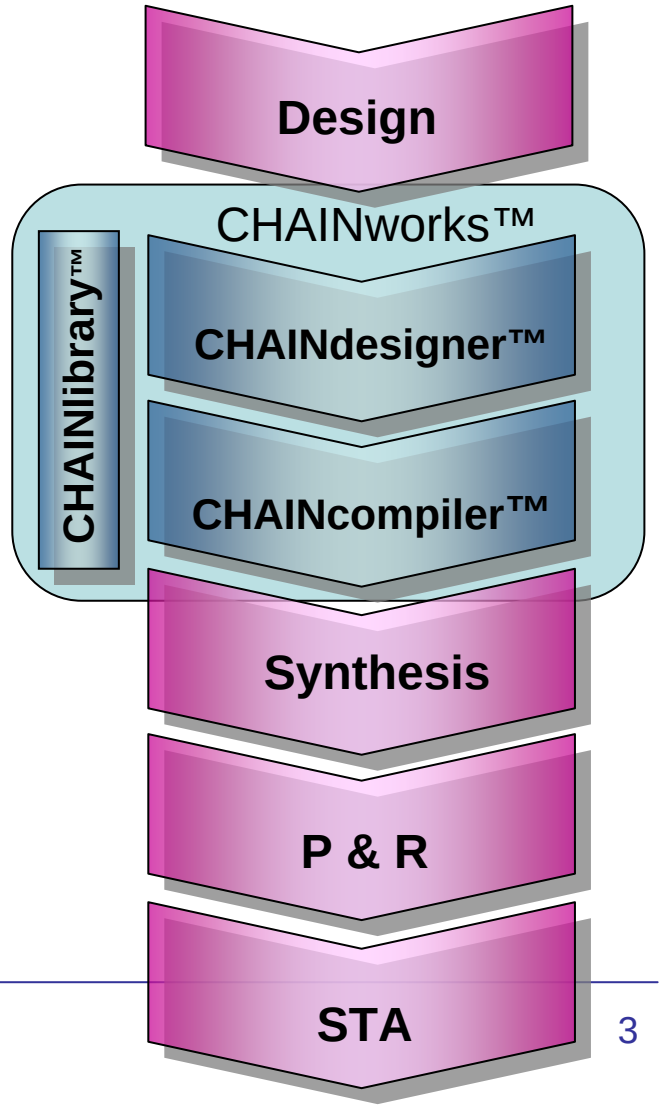
Silistix

- Venture funded UK company founded in late 2003
  - Intel Capital is lead investor
- Spin-out of University of Manchester
  - Technical founders from Steve Furber's AMULET research group
- Presence in US, UK, Japan

CHAINworks

Silistix

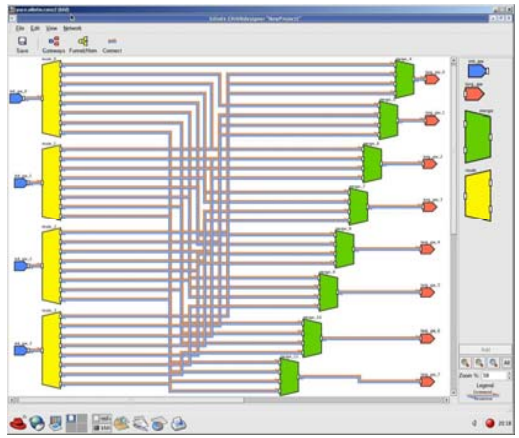
- Silistix is an EDA company
- CHAINworks fits easily within existing COT flows
  - Reduced power consumption
  - Reduced design effort / better reuse
  - Easier timing closure
- CHAINworks includes design and synthesis tools necessary to develop effective on-chip interconnect fabrics
  - Outputs systemC models
  - Outputs verilog netlists

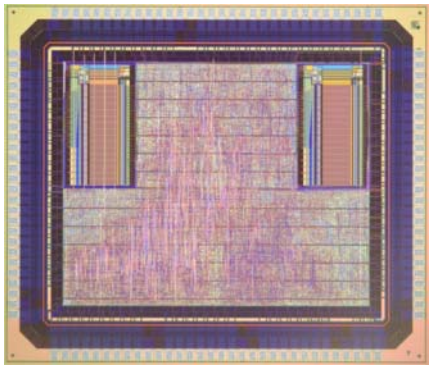


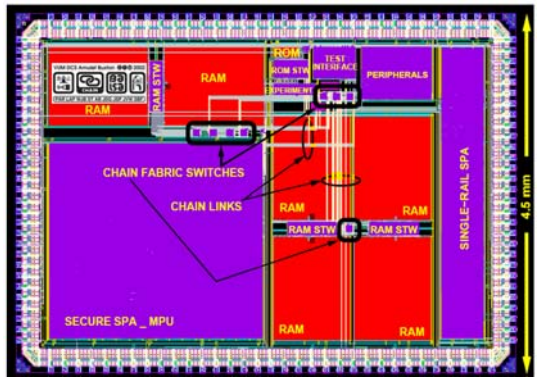
A few details & screen shots

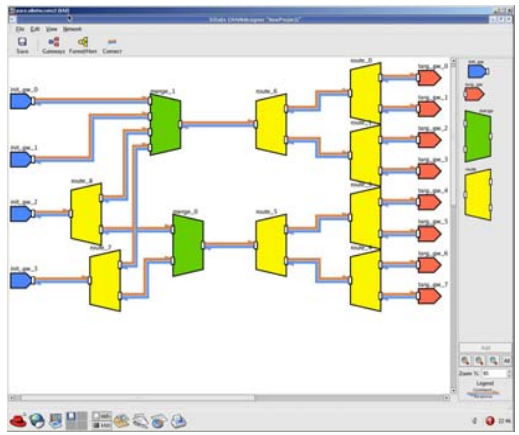
Silistix

- CHAINworks supports graphical exploration of tradeoffs between architectural and implementation choices - minimize resource use whilst maximising performance
- NoC fabric uses self-timed technology
  - GALS approach to SoC design
- Protocol adapters supplied to support existing synchronous bus protocols
- Early evaluations underway – release this year









Technion NoC group

Haifa, Israel

4 Faculty members

VLSI/Networking/System backgrounds

10 Graduate Students

Industrial liaison & funding

SRC/Freescale, Intel, Ceva

Israel Cidon

EE Department

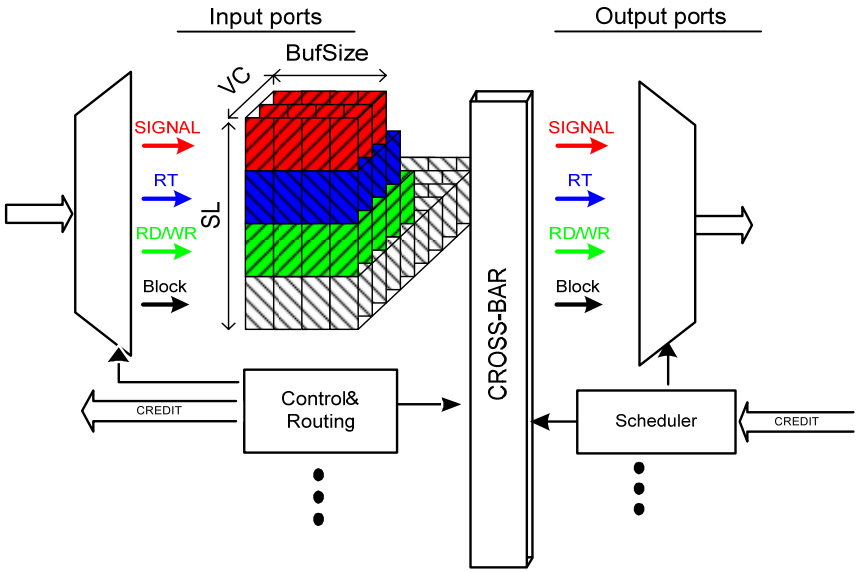
Technion—Israel Institute of Technology

Technion NoC group focus: **The Network Layer**

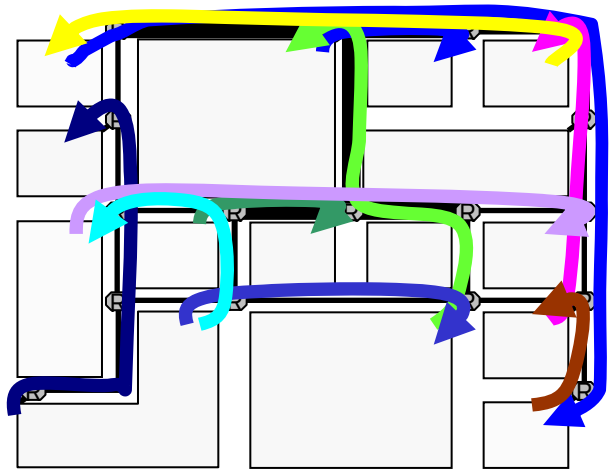
- Quality of Service assurance in NoC
- On-chip Costs
  - Routers and buffers are expensive
  - Power considerations
- NoC services for mutli-core processors
- Heterogeneous design scenarios
  - Predefined \ unknown traffic
  - Predefined (e.g.FGPA) \ undefined net resources
- Utilizing long distance communication
  - Both link and network layers

Technion NoC group: **Posters**

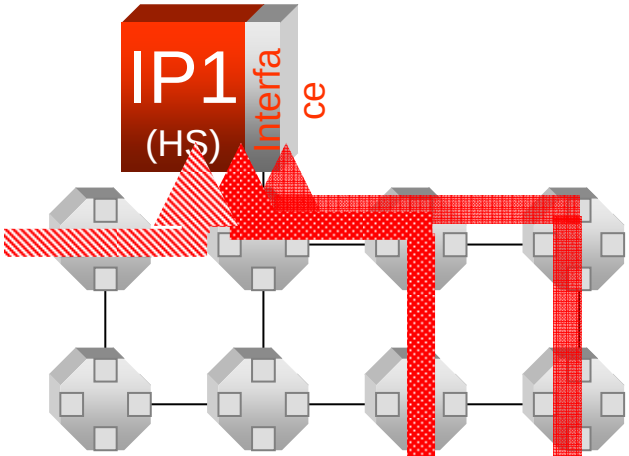
- QNoC architecture



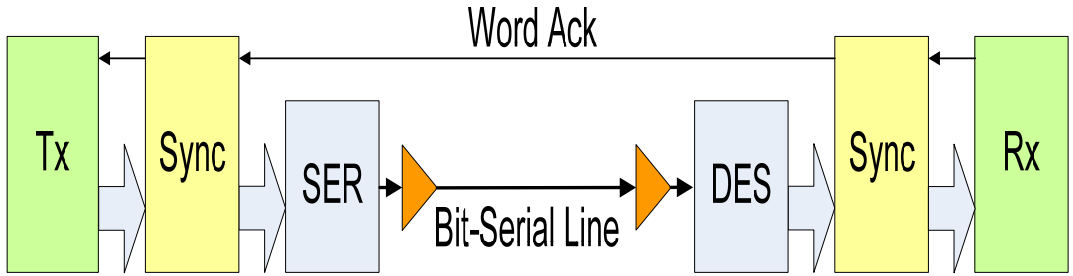
- Allocating capacity to network links



- Curing hot spots



- Fast asynchronous link



STNoC

An evolution towards MPSoC era

M. Coppola [1], C. Pistritto [2], R. Locatelli [1], A. Scandurra [2]

AST – Grenoble / OCCS - Catania

STMicroelectronics

Starting Points & Strategy

HPC

STBus On Chip Communication Experience

AST

NoC Research Experience

STNoc
NoC Architecture

- **Architecture**
- **Microarchitecture**
- **SystemC Models**

- **RTL Design**
- **FPGA Prototype**
- **Development Envr**

AST

To provide the advanced system knowledge able to establish ST as the system on a chip leading company in the market for the products of the next decade

A global research organization

HPC – OCCS (On Chip Communication System)

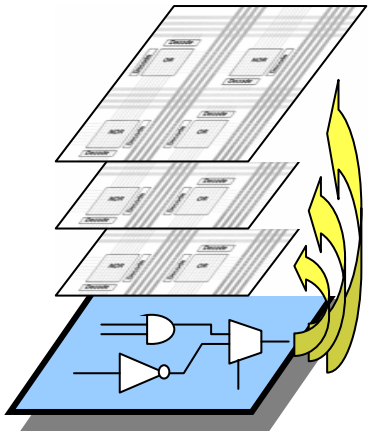
Mission:

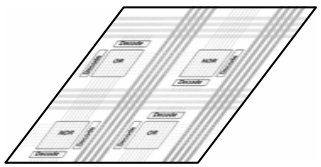
To provide ST divisions and key customers with state of the art competitive technology and infrastructure for on chip communication systems and off chip memory access.

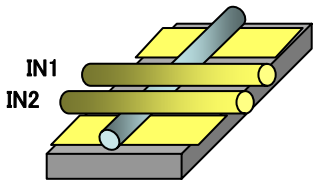
Team:

Catania, Tunis, Grenoble, Noida

Project : Nano-architecture for Post Silicon (Toshiba with Stanford and Caltech)







Ex. Carbon Nanotube

What suitable application?

System (**3D**)

NoC

Feed-back

Build-up

Building Blocks
(New IP)

Feed-back

Build-up

Circuit
(New Library)

Feed-back

Build-up

New Device

Figure out total design by new simulation tools with high accuracy.

Every layer should be designed simultaneously. (Co-design)

Simulated Reality for Post Silicon

Collaboration Scheme

Research Project Leader: Dr. Fujita

Emerging research memory based circuit Prof. Nishi Prof. Wong (**Stanford**)

Emerging Device based 3D Circuit Prof. Lee (**Stanford**)

Emerging Device based Defect Fault Tolerant & Architecture Prof. DeHon (**CALTECH**)

Toshiba Research America Inc. (San Jose)

V.P. : Mr. Okajima

Research Scientist: **Dr. Paul** (Visiting Scientist)

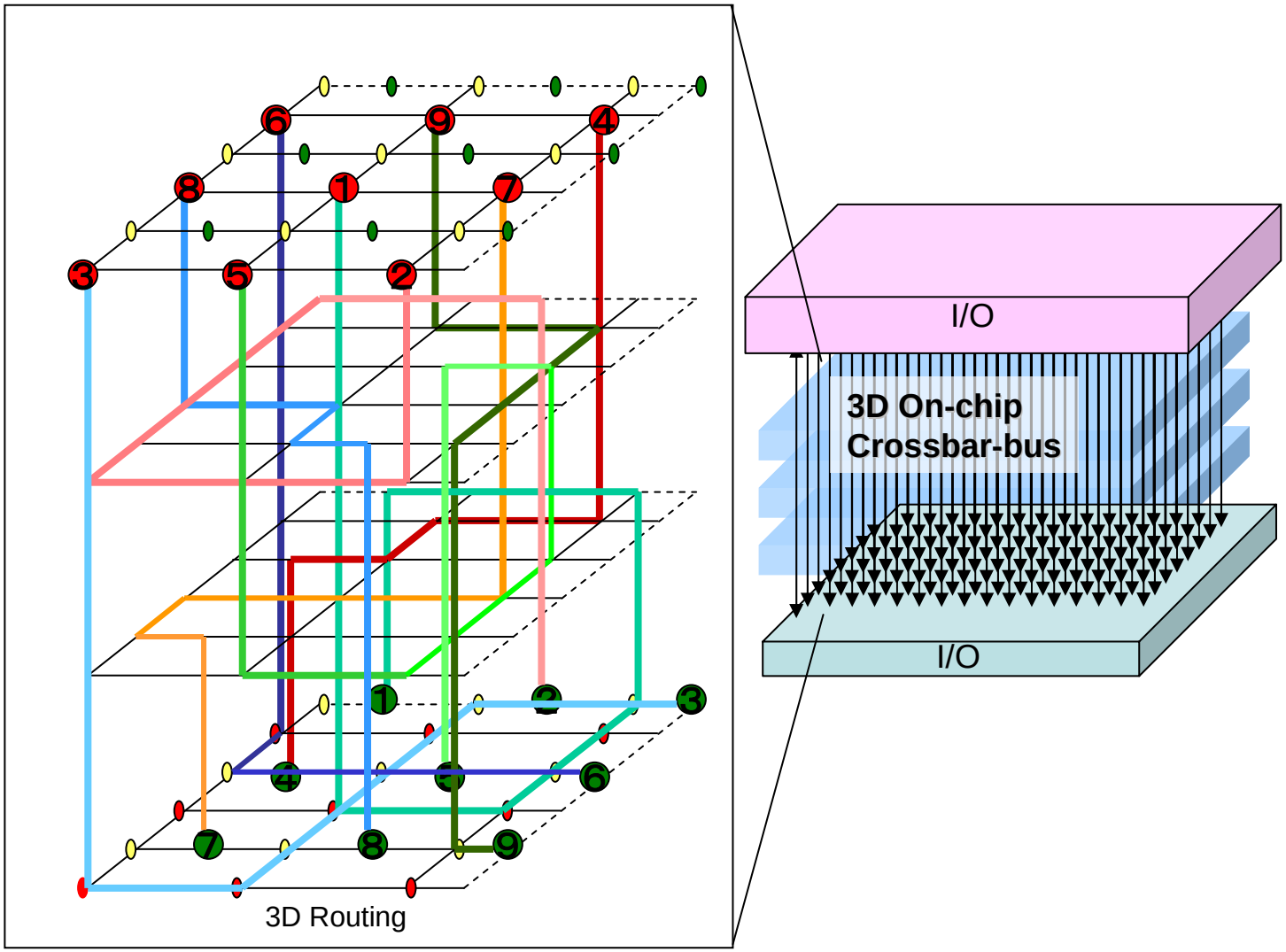
Toshiba Corporate R&D center, ***Frontier Res. Lab.*** *(Japan)*

Research Scientist
T. Tanamoto
S. Yasuda
K. Abe
K. Nomura

Univ.=4xProf. + 5x(PostDoc , PhD students)

Toshiba's researchers=6

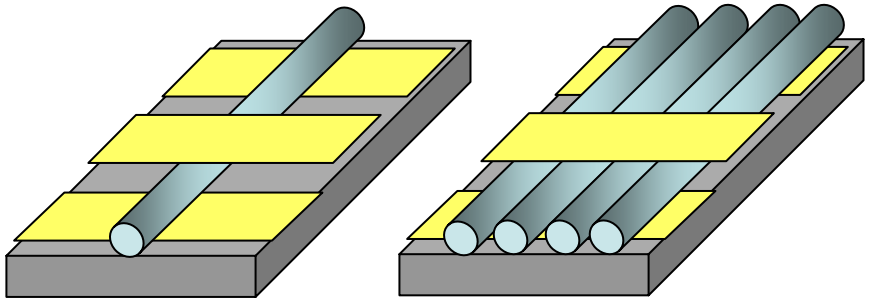
3D On-chip Crossbar Bus using Post Si



Ref. [1] K. Nomura et al. to be submitted.

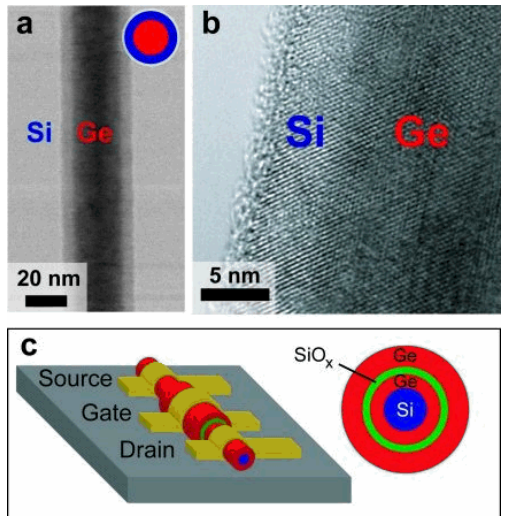
Post Silicon for switching devices

Carbon Nanotube



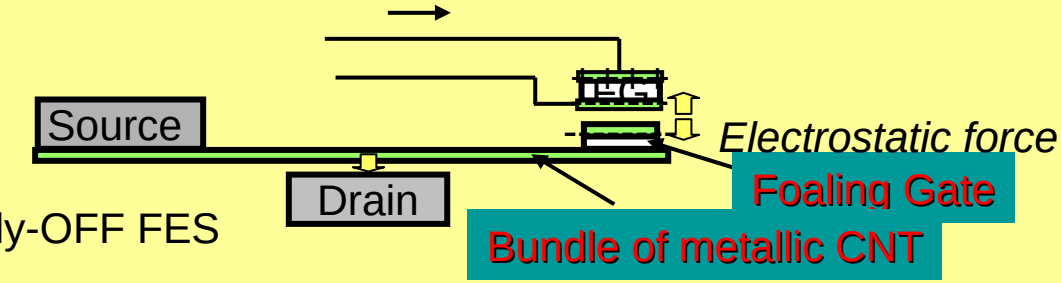
SiGe, Ge Nanowire

(III-V Compound Semiconductor)



Ref. Science

Carbon Nanotube **NEMS Switching Device**



Philips Æthereal Network on Chip

Kees Goossens
kees.goossens@philips.com
Embedded Systems Architectures on Silicon (ESAS)
IC Design
Philips Research

Philips Æthereal NOC group

- active since October 2001
- size of group varies

- Philips
  - Philips Research
    - IC Design Sector
      - Embedded Systems Architectures on Silicon (ESAS)
      - Digital Design and Test (DDT)
  - Philips Semiconductors
  - Philips Consumer Electronics
  - Silicon Hive

Philips Æthereal NOC focus

- focus of group listed as it changes over time
  - basic concepts [Progress'01]
    - QoS, transaction models, connections
    - programming models [Dekker'03, Kluwer'03, DT'05]
    - architecture [DATE'02, ISSS'05]
  - router architectures [DATE'03, CDT]
  - network interface architectures [DATE'04, TCAD'05]
  - NOC design flow [DATE'05]
    - NOC instantiation & simulation (SystemC, VHDL) [DATE'04]
    - performance verification
    - configuration
    - synthesis
    - multi-mode / task graph / use cases [DATE'06, our poster today]

Philips Æthereal NOC focus

- focus of group listed as it changes over time (cont'd)
  - "stuff around the network"
    - memory controllers
    - memory architectures, DMA/CA, subsystems/tiles
    - system-wide QoS (Hydra), data flow
  - extending NOC scope
    - NOC as TAM [ETS'06]
    - monitoring & debug [IEE comm.'03, HLDVT'04,ISCAS'06]
  - design time to run-time configuration, etc.
  - applications
    - TV & STB [Kluwer'04,DATE'06]

Philips Æthereal NOC collaborations

- collaborations with
  - Technical University Eindhoven, Netherlands
  - KTH, Sweden
  - Technical University Twente, Netherlands
  - University of Lund, Sweden

- for more information
  - kees.goossens@philips.com
  - www.homepages.inf.ed.ac.uk/homepages/kgoossen

UBC Vancouver
35,000 undergraduate students
8,000 graduate students
4,000 faculty members

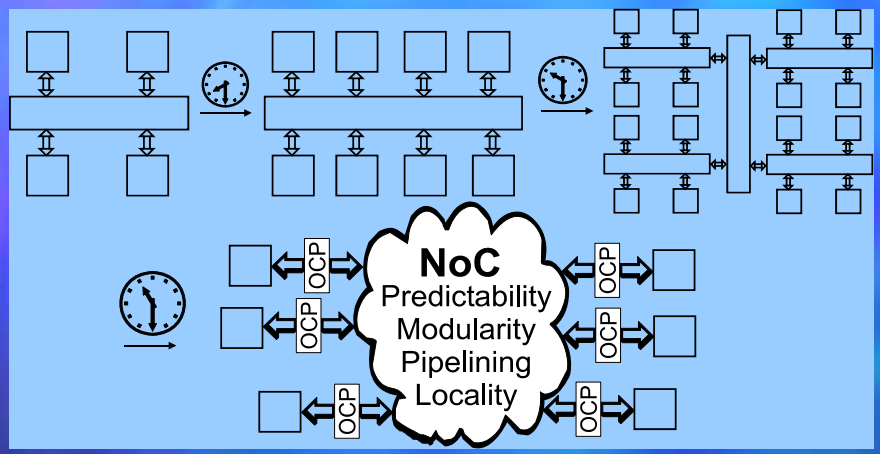
UBC ECE SOC
50+ graduate students
8+ faculty members

UBC ECE
650 undergraduate students
400+ graduate students
50+ faculty members

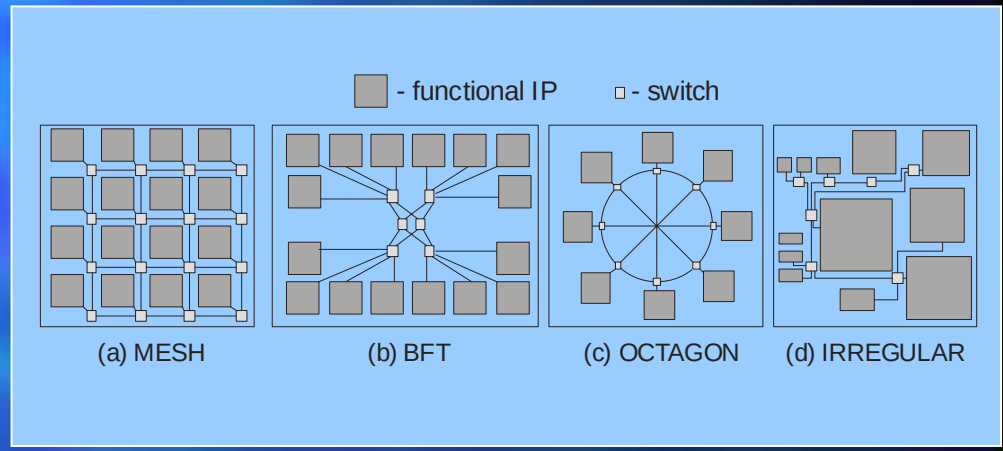
Network on Chip: Enabling Infrastructure for SoCs

P. Pande (now Assistant Professor at WSU)
C. Grecu (PhD candidate)
A. Ivanov
R. Saleh

Inter *IP* communication --- NoC to the rescue …



Different NoC Solutions/Architectures



Comparative Evaluation of NoC Infrastructures *METRICS*

- **Throughput**
- **Latency**
- **Energy/Power**
- **Area**

Test, Fault Tolerance & Reliability & Benchmarks ...

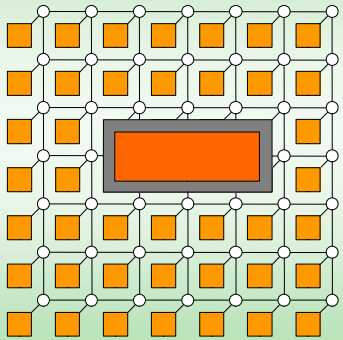
- Test, Repair, Fault Tolerance & Reliability
  - Built-In Self-Test Methodology
  - Built-In Self-Repair
  - Error Control (Fault Tolerance)
  - Reliability assessment and improvement
  - See Poster --- C. Grecu et al.

- NoC Benchmark Initiative
  - Promote and enable NoC advances (Design, Test, Evaluation) through comparison, exchange, etc
  - Expressed interest (academic)
    - R. Marculescu (CMU)
    - J. Sparso (TUD)
    - A. Jantsch (KTH)
    - A. Pinto (UCB)
    - P. Pande (WSB)
    - A. Ivanov (UBC)
  - OCP-IP support
  - Meet later today -- Lunch...!

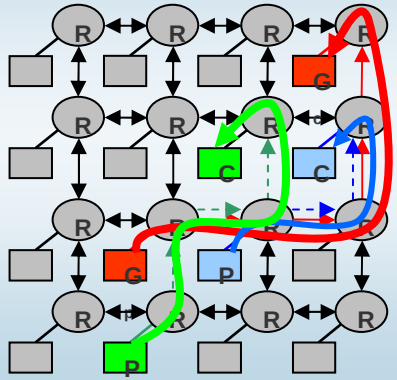
NoC Research at Jönköping University, Sweden

Research Overview

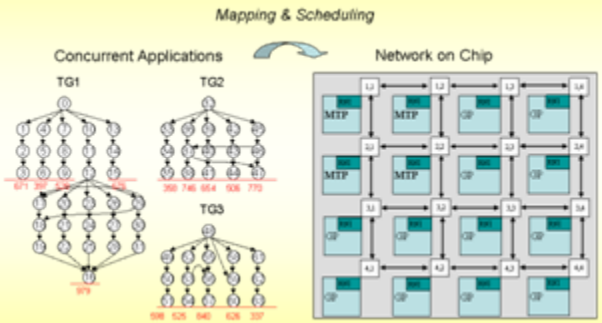
Region Concept and Deadlock free routing in Mesh NoC



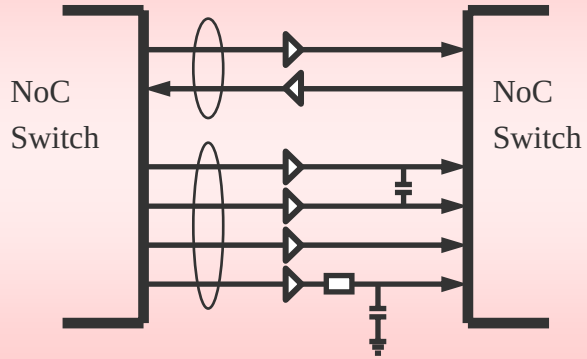
Routing Schemes in NoCs with Mixed QoS Traffic



Mapping Applications to NoC Systems



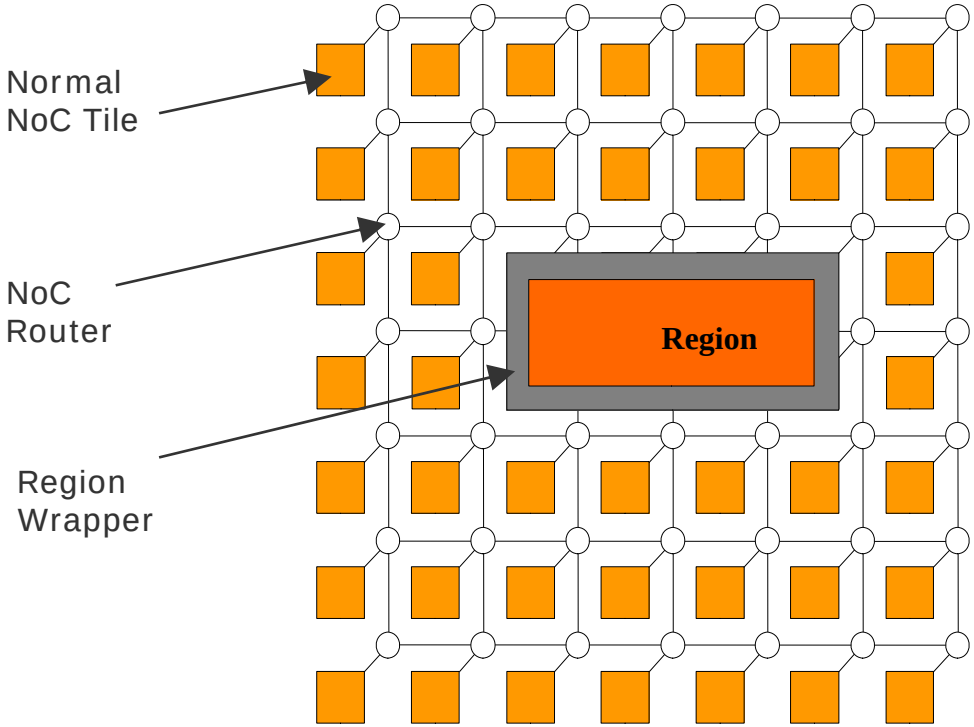
Delay Testing of NoC Interconnects



Region Concept & Deadlock Free Routing in NoC

Our Contribution:

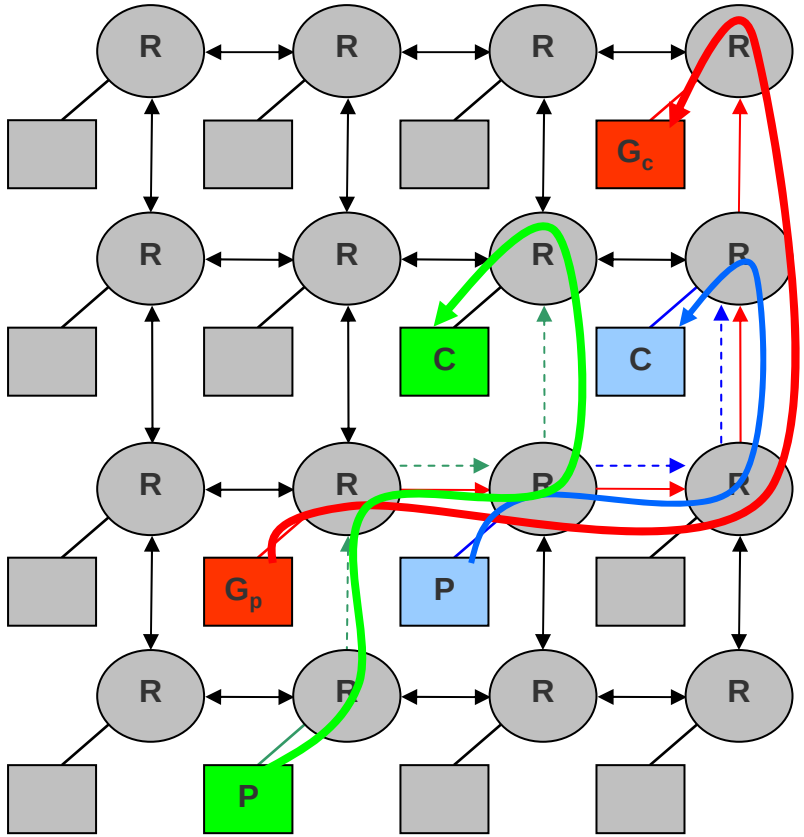
Dead lock free routing algorithm and evaluation of NoC with regions



Slack Time Aware Routing in Mixed QoS Traffic

Our Contribution:

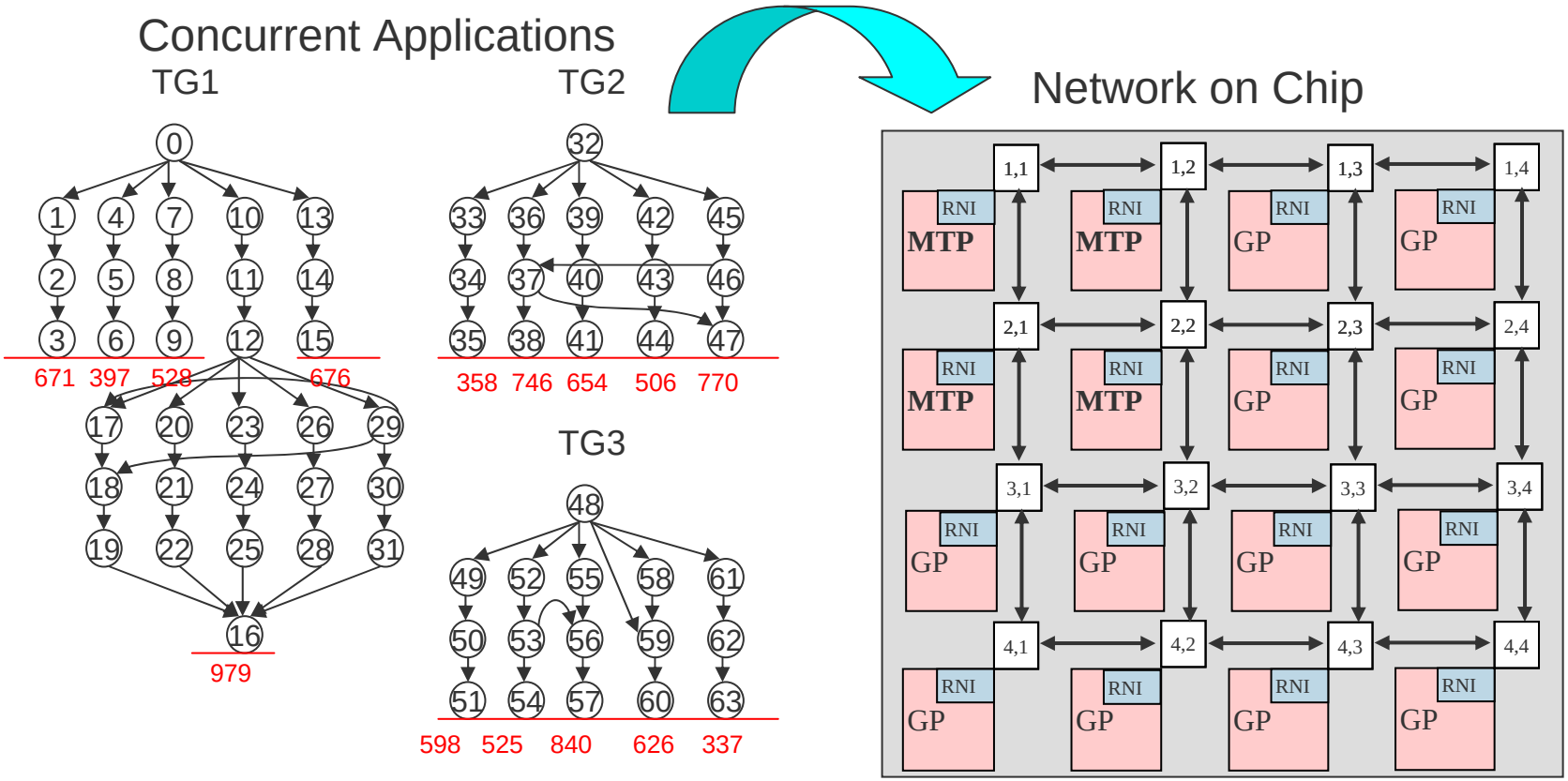
Routing schemes to use over-reservation of GT paths for improving BE performance



Mapping Applications to Mesh NoC with MTPs

Our Contribution:

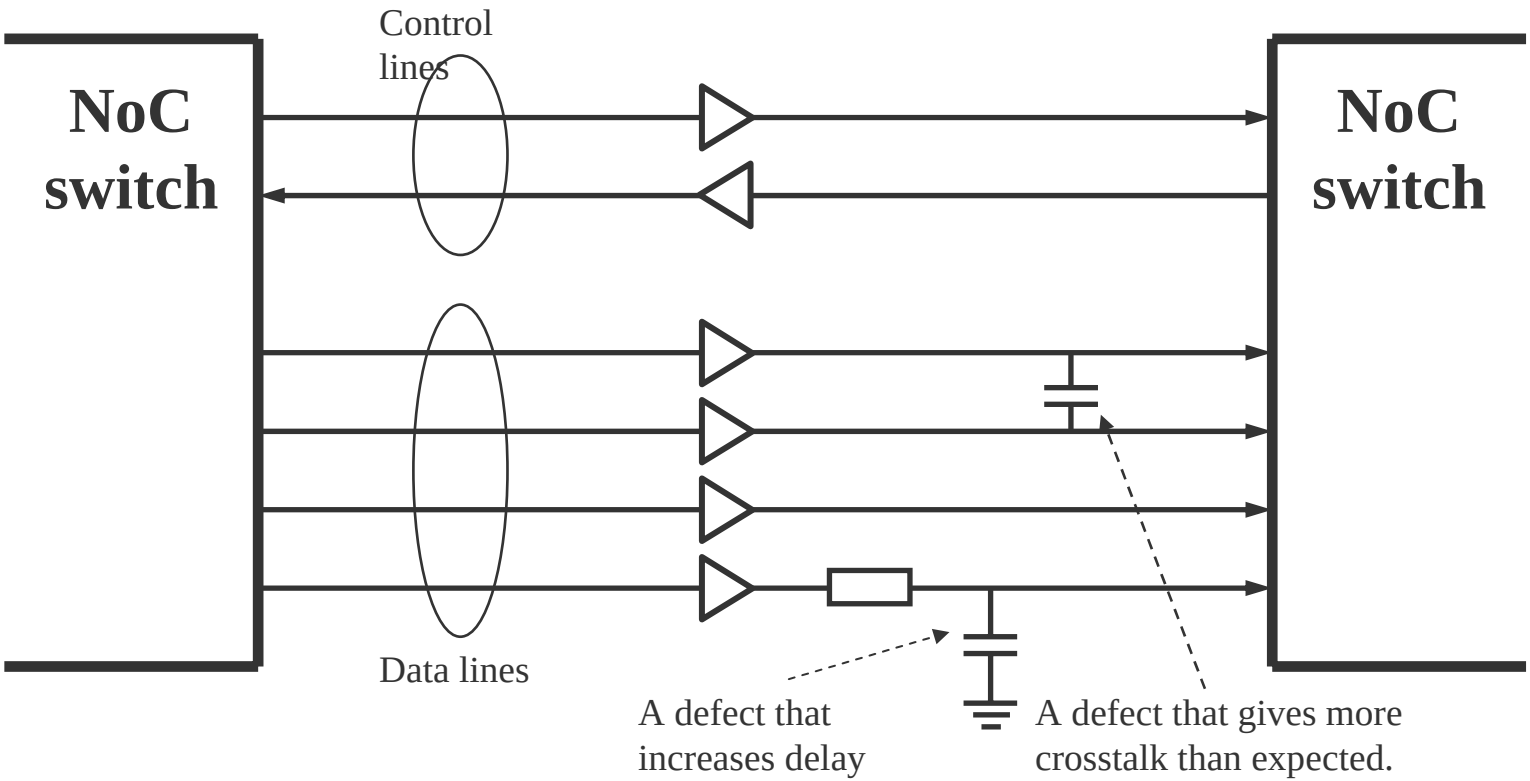
We demonstrate that MTP is a good resource for exploiting Thread Level Parallelism



Delay Testing of NoC Interconnects

Our Contribution:

An efficient method to test delay faults in NoC interconnects



Research Group

Performance and Cost optimization of application-specific Network-on-Chip

Philippe Martin, Arteris

Arteris Background

- **Incorporated in February 2003, in Paris, France**
  - Funded by leading international Venture Capital firms
- **Management from leading semi, EDA and system companies**
  - Successful track record with complex SoCs, IP products and services
  - 200 man years experience in SoC design and networking applications
- **Deliver NoC solutions solving all on-chip traffic management challenges**
  - NoC provides a layered approach compatible with existing IP
  - NoC brings best wire efficiency to transport transactions over complex SoC.
  - NoC brings scalable on-chip communication platform to re-use IP through next generation of CMOS processes.
- **Targets high-performance, IP-laden designs**
  - operating frequency > 250MHz
  - complexity > 10Mgates & > 40 IPs
  - 130nm, 90nm, 65nm CMOS process

Arteris™

Arteris enables application-optimized NoCs

SoC architecture constraints

- **Application constraints**
  - Reuse of existing IP cores
  - System Performance (bandwidth, latency, QoS)
  - SoC versatility (use cases)
- **Physical constraints**
  - Process technology
  - Floorplan constraints
    - I/Os, Clock and power domains
- **Cost constraints**
  - Minimize number of gates and wires

NoC optimization variables

- **Network topology**
  - Shared or private links
  - Multi-port network interfaces
  - Arbitration schemes
  - Buffering
  - Packet serialization
  - Operating frequency
  - GALS and clock domains

Arteris™

NoCexplorer™ - NoC topology exploration

- **High-level traffic modelling**
  - Stress and QoS requirements
- **Simple topology entry**
  - NoC interface and architecture
- **Fast, throughput-accurate simulations enable quick topology iterations**

- **SoC architects love it !**

Arteris™

System Level Design Group

Dept. of Electrical and Computer Engineering
Carnegie Mellon University
Pittsburgh, PA 15213, USA

Members

Faculty: Radu Marculescu

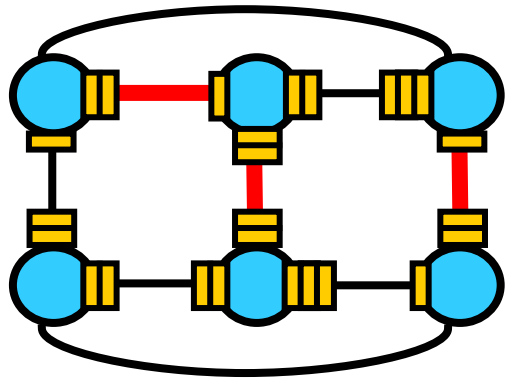
Phd Students: Umit Y. Ogras
Chen-linc Chou
Timothy Hou

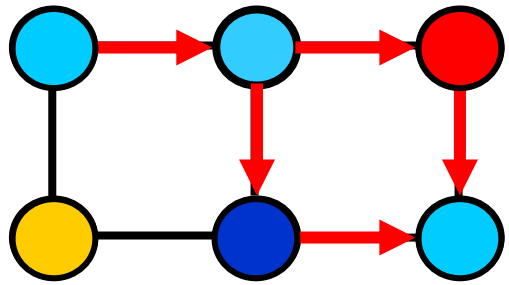
NoC Design Space Description

- NoC architecture can be characterized by the triple

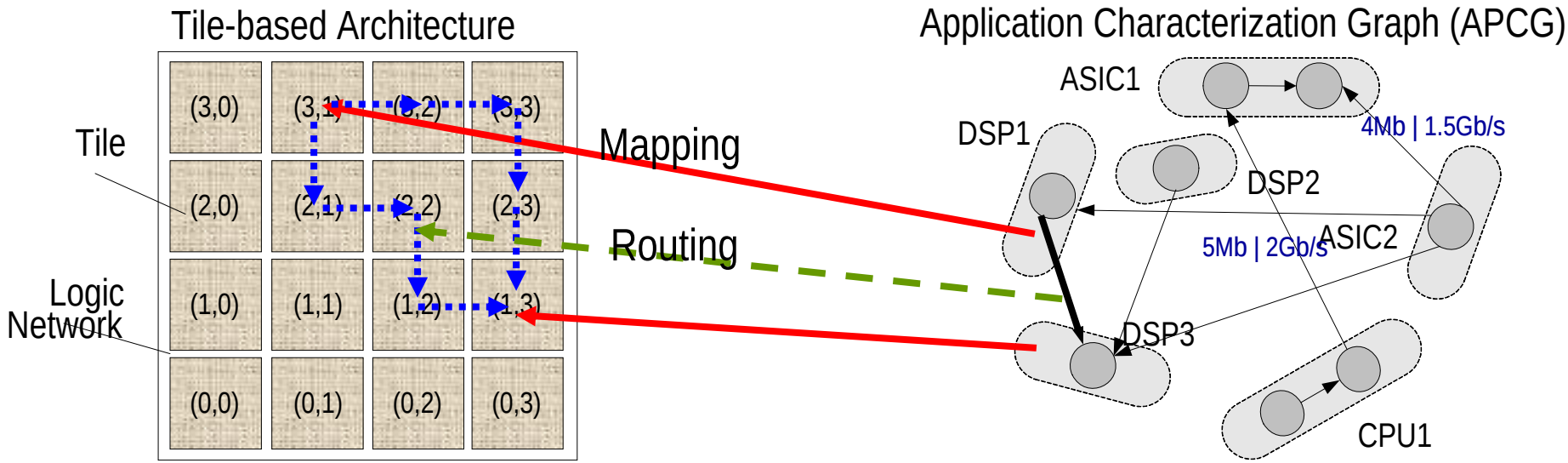
$$N(A(R,Ch),\Re,\Omega(C))$$

1. *A(R,Ch)*: the communication *infrastructure*
   - The set of routers and their interconnections
   - *R* and *Ch* can have multiple attributes (*e.g. buffer depth, channel width*)
2. $\Re$: the communication *paradigm*
   - The routing policy at a router given the source, destination, and congestion
   - The *switching* technique
3. $\Omega(C)$: the *mapping* of IP cores to the network

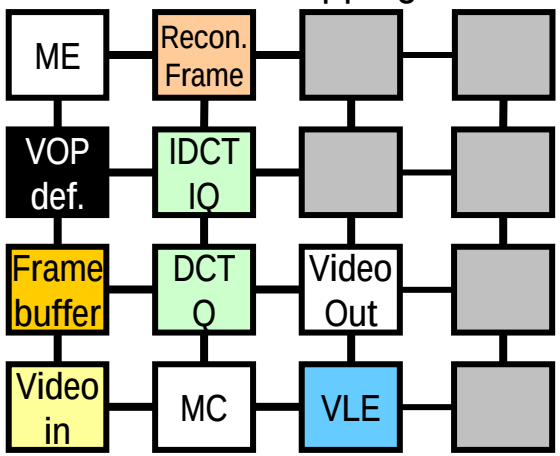




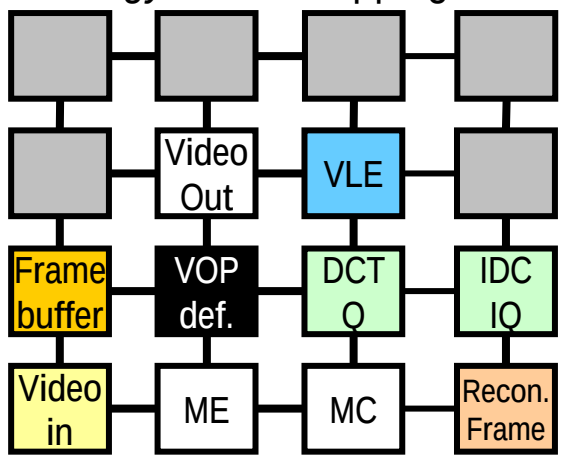
Application Mapping to Regular Architectures



MPEG design with *ad-hoc* mapping

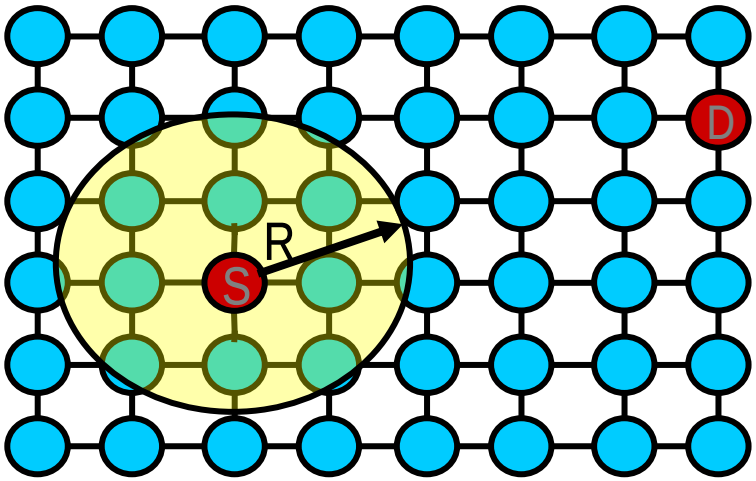


MPEG4 design with *energy-aware* mapping



Cycle-accurate simulations show ~50% communication energy savings!

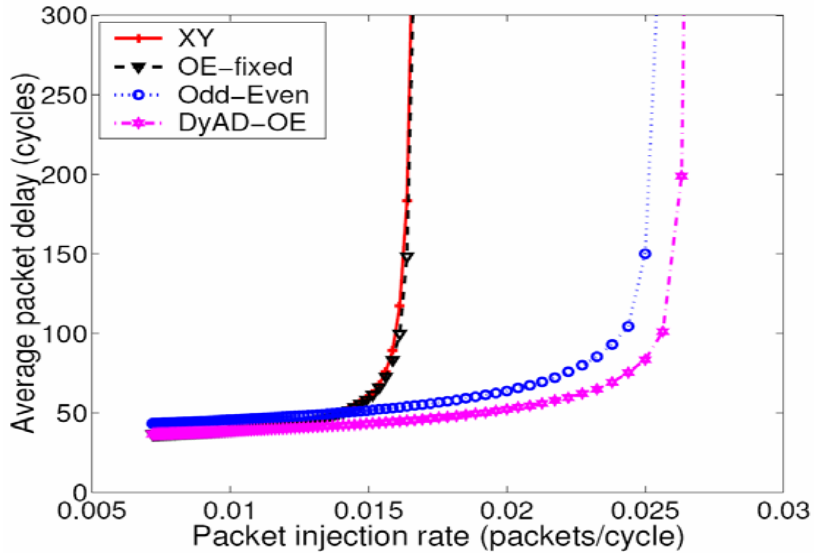
Communication Paradigm



-If dist < R : send to node with minimum congestion and when there are multiple alternatives, make a random decision

-else: send through the shortest path

- Deterministic routing
  - Lower latency at low levels of congestion
  - Performance degrades fast when congested
- Adaptive routing
  - Higher bandwidth saturation point
  - Higher latency at low levels of congestion
  - Deadlock issue



Tampere University of Technology
Institute of Digital and Computer Systems
Tampere, Finland

NoC research in the group of Prof. Jari Nurmi

Institute and group briefly

- Institute consists of 4 professors + about 100 researchers/assistants
- Typical annual production 100 international papers, 20 MSc, 5 PhD
- SoC/NoC research group of about 25 people since 1999

Background of Prof. Nurmi

- 19 years research on processors, ASIC/SoC for DSP/communication apps, on-chip communication/NoC
- Chairman of International Symposium on System-on-Chip since 2003 (SoC Seminar 1999-2002)
- Chairman of FPL 2005, TPC co-chair NORCHIP 2005, EWME 2006
- Co-editor of *Interconnect-Centric Design for Advanced SoC and NoC*, Kluwer Academic Publishers, 2004.
- Nokia Educational Award 2004
- Conference organizer of the year in Tampere 2005

NoC research topics at TUT

PROTEO flexible packet-switched NoC scheme (originally ring topology)

OIDIPUS network generation and optimization tool

XGFT (extended generalized fat tree) networks

Fault detection and repair in XGFT and Mesh NoCs

CDMA-based NoC concept

Latest: Hierarchical scheme for NoC

Computational elements around NoC

- COFFEE RISC Core™ (see coffee.tut.fi)
- **COFFEE-based multiprocessor platforms (with NoC)**
- Work on DSP and VLIW processors, co-processors, accelerators

Applications

- GPS and GALILEO positioning
- Multimedia applications
- RSA cryptography

Poster titles in this workshop

Presented by researcher Tapani Ahonen:

PROTEO – A Flexible Network-on-Chip Scheme

Network-on-Chip Generation and Optimization Tool

NoC-Based Platform Implementation on FPGA

A Hierarchical Approach to Network-on-Chip

Presented by Prof. Jari Nurmi:

Exploration of CDMA-Based Network-on-Chip

SystemC Simulation Model of a Flexible Network-on-Chip

Versatile XGFT Network-On-Chip with Improved Fault-Tolerance for Multi-Processor Systems-on-Chip

Fault-Diagnosis-And-Repair System for Improving the Fault-Tolerance and Manufacturability of MPSoCs

PICMOS
Photonic Integration on CMOS
STReP FP6-2002-IST-1-002131

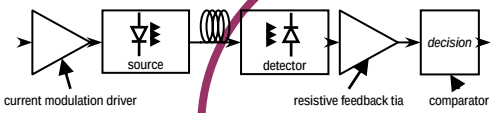
Ian O'Connor

Ecole Centrale de Lyon - LEOM

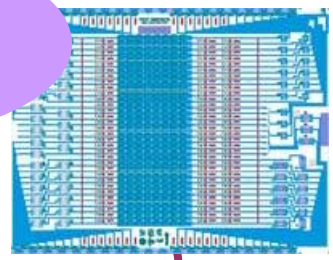
http://picmos.intec.UGent.be

PICMOS consortium

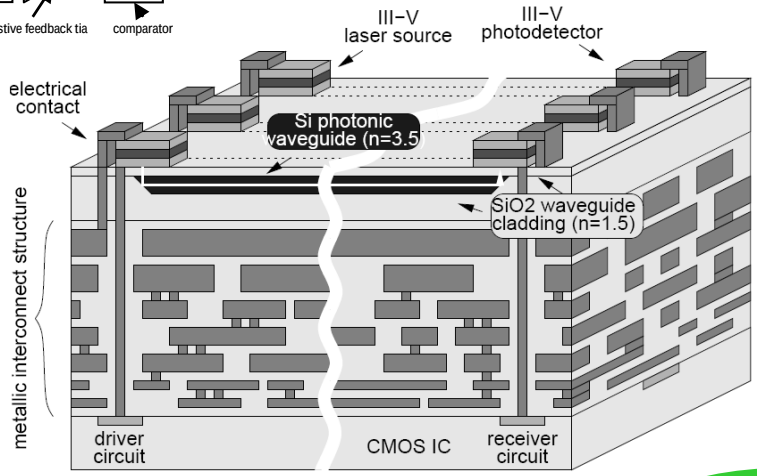
WP1 System analysis



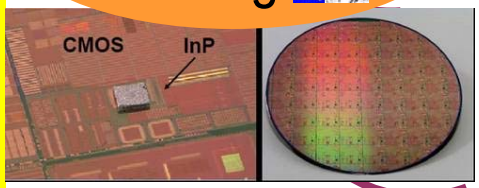
WP6 Integration



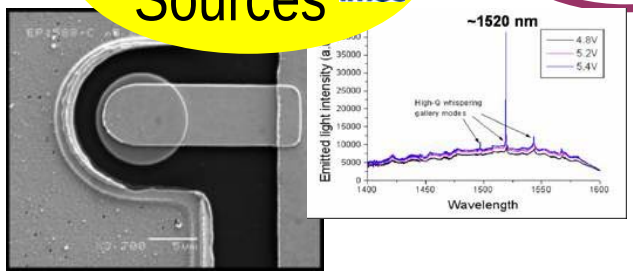
WP5 Waveguides



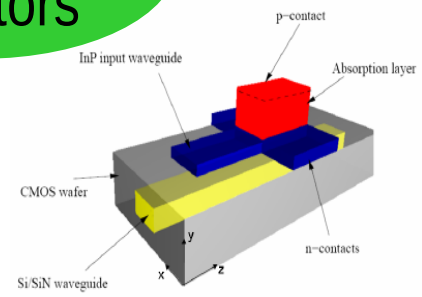
WP2 Bonding



WP3 Sources



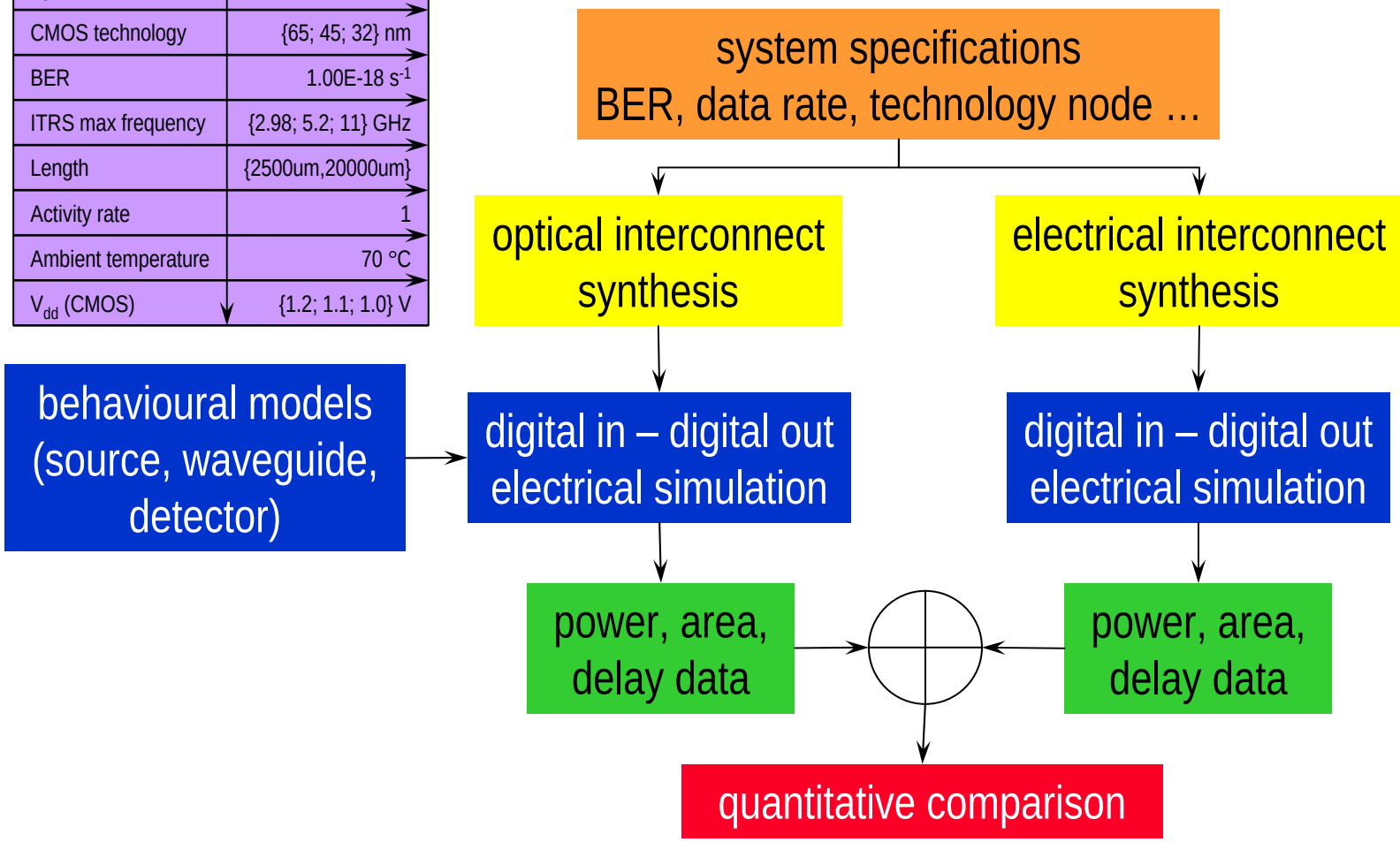
WP4 TU/e Detectors



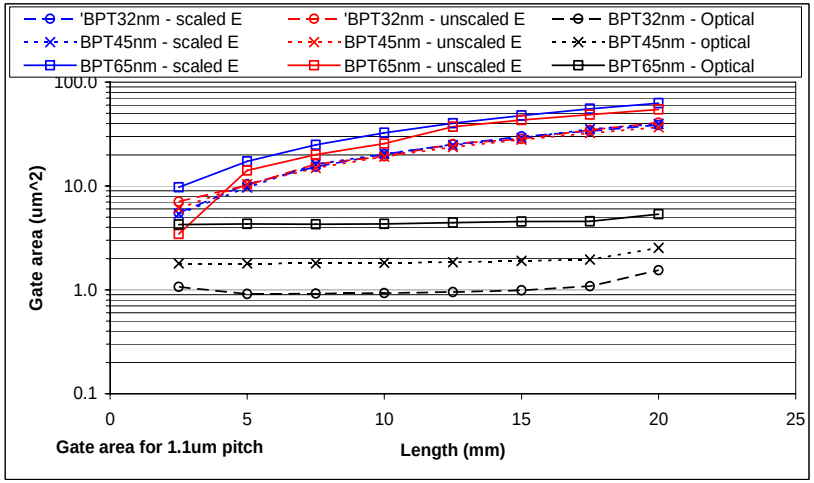
Research focus

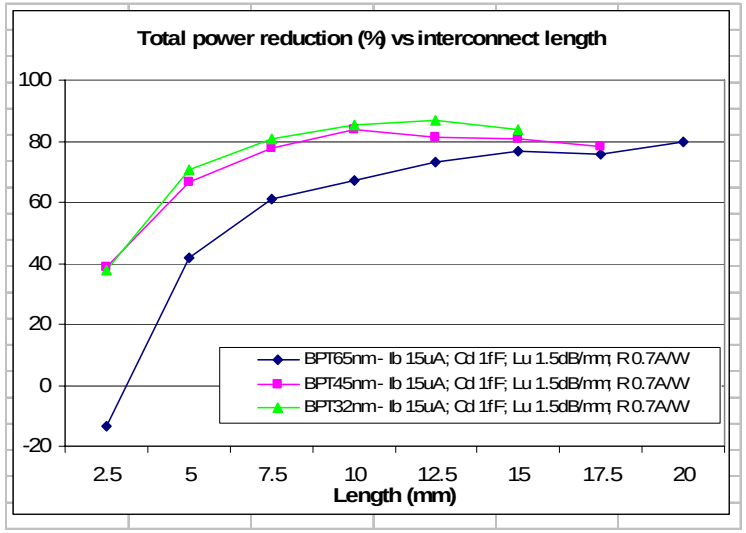
- **evaluate suitability of on-chip optical interconnect for data transport applications**

Specification	Value
CMOS technology	{65; 45; 32} nm
BER	1.00E-18 s^{-1}
ITRS max frequency	{2.98; 5.2; 11} GHz
Length	{2500um,20000um}
Activity rate	1
Ambient temperature	70 °C
V_{dd} (CMOS)	{1.2; 1.1; 1.0} V



Some results and conclusions





- **optical interconnect compares favourably for longer link lengths and more advanced technology (particularly true for gate area, also to some extent for delay and total power)**
- **design technology developed enables us to look at optical interconnect in various application contexts**

Introduction to KAIST BONE Project

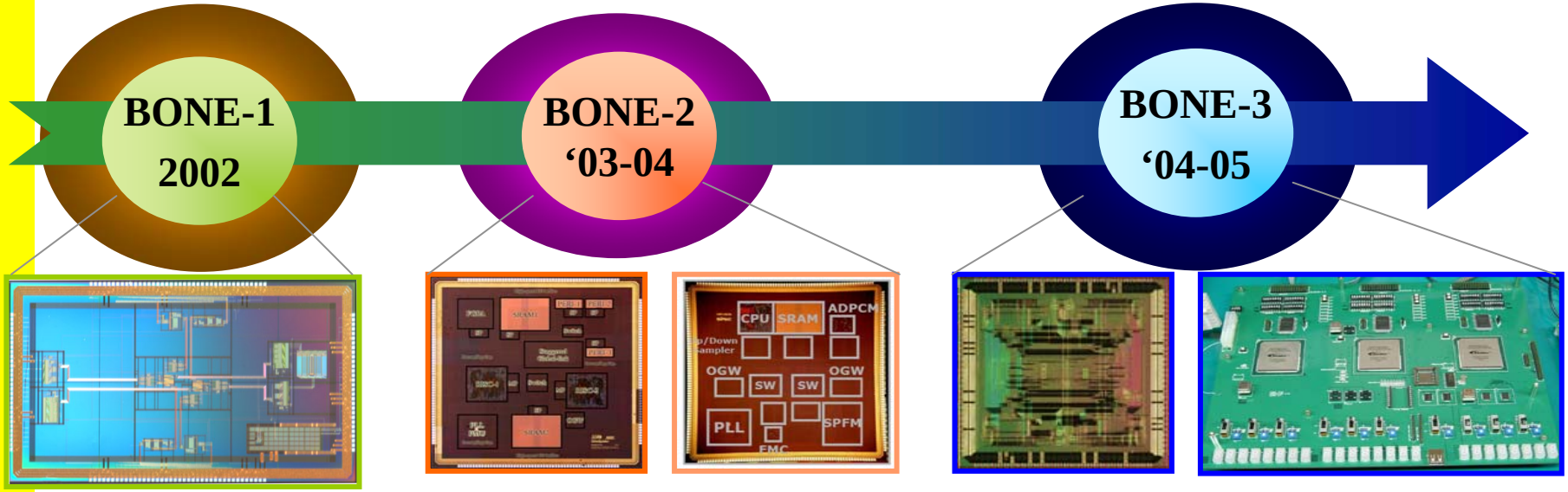
Kangmin Lee, Se-Joong Lee, Donghyun Kim,
Kwanho Kim, Juyoung Kim, and Hoi-Jun Yoo

Presented by Ju-Ho Sohn
Korea Advanced Institute of Science and Technology (KAIST)

KAIST

BONE Project since 2002

- **Realizes new NoC technology through IMPLEMENTATION!**
- **Covers**
  - **circuit-level designs,**
  - **architectural and protocol researches,**
  - **system integration on NoC Platform.**



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Further Information

→ http://ssl.kaist.ac.kr/ocn

Thanks!