CALL FOR PAPERS

IET Computers & Digital Techniques

(Formerly IEE Proceedings Computers & Digital Techniques)

Special Issue on Networks-On-Chip

The most daunting challenge to future on-chip multiprocessor systems is to realise the enormous bandwidth capacities and stringent latency requirements when interconnecting a large number of processing cores in a power efficient fashion. In a short time span, networks-on-chips have been recognised as the most important alternative for the design of modular and scalable communication architectures in the nanometre regime. This special issue intends to host relevant research contributions advancing knowledge in the field of on-chip networks. Submissions addressing design issues at all levels of abstraction are encouraged, from physical on-chip link design to data-link layer, from architecture design and optimisation to system-level design-space exploration, ranging up to programming models and application software.

Topics of interest include, but are not limited to:

- Network architecture (topology, routing, arbitration)
- Power and energy issues in NoCs
- NoC case studies, application-specific NoC design
- Timing, synchronous/asynchronous communication
- NoC reliability issues
- O/S support for NoC
- Metrics and benchmarks for NoCs
- NoC Network interface issues
- Modelling, simulation, and synthesis of NoCs
- Network-on-chip design methodologies
- NoC Quality of Service
- NoC support for CMP / MPSoC
- NoC support for memory access
- NoCs for FPGAs and structured ASICs
- Programming models
- Mapping of applications onto NoCs
- Novel interconnect links / switches /routers
- Signaling and circuit design for NoC links
- Physical design of interconnect and NoC
- NoC design tools
- Debug & Test of NoC
- Floorplan aware NoC architecture optimisation

Submission details

Authors are encouraged to submit high-quality research contributions that will not require major revisions. Extensions of paper presented at the International Symposium on Networks-on-Chip, Newcastle Upon Tyne, United Kingdom, April 7-10, 2008 (http://async.org.uk/nocs2008), are especially encouraged, but work not presented at the symposium is also welcome. Please identify clearly the additional material from the original symposium paper in your submitted manuscript. A minimum of 30% new material is required, including deeper theory or extensions of experimental results.

Prospective authors should submit their manuscripts electronically via the IET CDT submission site: http://mc.manuscriptcentral.com/cdt. Authors should clearly identify their papers as submissions for the 'Special Issue on Networks-on-Chip 2008' on their manuscript. All manuscripts are subject to the standard IET CDT review process. Instructions on how to submit a paper can be found at http://www.theiet.org/publications/journals/ and authors can contact the journal's managing editor, Tony Donegan (tdonegan@theiet.org) , for further assistance.

Guest Editors

Davide Bertozzi
Electrical Engineering Department
University of Ferrara, Italy
E-mail: dbertozzi@ing.unife.it

Kees Goossens
NXP Semiconductors Research /Computer Engineering Delft University of Technology, The Netherlands
E-mail: kees.goossens@nxp.com

Important Deadlines:

Submission deadline: July 1, 2008
Notification of Acceptance: November 1, 2008
Final manuscript submission: January 1, 2009
Target appearance date: March 2009 issue

IET Computers & Digital Techniques is available through the IET Digital Library (http://ietdl.org/IET-CDT/) and IEEE Xplore platforms, and is indexed worldwide in all major databases including ISI, Inspec and EI Compendex.