Newcastle University

Digital Systems Clocking with and without clock: a historical retrospective

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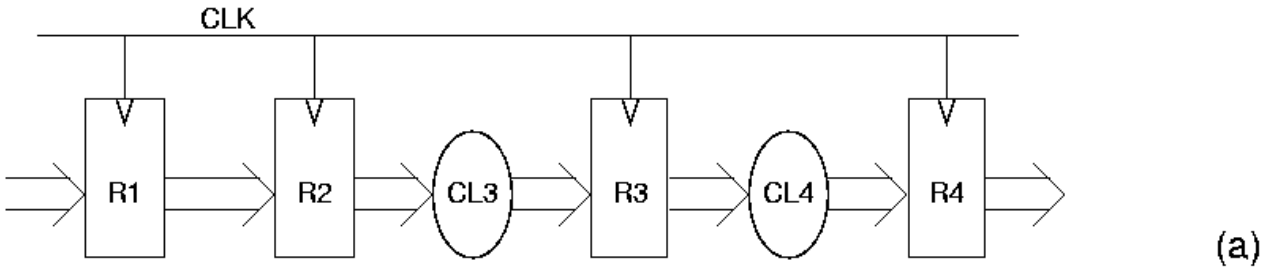
Outline

- Synchronous vs Asynchronous systems in a nutshell
- Brief history of “asynchronous clocking”
- LETI people in asynchronous design
  - Back then: Victor Varshavsky’s group
  - In recent years
  - Today
    - LETI in Newcastle
    - Electromagnetics Interest Group
    - Oliver Heaviside legacy
- Collaboration with Milos Krstic

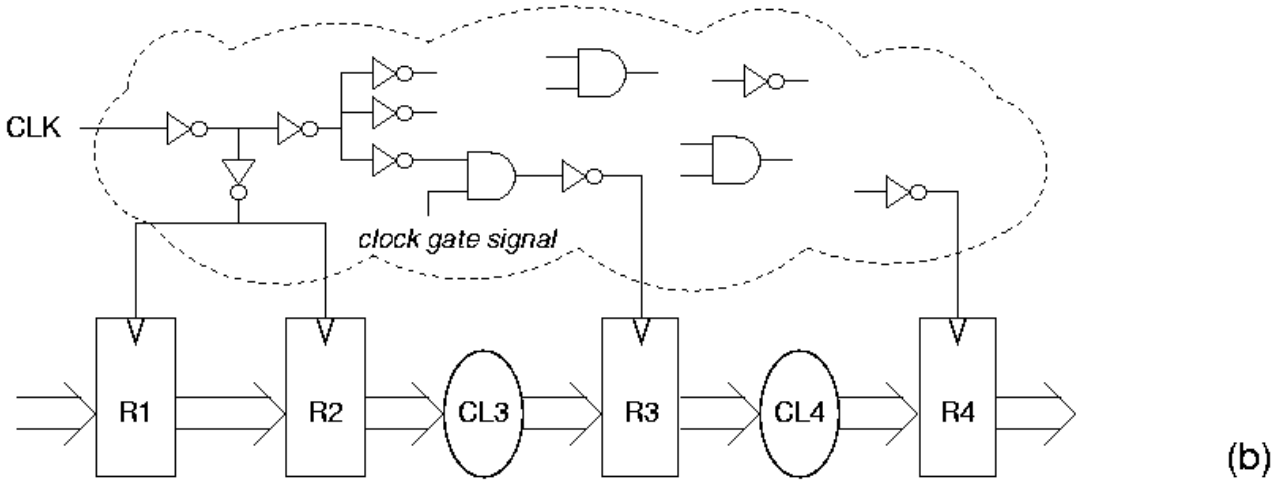
Synchronous clocking

How we think



(a)

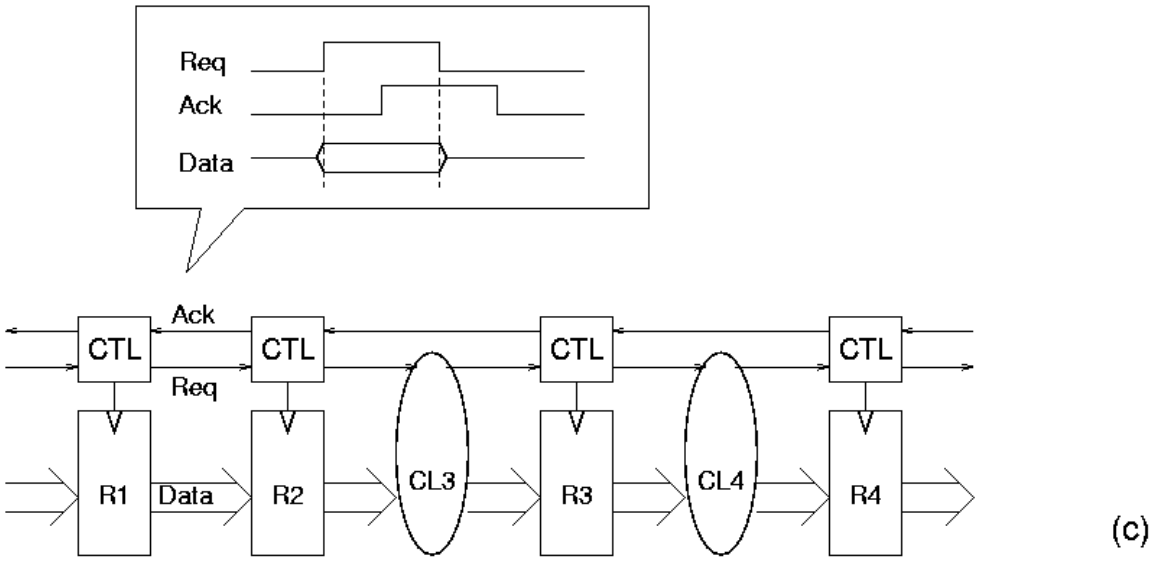
What we design



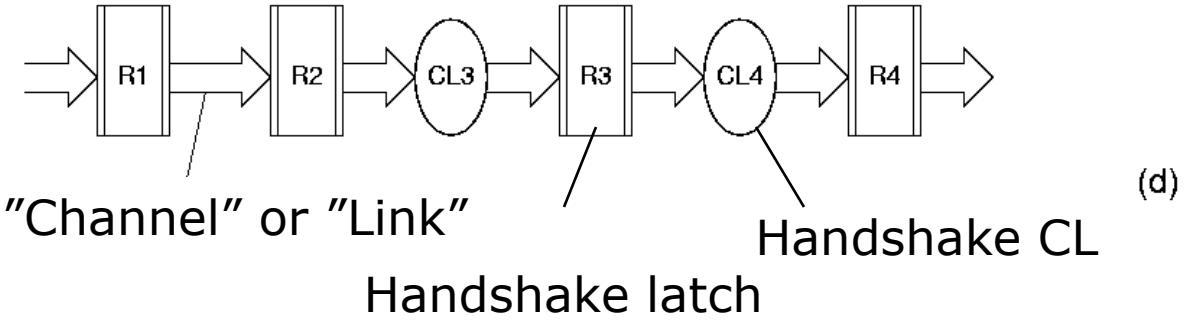
(b)

Asynchronous handshaking

What we design



How we think



Brief History of Asynchronous clocking

- In the 1950s there were no clocks in computers – they were ‘asynchronous’
- Theory of asynchronous switching circuits was created – David Muller et al from University of Illinois
- In the 1960s-70s circuits become more complex and designing them was easier with the clock
- In the 1980s VLSI circuits appeared and there began a battle between synchronous (circuits were complex to design and test; CAD tools started to appear based on clocked FSM paradigm) and asynchronous (interacting with the real world, metastability problems, working on average rather than worst case delays)

Brief History of Asynchronous clocking

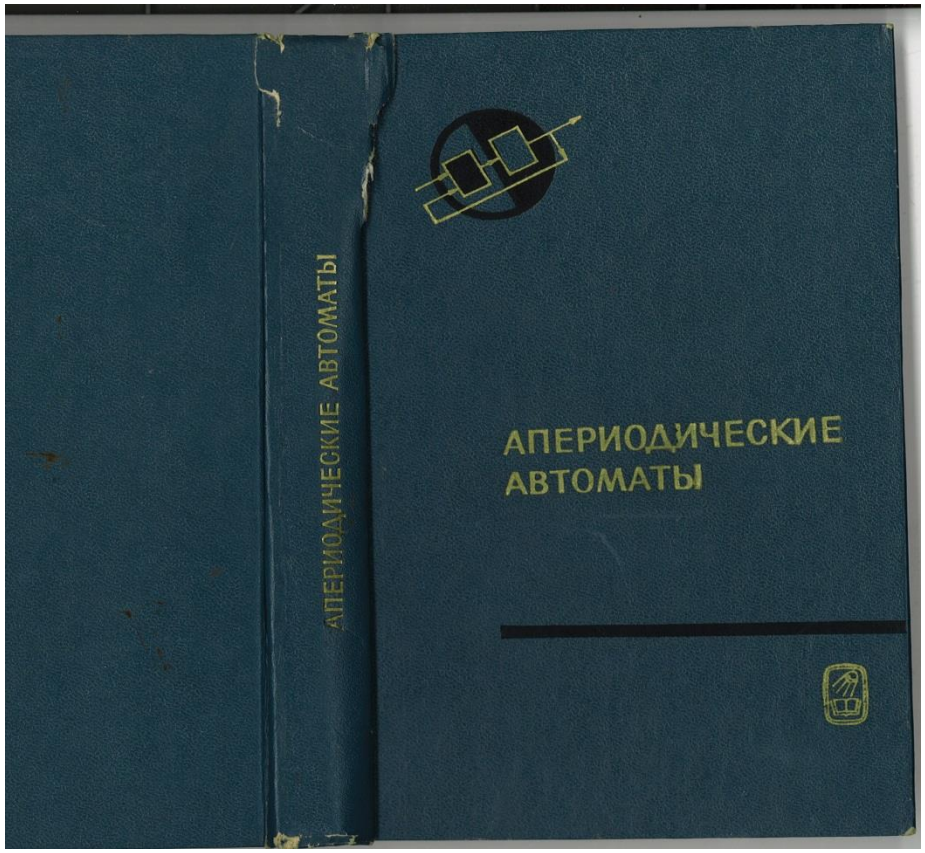
- In the 1990s drive for low power began and async gave some advantages; later the problem of design reuse came about and GALS approach was propose
- In the 2000s drive for robustness against PVT variations, security, noise and EMI reductions gave more drive to async
- In the 2010s multi Billion transistor chips design – many clock/Vdd domains, NOCS and GALS is a reality
- Push for ULTRA low power causes to work in near-threshold and subthreshold
- Analog-Mixed Signal comes on chip – needs little digital control – again asynchronous is important

LETI people in async world: back then

- Victor Varshavsky and his group
  - Early work of Varshavsky on digital systems and automata
  - 1970s: work in the USSR Academy of Sciences Institute of Economics and Mathematics (LOCEMI) and Institute of Social-Economic Problems (ISEP)
  - 1980: the group moves to LETI (MO EVM)
  - 1980s: the group develops methods for synthesis, analysis, new tools, first VLSI chips (FIFO in PLMs), multiprocessor systems (fault tolerant token ring interface for airborne onboard computers) -> first GALS system – 1986
  - Early 1990s: Trassa co-operative: libraries of modules, Trassa synthesis-analysis tools under MS DOS

Victor Varshavsky: pioneer of asynchronous design

The first book on asynchronous design



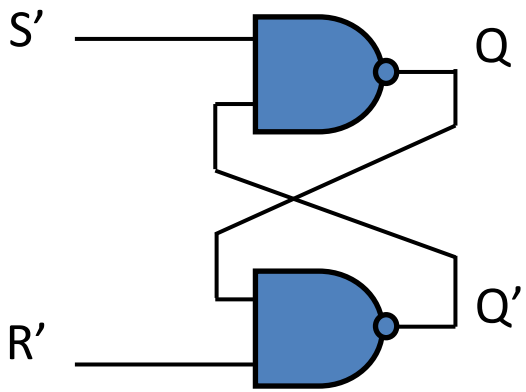
Aperiodic Automata, edited by V. Varshavsky, Nauka, Moscow, 1976

It contained:

Basic blocks with completion (flip-flops, registers, combinational)

Implementation of control (direct translation)

Asynchronous latches

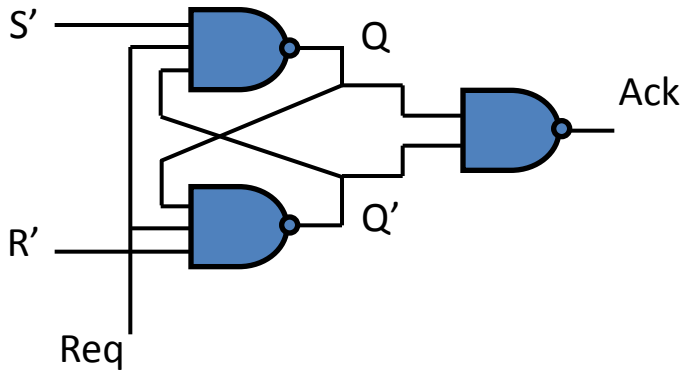


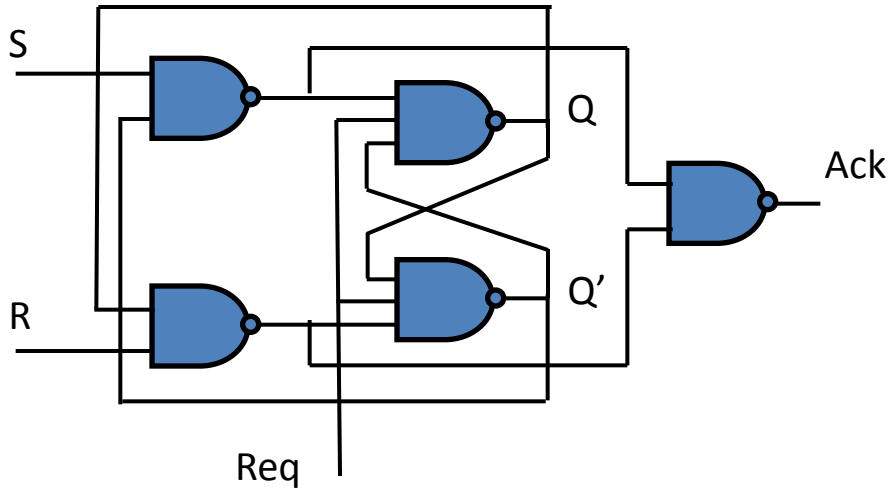
Classic RS-latch:
observing outputs cannot tell if operation
is completed

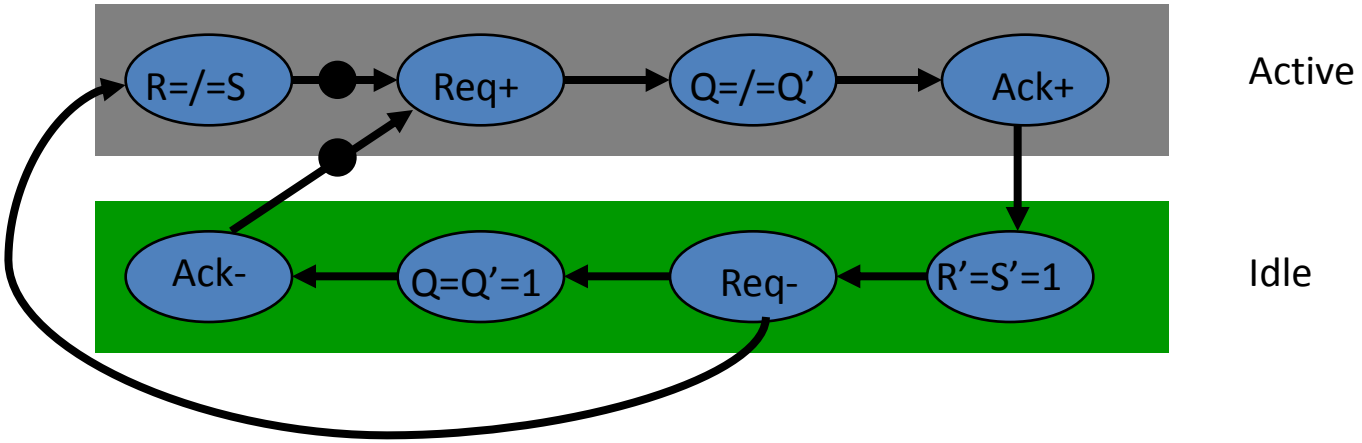
Completion detection

Partition computation into Idle and Active phases

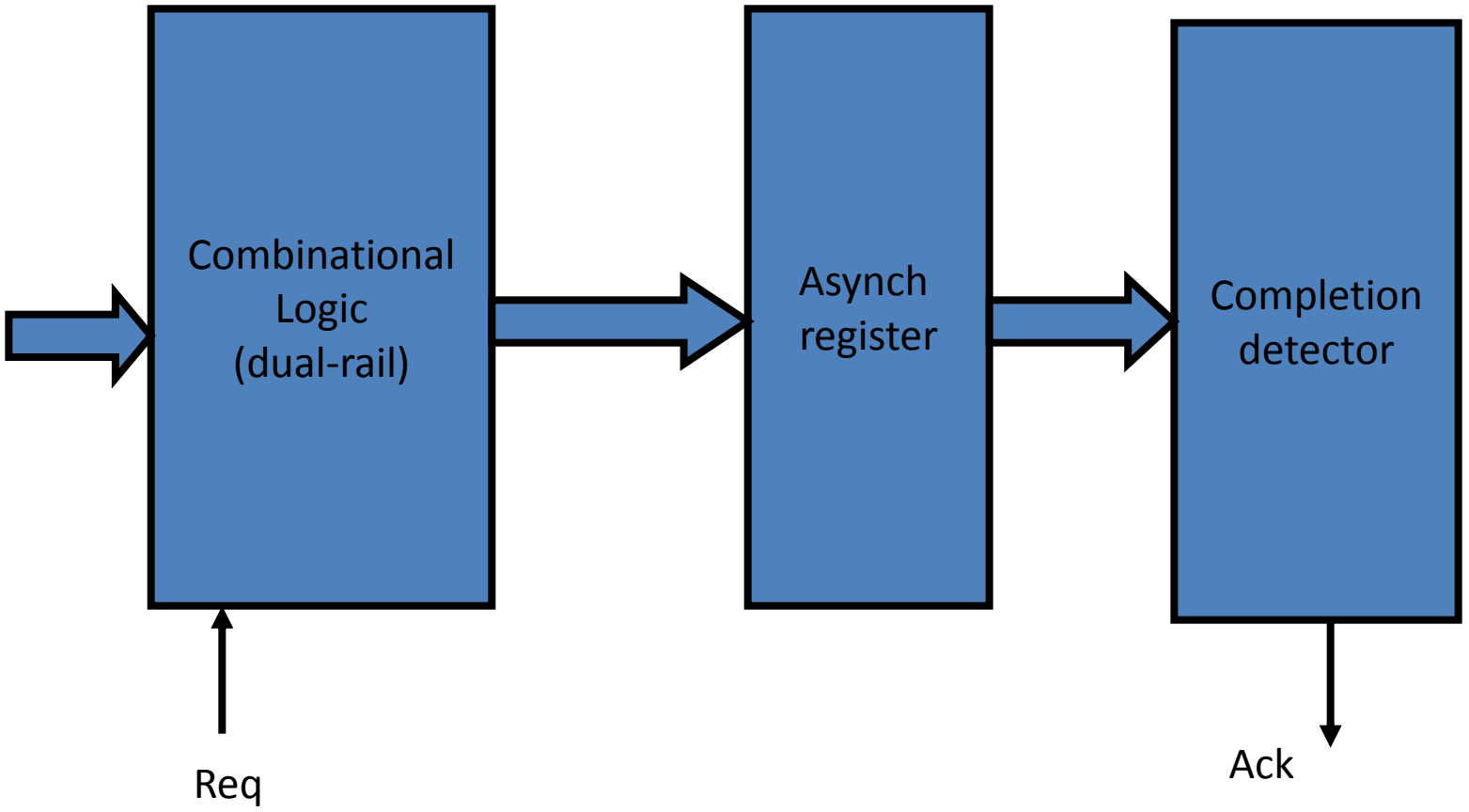
Asynchronous latches



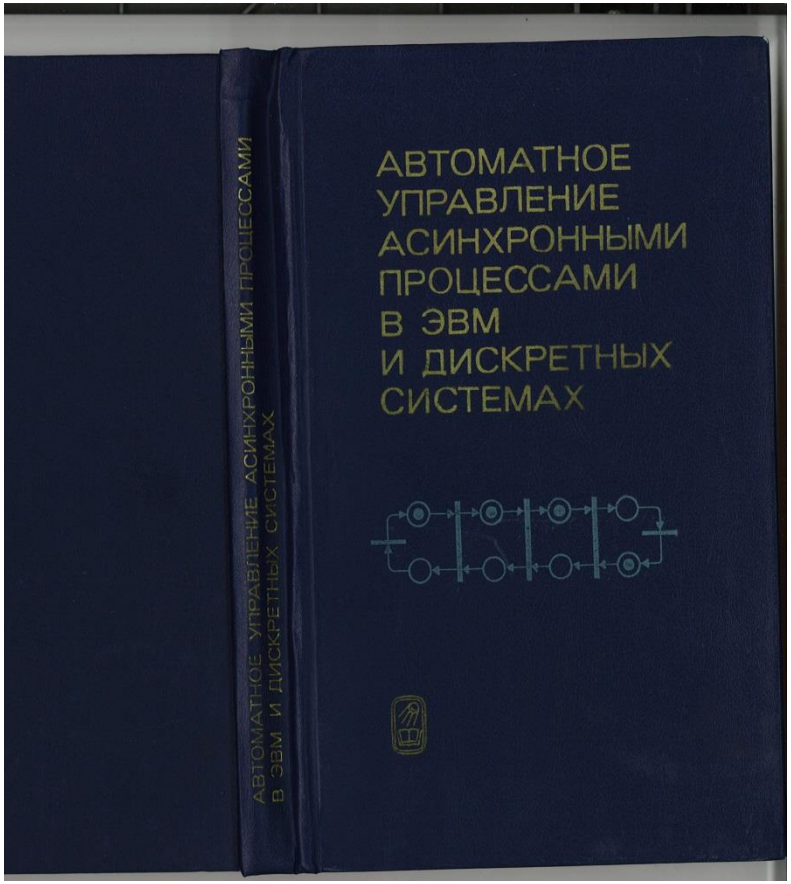


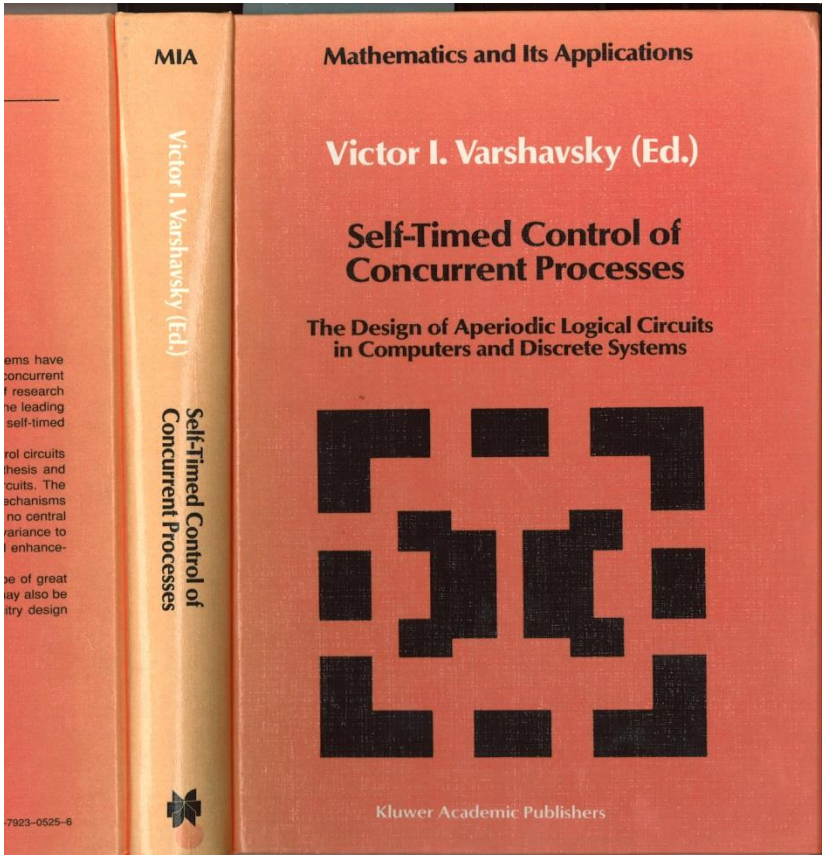


Two-phase asynchronous FSMs



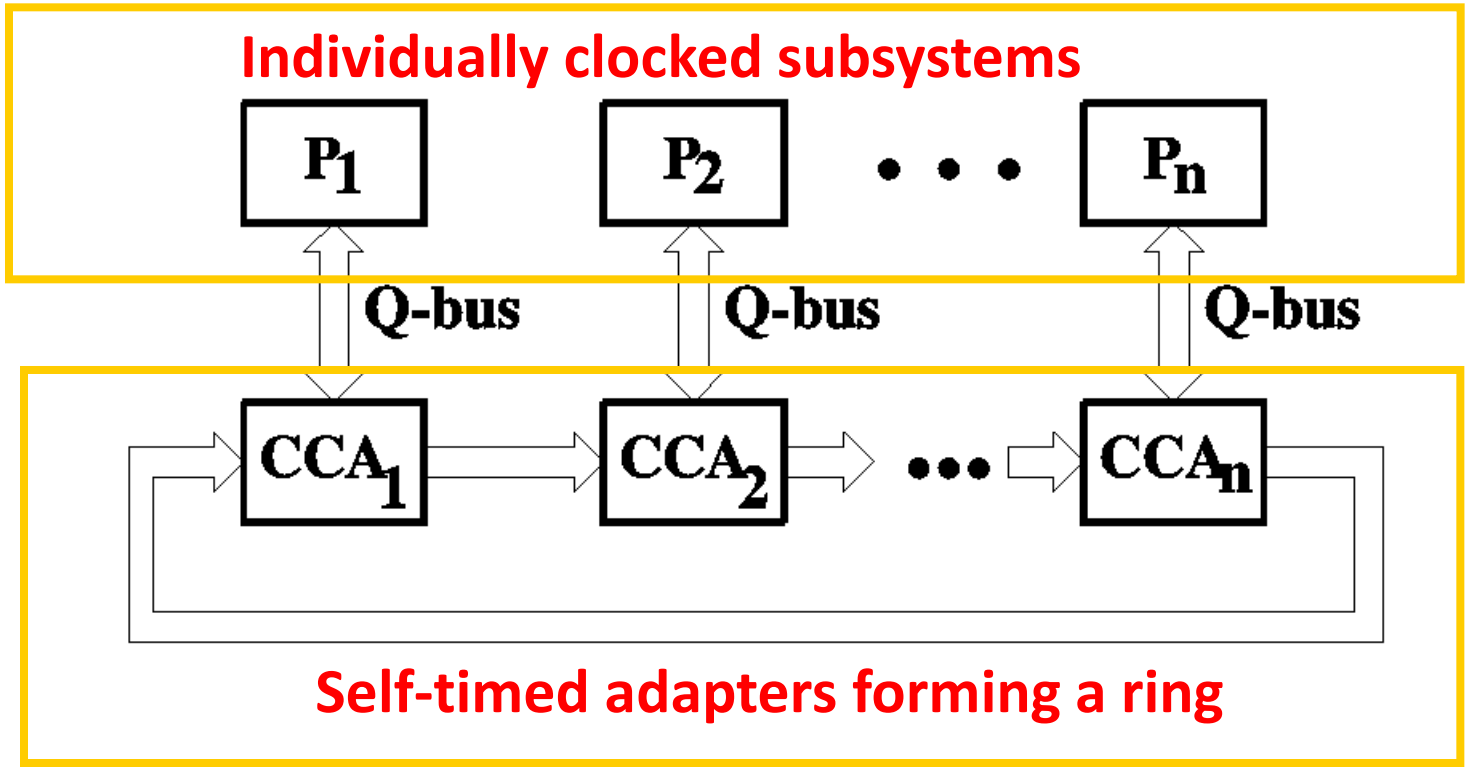
Second book (1986, 1990)



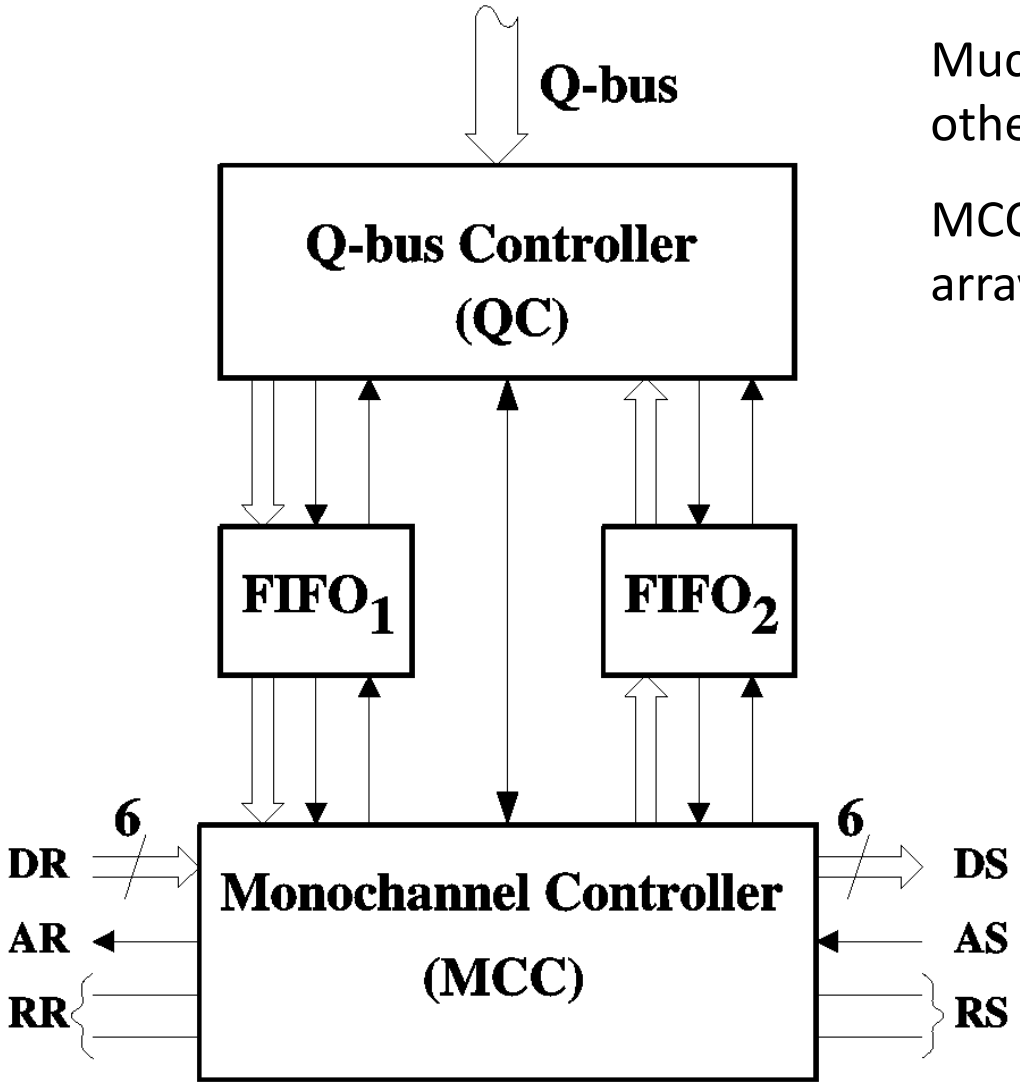


Fault-Tolerant Self-Timed Ring(1981-1986)

For an on-board airborne computer-control system which tolerates up to two faults. Self-timed ring was a ***GALS system*** *with* ***self-checking and self-repair at the hardware level***



Communication Channel Adapter



Much higher reliability than a bus and other forms of redundancy

MCC was developed TTL-Schottky gate arrays, approx 2K gates.

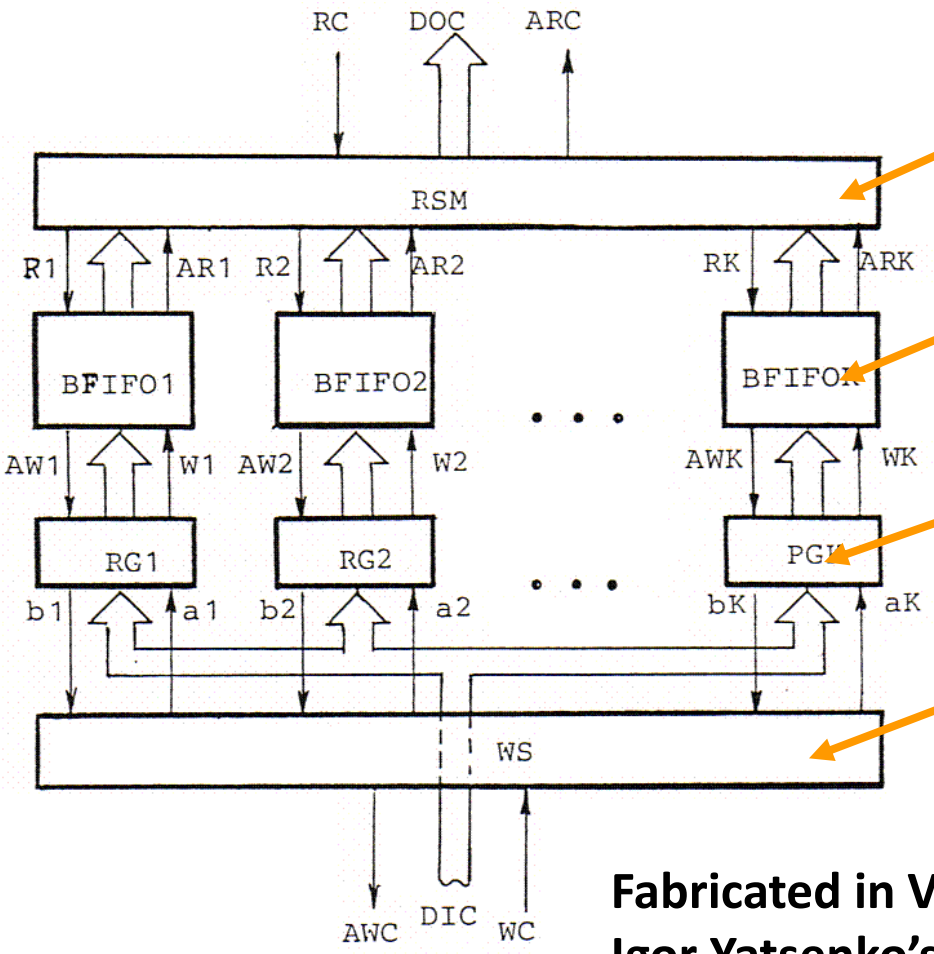
Data (DR,DS) is encoded using 3-of-6 Sperner code (16 data values for half-byte, plus 4 tokens for ring acquisition protocol)
AR, AS – acknowledgements
RR, RS – spare (for self-repair) lines

Self-Timed Ring published

- V.I. Varshavsky, V.B. Marakhovsky, L.Ya. Rosenblum, Yu.S. Tatarinov, V.Ya. Volodarskii, A.V. Yakovlev, **THREE papers** in Avtomatika & Vychislitelnaya Tekhnika, Control and Computer Science (Translated from Russian, Alerton Press), (1988-1989)
- A. Yakovlev, V. Varshavsky, V. Marakhovsky and A. Semenov, “Designing and asynchronous pipeline token ring interface”, Proc. 2nd Working Conf. on Asynch. Design Methodologies, London, May 1995, IEEE CS Press, N.Y., pp. 32-41, 1995.

Self-Timed FIFO (1985-1988)

Basic FIFO are connected using a wagging-tail buffer method



Read mux

Basic FIFO

Buffer registers

Write demux

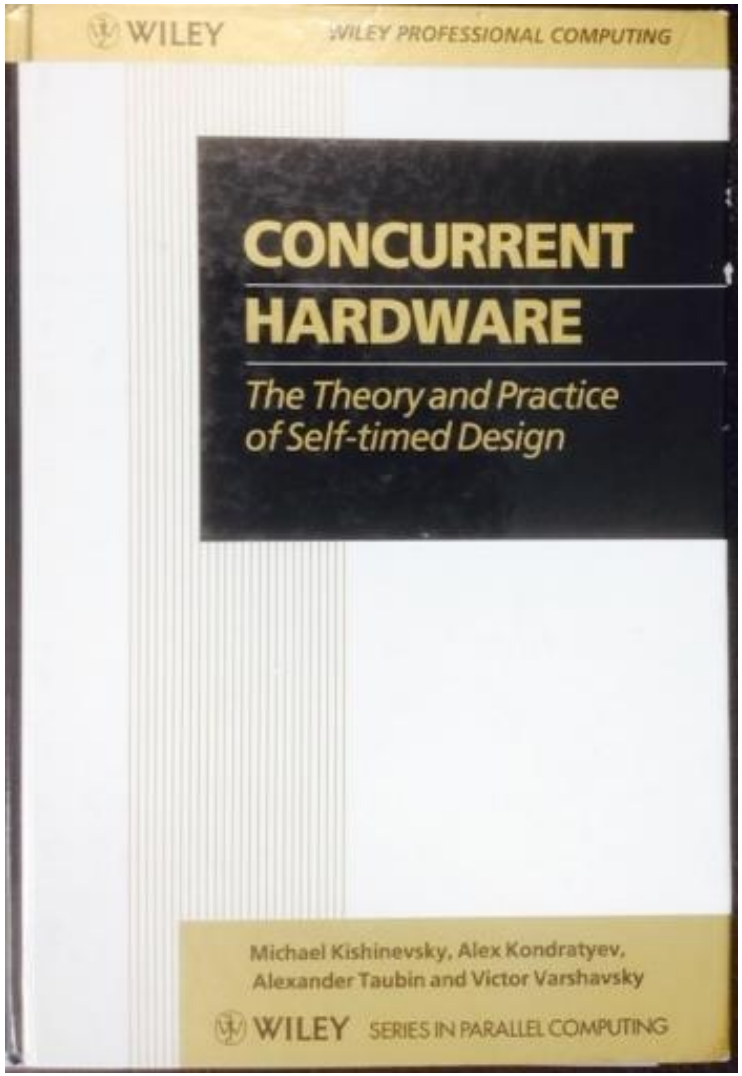
Throughput doesn't depend on the delay of Basic FIFO.

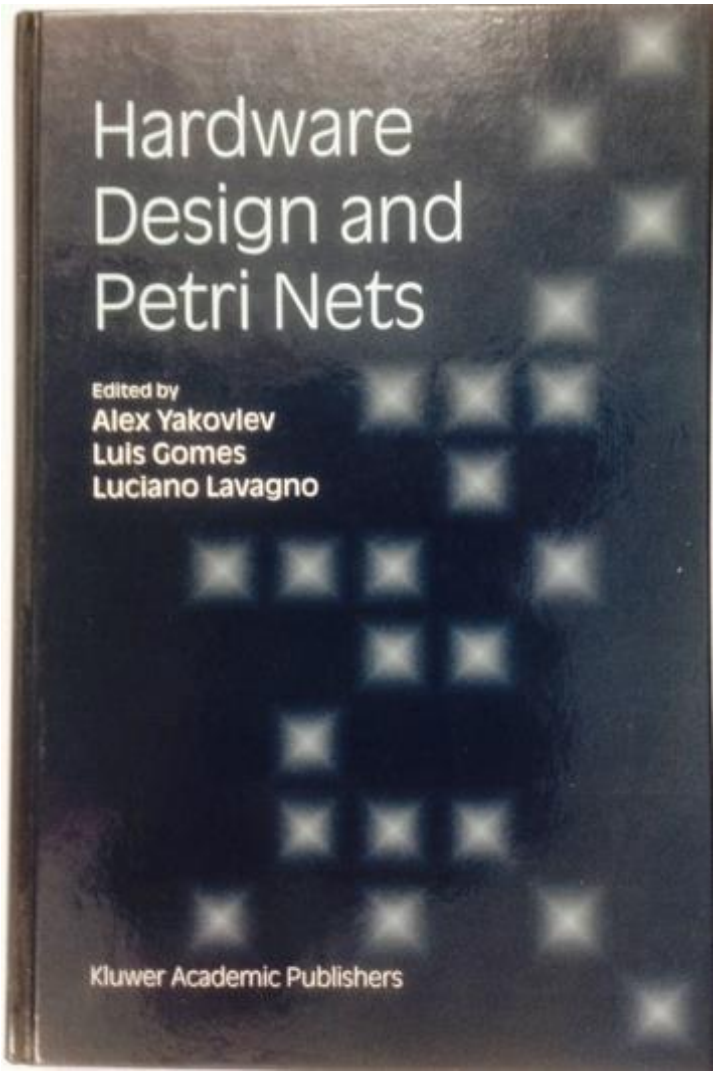
Fabricated in Voronezh, and fully described in Igor Yatsenko's PhD thesis, 1988

LETI people in async world: recent past

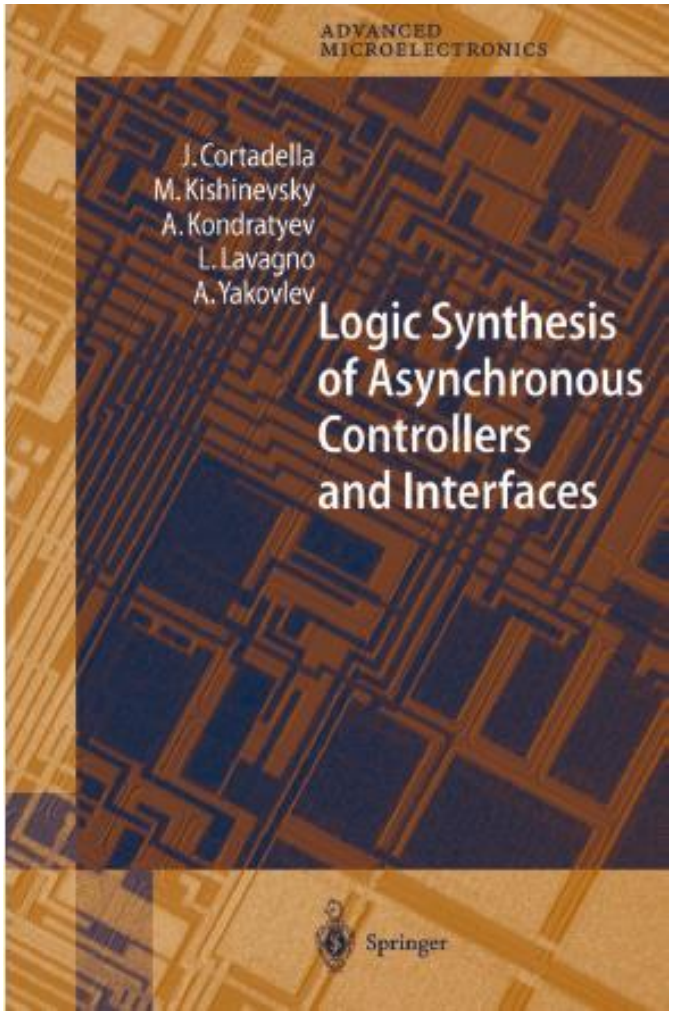
- From 1993: Varshavsky is in Univ of Aizu in Japan with part of his group (Marakhovsky, Kishinevsky, Kondratyev, Taubin)
- From 1990: Rosenblum is in the USA
- From 1991: Yakovlev is in the UK
- Starodoubtsev is in Russia (NTO of Academy of Sciences)
- Active work on synthesis and verification methods for STGs
- Collaboration between Yakovlev, Kishinevsky, Kondratyev, Taubin and Cortadella (Barcelona) and Lavagno (Turin)
  - Many papers in IEEE Transactions and leading confs: ASYNC, DAC
  - Software tool Petrify
  - Springer book published in 2002

Group's Books on Async Design



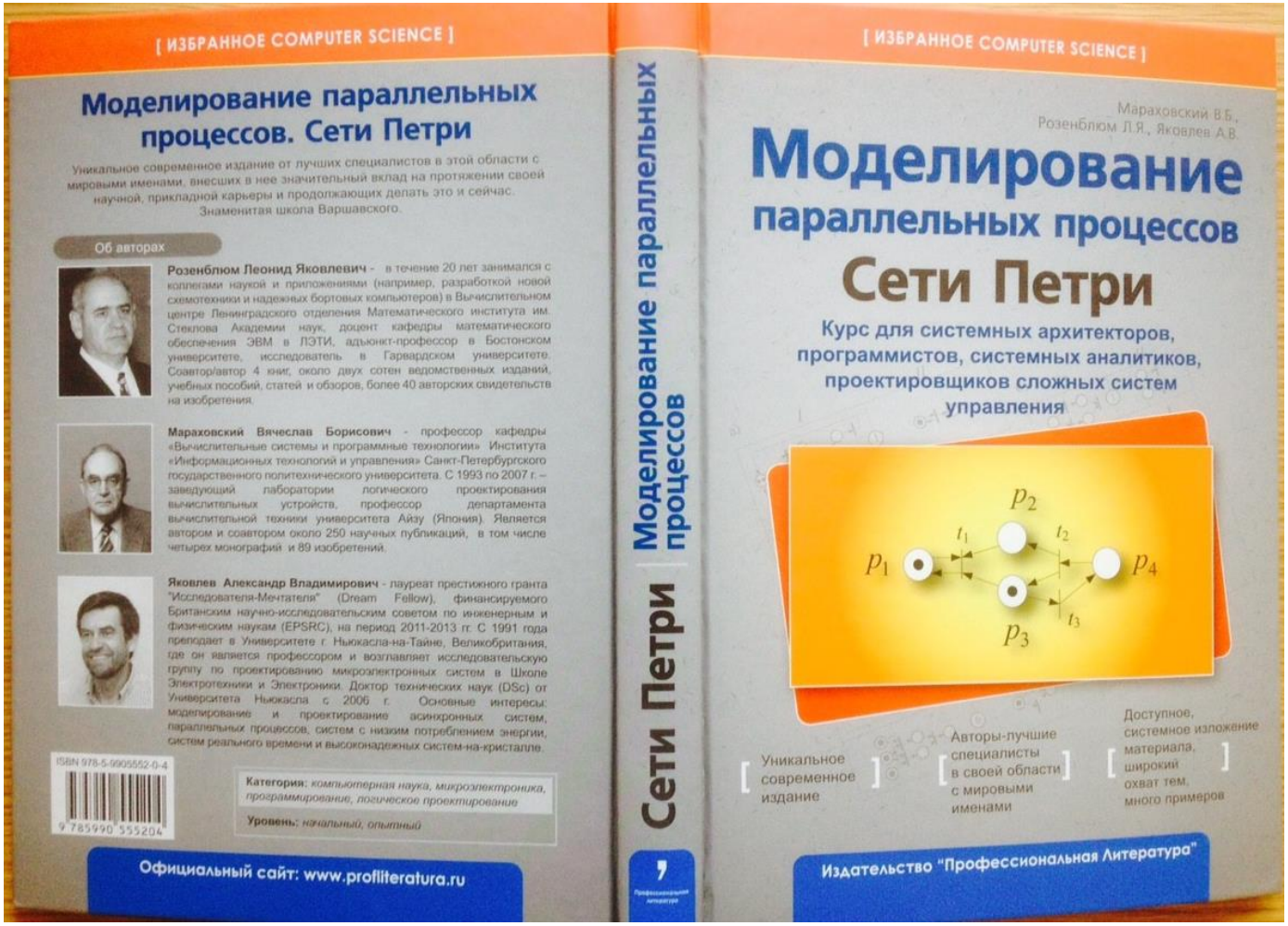


Book on Petrify Method and Tools



- The book on Signal Graphs Methods and tools.
- Collaboration with Cortadella (UPC Barcelona) and Lavagno (Turin, Cadence)
- Kishinevsky (Intel), Kondratyev (Theseus Logic, Cadence)

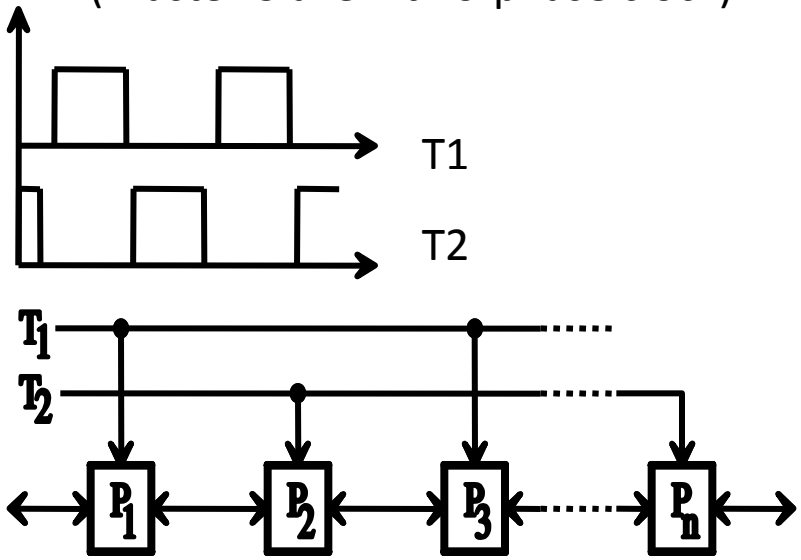
The most recent book from the group



Globally Asynchronous Locally Arbitrary (GALA,1995)

Synchronous

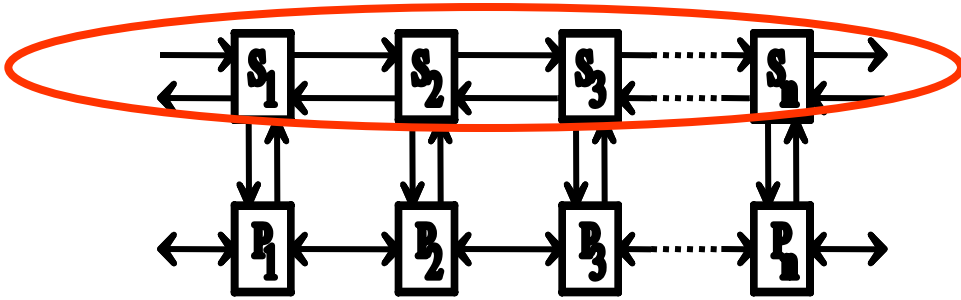
(Master-Slave + two-phase clock)



Asynchronous

Pk= F(P(k-1, t), P(k,t-1), P(k+1,t))

Synchrostratum



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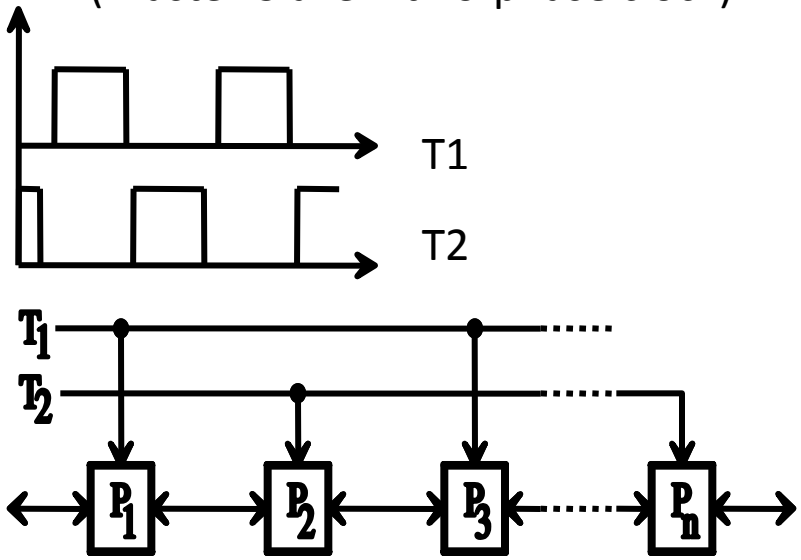

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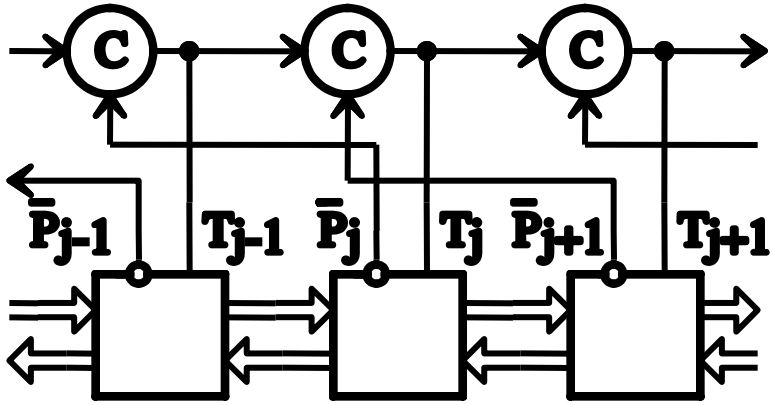


Applications:

Counters with constant response time

Arbiter-free counterflow pipeline

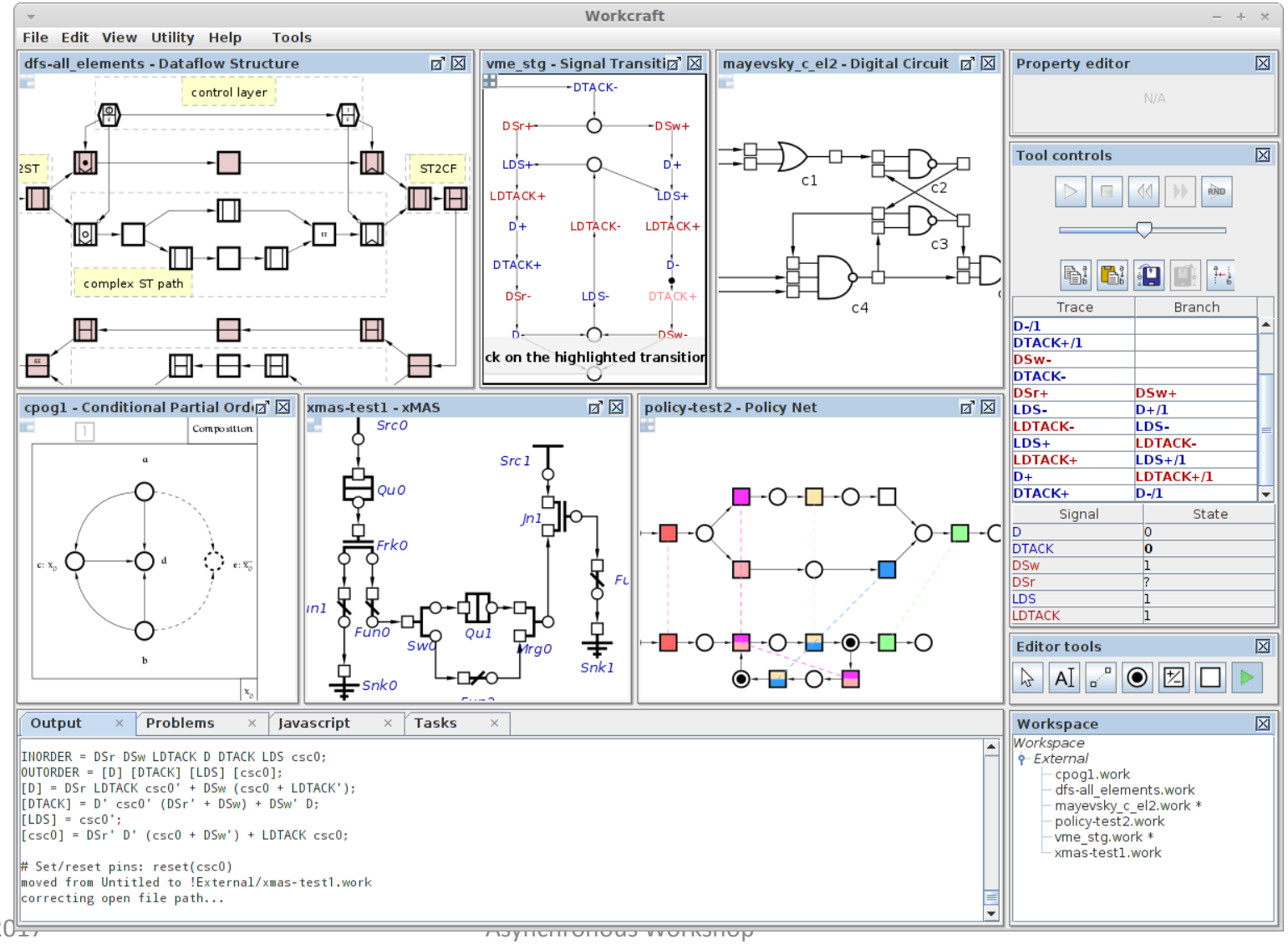
GALA published

- V. Varshavsky, V. Marakhovsky, "GALA (globally asynchronous - locally arbitrary) design" in Concurrency and Hardware Design Advances in Petri Nets, Springer, pp. 61-107, 2002.
- V. B. Marakhovsky and A. V. Surkov, "Globally asynchronous systems of interactive Moore state machines," in *IET Computers & Digital Techniques*, vol. 10, no. 4, pp. 186-192, 7, 2016.

Today: “LETI in Newcastle”

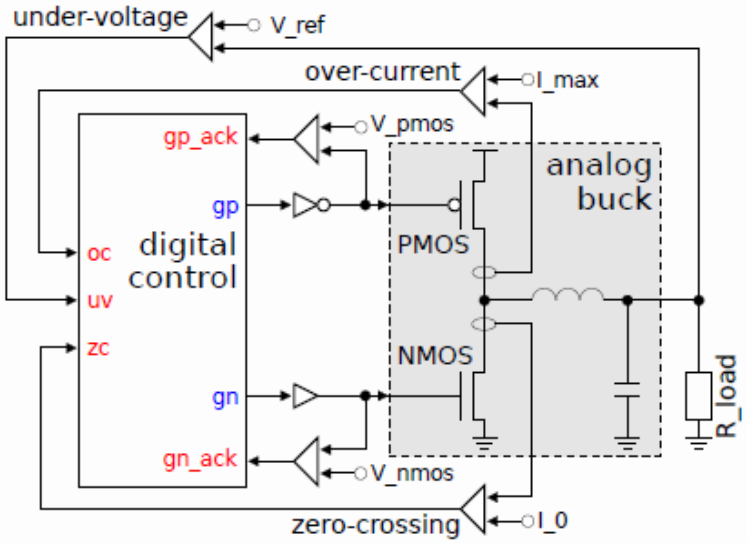
- Newcastle has now formed as the world leading centre of asynchronous research in the Microsystems research group, which produced more than 40 PhD graduates, 25 Research projects, mostly in asynchronous systems
- Industrial impact: Intel, Oracle, Atmel Smart Cards, Dialog Semiconductor
- Most recent success: asynchronous for analog (e.g. power converters)
- See http://async.org.uk
- Workcraft tools: http://workcraft.org
- Collaborations with researchers from several European Centres (e.g. **IHP - Germany**, DTU – Denmark, LETI (!) – France, IMEC – Belgium)
- Active development of methods for GALS

Workcraft toolkit

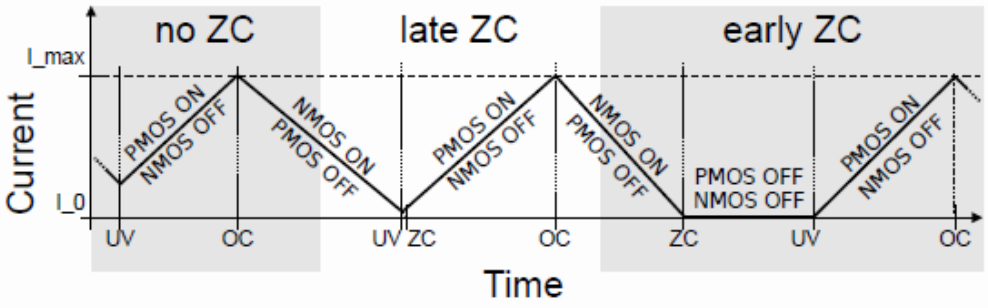


Asynchronous for Analog

- Buck converter control



Phase diagram specification:



Buck conditions:

- under-voltage (UV)
- over-current (OC)
- zero-crossing (ZC)

Operating modes:

- no zero-crossing
- late zero-crossing
- early zero-crossing

Electromagnetic Theory in Newcastle

- NEMIG interest group seminar – examples

HISTORY

- From a Spark to a Flame: Wireless Telegraphy in the North-East up to and including World War One - Dr. Elizabeth Bruton
- 150 Years of Maxwell's Equations - Dr John Arthur

THEORY

- The Challenges and opportunities for the characterisation and quantification of Stochastic Electromagnetic Fields - Prof. Dave Thomas
- Explicit Symmetry Breaking of an Electrodynamic System and Electromagnetic Radiation - Prof. Gehan Amaratunga -
- Non-abelian magnetic monopoles - Prof. Paul Sutcliffe

APPLICATIONS

- Perpendicular magnetic anisotropy: from ultralow power spintronics to cancer therapy - Prof. Russell Cowburn
- The Time Domain, Superposition, and How Electromagnetics Really Works - Dr. Hans Schantz

The Heaviside Memorial Project

- The aim was to restore interest to Oliver Heaviside and his role in science and engineering, and
- Restore his gravestone in Devon, England

www.theheavisidememorialproject.co.uk

Unveiling Ceremony

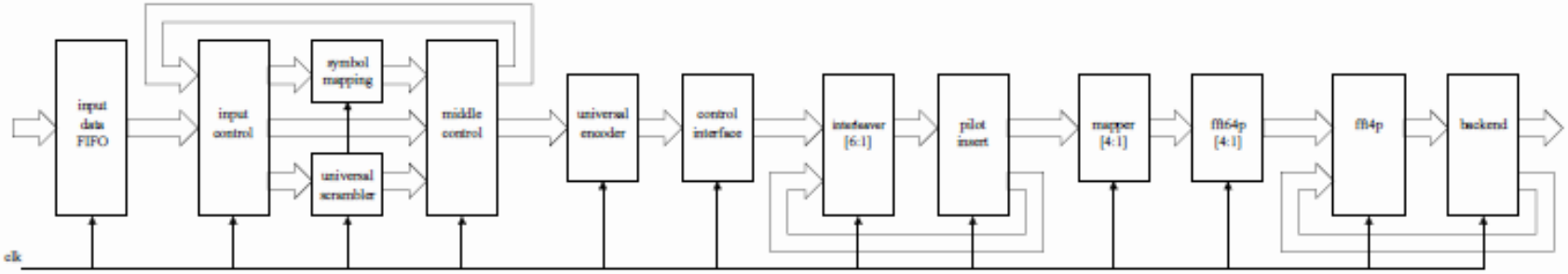
Ex-

Collaboration with Milos Krstic

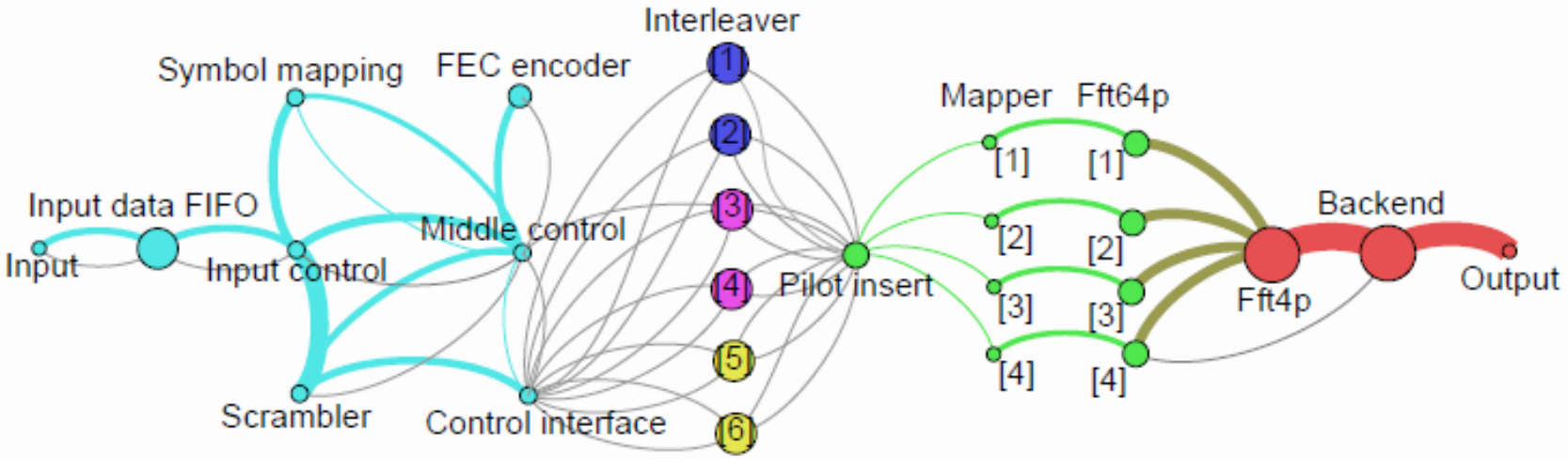
- GAELS project (involving Manchester University and IHP,Germany)
- Globally Asynchronous Elastic Logic Synthesis
- Design Automation for GALS

Clustering complex IC designs

- High-level schematic of IHP transmitter

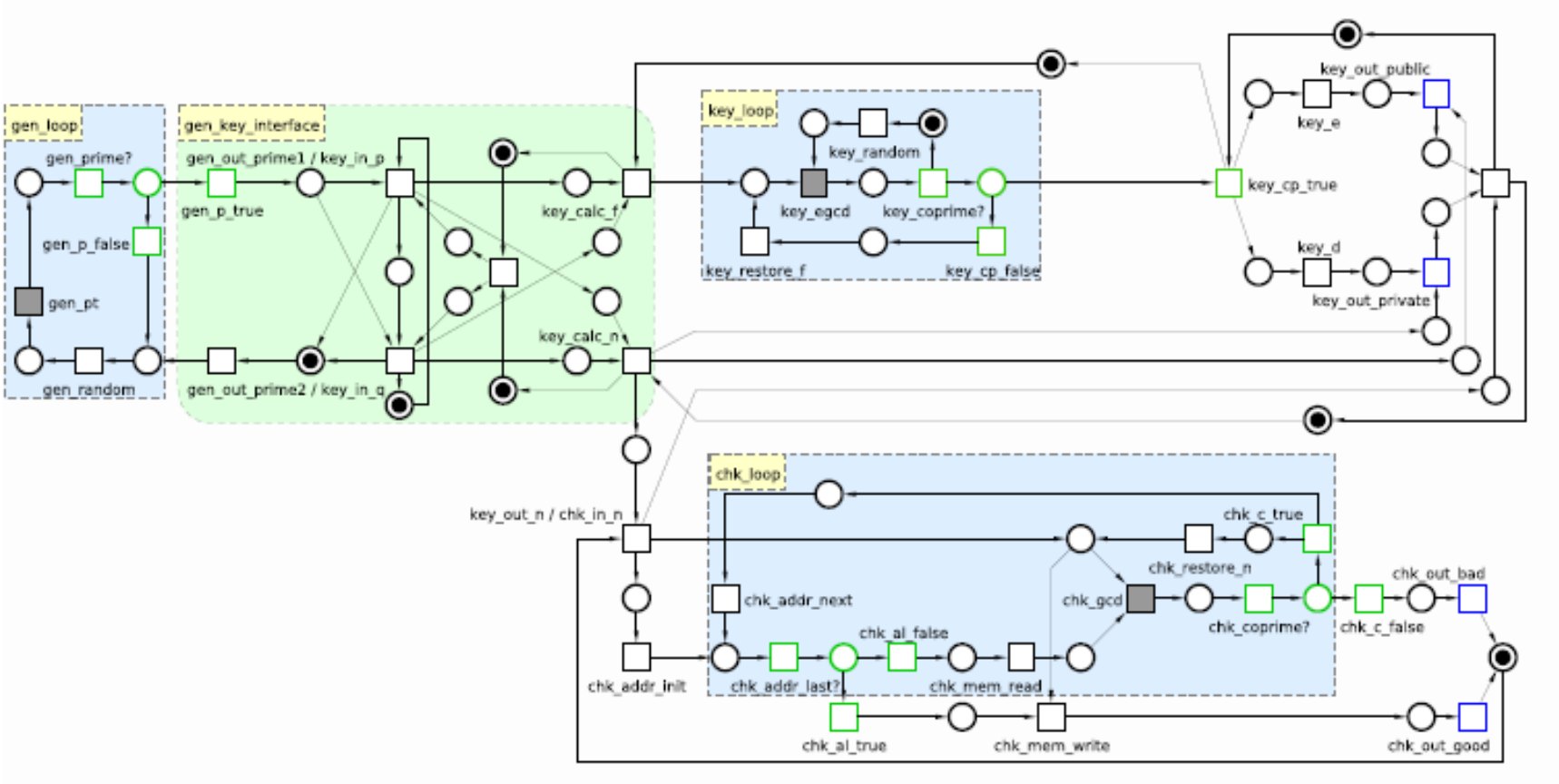


- Graph representation of IHP transmitter in Gephi

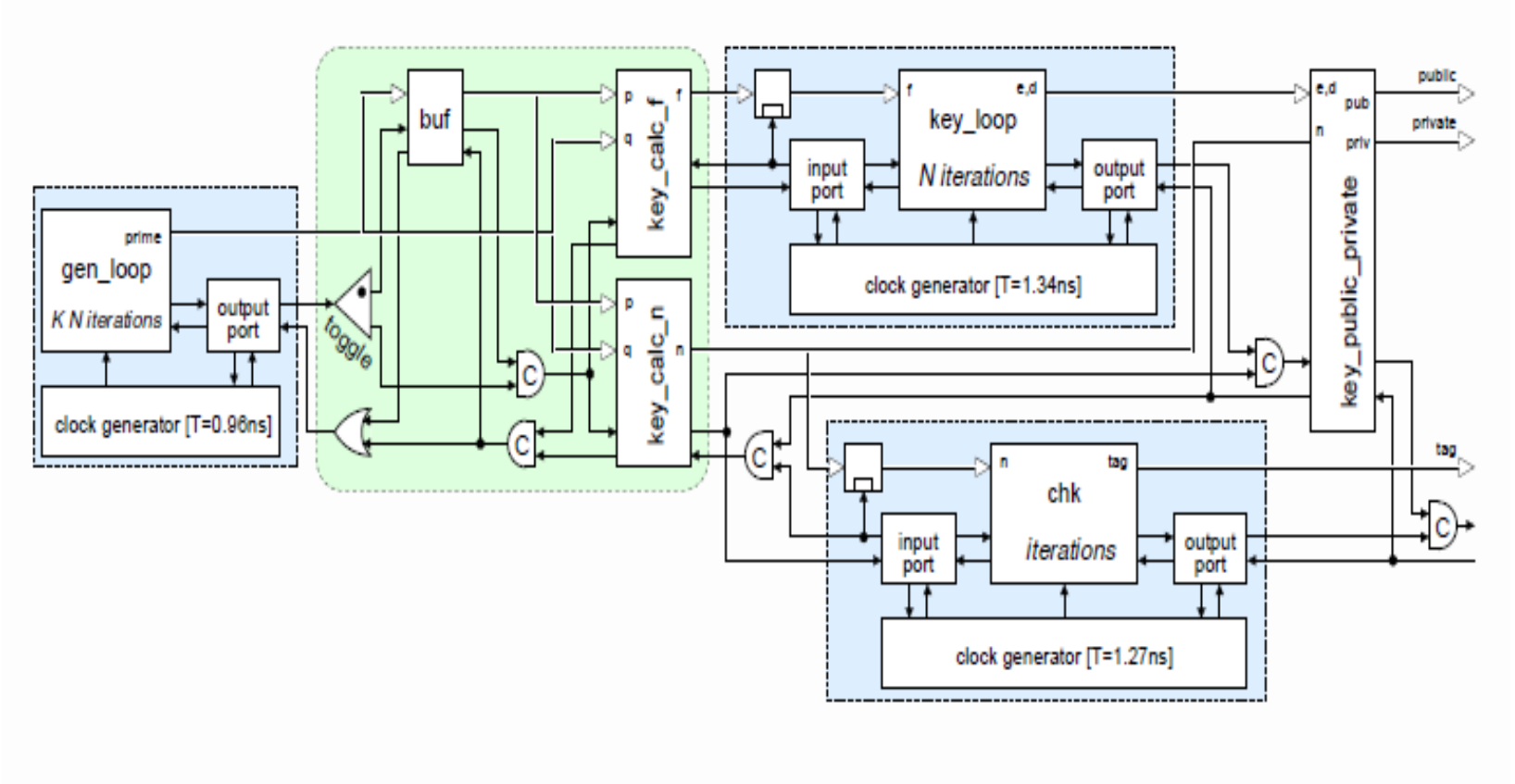


★ Colour encoding for 6 clusters ★ Node size for area ★ Edge width for interconnect

Modelling and design of GALS with Petri nets

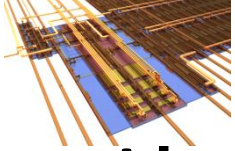
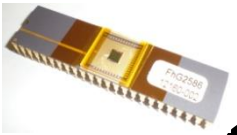


Implementation

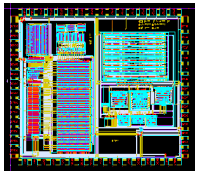
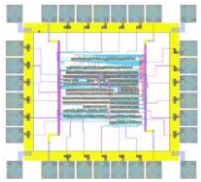
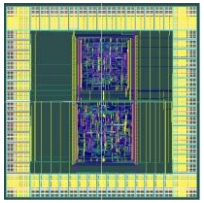
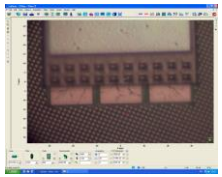
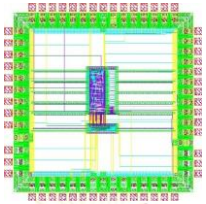
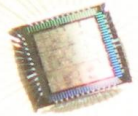


Now comes the talk of Prof Milos Krstic, IHP and Potsdam University

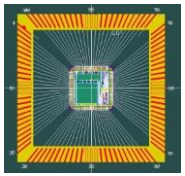
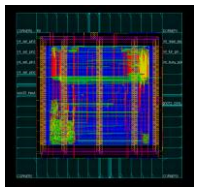
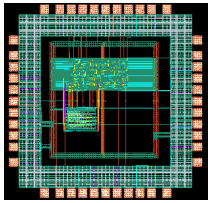
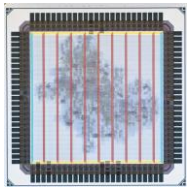
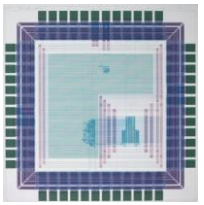
“**Reducing Switching Noise Effects by Advanced Clock Management**”

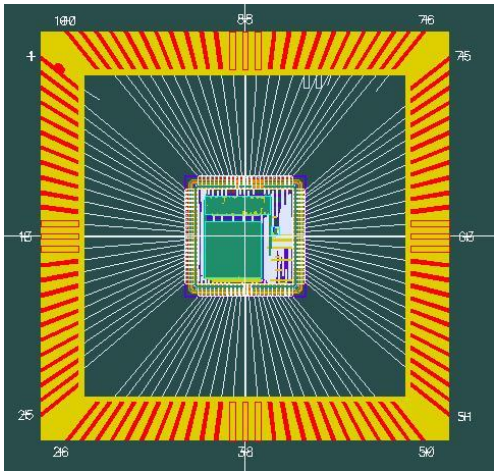

Newcastle Async Chip Designs

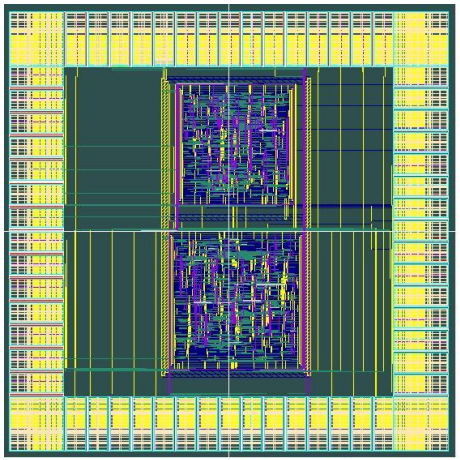
- Arbitration: HADIC1 (2000, CMOS 0.6um) – asynchronous arbiters, ADC, Async communication mechanism
- Time measurement: TMC (2003, CMOS 0.2um, collab. with Sun) time amplifier and time-to-digital converter
- Synchronization: SYRINGE1 (2006, UMC 0.18um), SYRINGE2 (2008, UMC, 0.13um) metastability measurement, robust synchronizer
- Security: SCREEN1 (2005, AMS 0.35um), SCREEN2 (2006, AMS 0.18um) AES cores with power balancing; SURE (2008, UMC 0.13um), Galois Encoded Logic, Script1 &2 (2010, TSMC 90nm)
- Networks on Chip: NEGUS1 (2007, UMC 0.13um), phase-encoding signalling, NeuroNOC (2009, TSMC 90nm) reconfigurable neural network, 3D-chip (2011, MIT Lincoln Labs, 150nm with TSVs)
- Energy harvesting: Holistic1 (2011, UMC 90nm), self-timed SRAM, Holistic 2 (2012, UMC 0.18um), reference free voltage sensor
- Power proportionality: Async 8051 (2013, STM CMP 0.13um)
- SAVVIE and A4A chips: to be reported

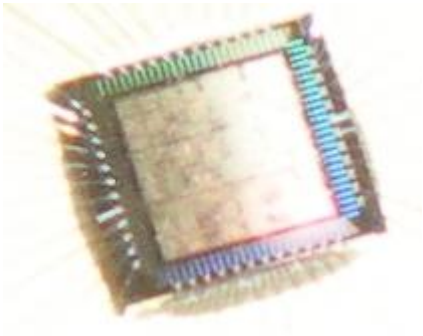
Some Security Chips



SCREEN1: AES encryption core design using alternating spacer dual-rail signalling for power balancing (generated from synchronous RTL using in-house tool VeriMap)

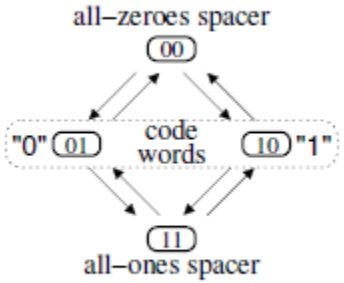


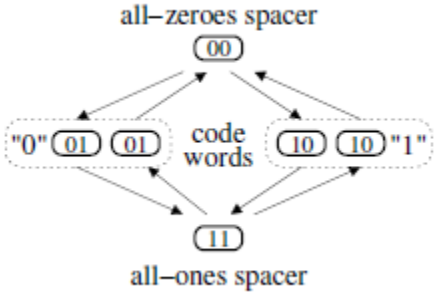
SCREEN 2: different (synchronous single-rail and power-balanced) versions of AES S-box.

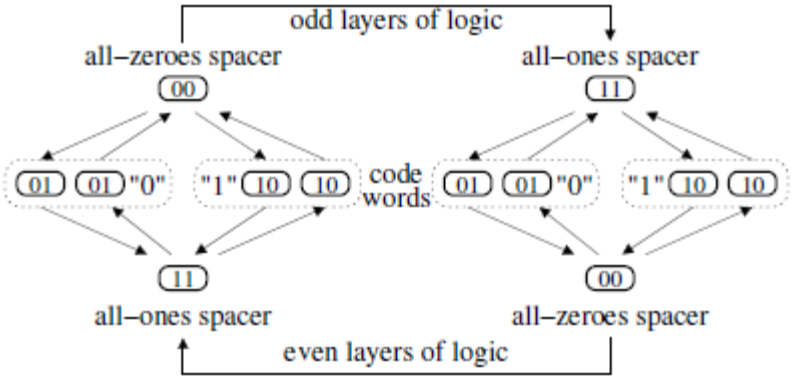


SURE: Galois Encoded Logic AES-128 IP core. Implements side-channel secure "high radix" AES-128 encryption in a fully parallel architecture to investigate the security and study the market feasibility of the technology.

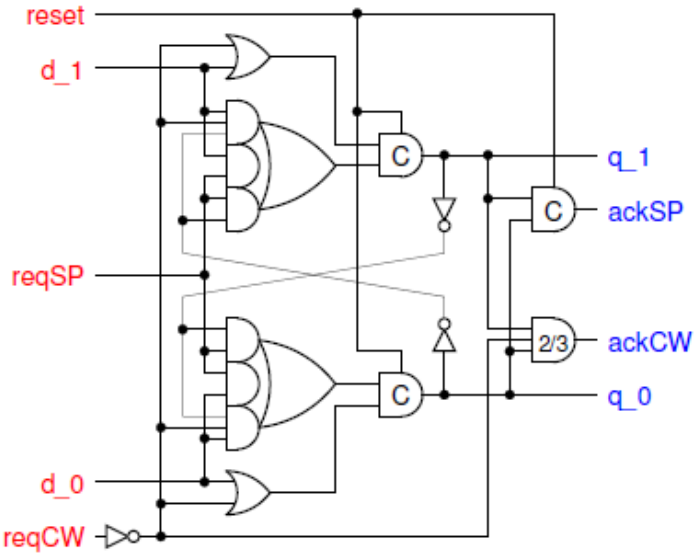
Verimap: Dual spacer and negative gate optimization

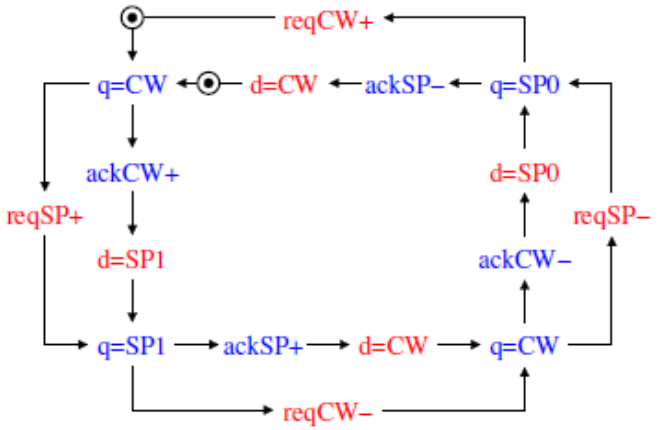






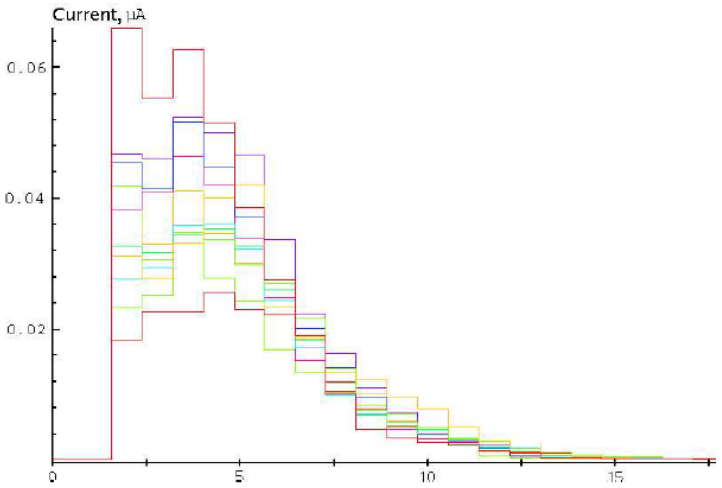
Alternating spacer dual-rail flip-flop



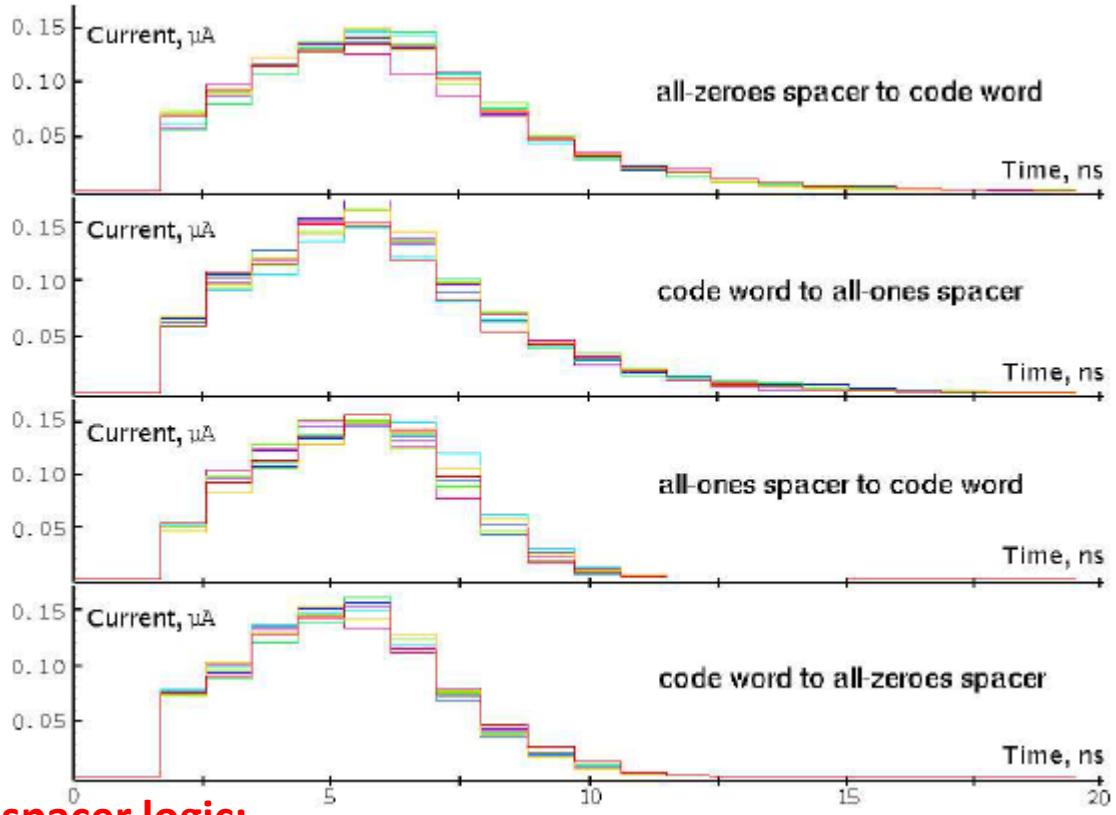


Example: Verimap AES design

Single Rail current trace



Dual Rail alternating spacer traces



Key property of dual-rail alternating spacer logic:

For every operational cycle of the circuit all logic nodes fire => maximum power balancing