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Basel Halak, Alex Yakovlev

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Contacts

basel.halak@ncl.ac.uk

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School of Electrical, Electronic & Computer Engineering,
Merz Court,
Newcastle University
Newcastle upon Tyne, NE1 7RU, UK

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Abstract*. The effect of crosstalk avoidance codes on the throughput of fixed width communication channels is studied. Closed form expressions of the throughput which incorporate the dimensions of the interconnects and the wires overheads by such techniques are derived for lines under different buffering conditions. These formulae are utilised to optimise the bandwidth of fixed width parallel buses under different latency and reliability constraints. Our results are confirmed by the simulations we have performed in Spectre for a UMC CMOS 90nm technology.*

1. Introduction

As VLSI technology progresses toward integration densities that will allow for more than a billion active devices per chip, the cost of high-speed wire networks will become excessive [1]. The economic demands to continue the exponential reduction in price per function will force the use of area efficient wiring methodologies that will require a shift from a low-density latency-centric global wire design to a high-density throughput-centric wire design [2]. The interconnect performance in current deep sub-micron technologies is greatly affected by crosstalk noise due to the decreasing wire separation and increased wire aspect ratio [1]. The capacitive crosstalk between adjacent wires significantly increases the propagation delays. This trend is anticipated to worsen in the future. Techniques to avoid the crosstalk delay have been proposed by many researchers [2-10]. These methods can generally be implemented on the physical or data link layers of the design or on both levels. Physical layer solutions include wire sizing optimisation and shield insertion [2-4]. The techniques implemented on the data link layer consist of data encoding to avoid crosstalk [5-10]. Although the use of crosstalk avoidance techniques improves the wire delay, it incurs wiring overheads, which may reduce the link throughput.

This paper explores the design tradeoffs of global interconnect architectures. The key question that we try to answer is, given a fixed area in which to distribute interconnect, what is the best arrangement of wires to obtain the highest bandwidth. Is it to use all the wires to send data at a low signalling frequency, or to implement crosstalk avoidance techniques to operate at a higher signalling frequency but with less number of wires? What effects does repeater insertion have?

Opportunities for achieving high throughput and area efficient links are revealed through the creation of new physical models for interconnect throughput. These new models incorporate the channel geometry (wires dimensions) and the wiring overheads incurred by crosstalk avoidance coding schemes (CAC's).

To the best of our knowledge the effect of CAC's on the throughput has not been addressed before.

The organisation of this paper is as follows; the derivation of the throughput formula for fixed width links is explained in section 2, in section 3 we propose a new throughput optimisation methodology which takes into accounts the design constraints of the communication link, we considered three types of buses; *Throughput-centric, Latency-constrained and Reliability-constrained channels*, in section 4 our throughput model is employed to find optimum combination of wire sizing solutions and crosstalk avoidance methods that maximise the throughput for links under different design requirements and buffering conditions, in section 5 we briefly summarise the simulations we performed in Spectre for *UMC CMOS 90nm* technology section 5. Finally conclusions are drawn in section 6.

2. Model Derivation

2.1. Throughput

Throughput in this article refers to the number of data bits per second that is delivered over a physical link. It is the product of the number of data carrying wires and the clock frequency. The latter depends on the worst-case wire delay. The maximum frequency of the channel is given as follows:

$$f_{max} = \frac{1}{\eta * D} \quad (1)$$

where D is the worst case wire delay, which is widely accepted to be the 50% propagation delay of signals. η is a safety factor which depends on the application [12], and on the variability of wire delays. We chose the value of η to be 1.5 in order to account for the 50% expected variability of wire parasitic in future technology as indicated in [1]. For an *n*-wire communication channel, the bandwidth (throughput) can be calculated as follows:

$$BW = n * f_{max} \quad (2)$$

For communication links with a fixed width (*cw*) (see figure 1), the total number of wires is a function of the wire width (w) and spacing (s). This can be written as follows.

$$n = \frac{(cw / w_{min}) - s}{w + s} \quad (3)$$

where w_{min} is the minimum wire width, w and s are multiple of w_{min}.

If crosstalk avoidance codes are used to reduce the wire to D', the number data carrying wires will be decreased, the bandwidth of an encoded channel is given as follows.

$$BW = \frac{cr * n}{\eta * D'} \quad (4)$$

where *Cr* is the coding rate of the crosstalk avoidance code, it can be calculated as the ratio between the number of data carrying wires and the total number of wires available in the channel.

2.2. Wire Parasitic Elements

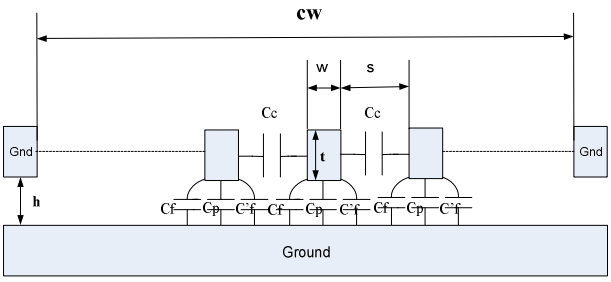

Fig.1: Cross Section of Global Interconnect

To perform timing analysis, it is essential to translate interconnect layout and technology information, such as the width and length of the wire, neighbouring line conditions and related dielectrics, into electrical parameters. This is achieved through parasitic extraction. Based on the design and technology

specifications, a physical line is usually converted into a netlist composed of resistors (*R*), capacitor (*C*), and if necessary inductors (*L*). On chip interconnect structures are usually composed of metal lines with rectangular cross sections [13], [14]. For a uniform metal line of width *w* and thickness *t* (figure 1), its dc resistance per unit length can be calculated as

$$R = \rho \frac{1}{w * t} \quad (5)$$

where ρ is the metal resistivity.
Capacitances extraction is done using the following formulae proposed in [15], which proved to have a good accuracy in deep sub micron geometries (see figure 1).

$$Cf = \varepsilon_k \left[.075\left(\frac{w}{h}\right) + 1.4\left(\frac{t}{h}\right)^{0.222}\right] l \quad (6)$$

$$C'f = Cf\left[1 + \left(\frac{h}{s}\right)^{\beta}\right] \quad (7)$$

$$Cp = \varepsilon_k \frac{wl}{h} \quad (8)$$

$$Cg, mid = Cp + 2C'f \quad (9)$$

$$Cc = Cf - C'f + \varepsilon_k \left[.003\left(\frac{w}{h}\right) + 0.83\left(\frac{t}{h}\right) - 0.07\left(\frac{t}{h}\right)^{0.222}\right]\left(\frac{h}{s}\right)^{1.34} l \quad (10)$$

where β is a technology constant which is calculated from a database of values generated by a field solver. Typical values of β range from 1.5 to 1.75, and 1.65 may be used for most deep submicron technologies [2, 15].

The accuracy of these equations is reported to be over 85% when the following inequalities are satisfied.

$$0.3 < \left(\frac{w}{h}\right) < 30 \; ; \; 0.3 < \left(\frac{t}{h}\right) < 10 \; ; \; 0.3 < \left(\frac{s}{h}\right) < 10$$

Inductance is a single measure of the distribution of the magnetic field created by a current. Inductive coupling is a long range effect because magnetic fields penetrate well beyond the metal surface and decay very slowly with increasing line spacing.
Therefore, the extraction analysis should include all neighbouring lines that are possibly involved in the current loop [14]. Since the consideration of *L* usually requires very expensive computation, it is desirable to include *L* only when it is necessary. From the standpoint of signal timing the importance of the inductance can be determined by three time constants, namely; the driver input signal slew rate *tr*, the time of flight of the transmission line ($tf = wire\ length * \sqrt{lc}$) and finally Elmore delay of an RC line ($te = (wire\ length)^2 * rc/2$). As a figure of merit the interconnect should be modelled as *RLC* lines if they satisfy the following two conditions:

$$\frac{tr}{2} < tf \quad and \quad te < tf$$

Translated into relationships between the interconnect length and *RLC* components, these two conditions can be summarised as:

$$\frac{tr}{2\sqrt{lc}} < \text{Wire Length} < \frac{2}{r}\sqrt{\frac{l}{c}} \quad (11)$$

The inductance can be ignored if the constraint on the left-hand side is larger than that on the right-hand side.

To assess the importance of the inductance in future technologies, we calculated the lower and upper bounds of the wire length, defined in equation (11), for several technologies. The wire width was considered to be 6 times the minimum width specified for each technology in order to magnify the inductance impact. The spacing was set to be equal to the wire width. The wire thickness and height were two times the minimum width. The wire parasitic components R, L and C were calculated using the predictive technology model (PTM) [16]. The results are shown in figure 2.

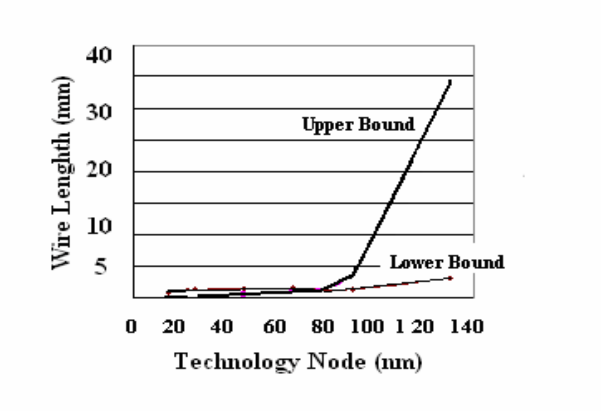

Fig.2: The Importance of Inductance in Future Technology

It can be seen that for the specified wire geometry, the region within which the inductance should be taken into account does not exist for technologies smaller than 65nm. This is due to the shrinking in the dimensions of wires, which leads to a sharp increase in their resistive loss [1], which in most cases masks the inductance effect.
Therefore in this analysis we will consider the distributed RC model of the interconnect.

2.3. Wire Delay

The RC propagation delay of waveforms on un-buffered lines can be calculated as follows.

$$D = 0.4*R*(Cg + pCc)(wire\ length)^2 \qquad (12)$$

where p is the worst-case capacitive switching factors which depends on the transitions activities on adjacent lines, Table 1 summarise the values of p on the middle lines in three wire bus for different transition patterns. Note that ↑, ↓, and −,denote 0-to-1, 1-to-0, and no transitions, respectively. *d0* is the delay of a crosstalk-free line.

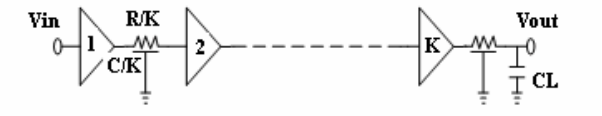

Fig.3: A Uniformly Buffered RC Modelled Wire

The delay of a uniformly buffered lines is calculated by the following expression denoted (13).

$K\left[\frac{0.7Rd}{H}\left(\frac{Cg+PCc}{K}+KCd\right)+\frac{R}{K}\left(\frac{0.4Cg+0.4PCc}{K}+0.7HCd\right)\right]$ where Cd and Rd are the input capacitance and output impedance of a minimum sized buffer [14].
K, H are the number of buffers and their sizes respectively see figure 3.

Table 1: Wire Delay for Different Crosstalk Cases

Crosstalk Case	Transitions	The Coupling Factor *p*	The Middle Wire Delay
1	↑↑↑, ↓↓↓	0	d0
2	↑↑- ,↓↓-, -↑↑, -↓↓	1	$(1 + \lambda)d0$
3	-↑- , -↓-, ↓↑↑ , ↑↓↓ , ↑↑↓, ↓↓↑,	2	$(1 + 2\lambda)d0$
4	↓↑-, -↓↑, -↑↓, ↑↓-	3	$(1 + 3\lambda)d0$
5	↓↑↓, ↑↓↑	4	$(1 + 4\lambda)d0$

For optimally buffered lines the values of *K* and *H* depends on wire dimensions and worst-case capacitive coupling factor. They can be calculated as follows [2].

$$K_{opt} = \left[\frac{0.4\,RCg + 0.4\,RCc * p}{0.7\,RdCd}\right]^{0.5} \quad (14)$$

$$H_{opt} = \left[\frac{0.7\,RdCg + 0.7\,RdCc * p}{0.7\,RCd}\right]^{0.5} \quad (15)$$

2.4. Coding Rate

Crosstalk avoidance codes (CAC's) achieve delay reduction by reducing the worst case delay of a bus from $(1 + 4\lambda)\ d0$ to $(1 + p\lambda)\ d0$, where $p = 1, 2,$ or 3 is the worst-case capacitive coupling factor on the encoded bus *p*, these codes are usually characterized by this factor. For an *n* wire link, the coding rate of linear CAC's is a function of *n* and *p*, however*;* for wide buses (*n*> *8*),the coding rate dependency on the number of wires *n* is very weak and can be neglected. Using curve fitting techniques [17], the expression of *Cr* as a function of *p* has been derived as shown below.

$$Cr = 0.2355 * e^{(0.3586*p)} \quad (16)$$

The coding rates of non-linear CAC's have a strong dependency on the number of wires in the channels as can be seen in figure 2 [11]. To simplify our analysis we consider the range of links ($32 < N < 64$) where in the coding rate dependency on the number of wires is negligible. Using curve fitting techniques the expression of *cr as* a function of *p* has been derived for the specified range (see (17)).

$$Cr = 0.4145 * ln(p) + 0.4128 \quad (17)$$

Table 2 shows a comparison between the coding rates of CAC's calculated in [11] and those calculated using our curve fitting techniques. Row 2 represents the maximum capacitive coupling factor on an encoded bus. It can be seen that the difference between the two figures are less than 3%.

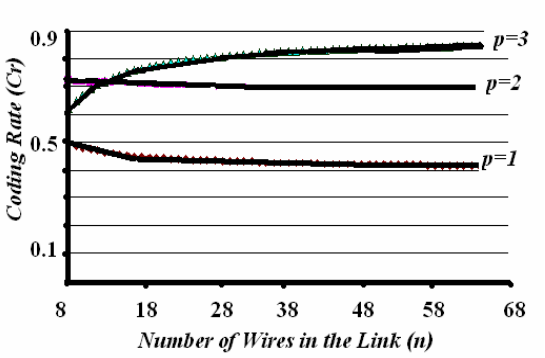

Fig.4: The Non-Linear CAC's Coding Rate

Table2: The Coding Rate of CAC's

	Linear CAC's				Non-Linear CAC's			
P	1	2	3	4	1	2	3	4
Cr[11]	.3	.5	.66	1	.42	.69	.83	1
Cr (Curve Fitting)	.3	.48	.69	.98	.41	.7	.86	.98

3. Problem Formulation

Consider a communication channel with a width denoted *cw* (see figure 1). Let w_{min} be the minimum width of the wires, *w* the width of wires and s the spacing between adjacent wires. Note that *w* and *s* are multiples of w_{min}. The rest of the parameters i.e. wire thickness, dielectric height are usually specified by the technology, so they are not design parameters. For this channel, there are several crosstalk avoidance methods that can be employed to reduce its worst case delay or to enhance its reliability, these desired properties come at the expense of the number of data carrying wires. We consider three types of buses, namely:

1. Throughput-Centric Buses

The throughput in this type is the most crucial aspect of the communication link; this is the case for non-interactive or bulk traffic. All design parameters (*p*, *w*, *s*) should in this case be optimised to maximize the throughput.

2. Latency-constrained Buses

A good example where low latency is necessary is at bottlenecks such as a micro-processor to cache connections. It is well known that a high cache latency can dramatically reduce the amount of work that can be usefully done by a processor. In such cases the dimensions of the wires are predefined by delay requirements, which means that only the worst-case coupling factor *p* can be used to optimise the throughput.

3. Reliability-constrained Buses

Crosstalk avoidance methods are required to improve channel robustness against crosstalk glitches caused by transitions on adjacent wires. This means the maximum coupling factor allowed on the bus *p* is predefined by reliability restrictions; consequently the throughput optimisation can only be done on the wire dimensions.

Based on the above mentioned classification of buses, three throughput-centric optimisation problems can be formulated as follows.

- *Problem 1*: For a fixed width channel, find the wire width (*w*), the wire spacing (*s*) and the crosstalk avoidance method (*p*) that achieve the maximum bandwidth.
- *Problem 2*: For a fixed width channel with specified geometry (i.e. *w, s* are given), find the crosstalk avoidance method (*p*) which achieves the maximum bandwidth.
- *Problem 3*: For a fixed width channel with a certain crosstalk avoidance requirement i.e. p is pre-set, find the wire width (w) and spacing (*s*) that maximize the bandwidth.

These problems are addressed for both buffered and un-buffered wires.

4. Throughput-Centric Optimisation for Interconnect

Based on the analysis in the previous sections, the throughput of a fixed width links is a function of three design variables namely; wire width *w*, wire spacing *s* and the worst-case coupling factor *p*. This summarized in the following equation.

$$BW = \frac{cr * n}{1.5 * D} \tag{18}$$

Cr can be substituted from equations (16) and (17) depending on which type of crosstalk avoidance methods is employed. *n* is replaced from (3) and D from equation (12) or (13) depending on buffering conditions.

In the remainder of this section we briefly summarise the analytical methods we employed to solve to the three optimisations problems specified in section 3. We study three cases depending on the type of buffering in the channel; wires with no buffers, buffered wires and finally optimally buffered lines. It should be noted here that we only consider uniform buffer insertion.

Problem 1: find (p, w, s) at which BW reach its global maximum.

The partial derivative of *BW* with respect to *p, w and s* at its maximum points is equal to zero [17]. This property can be used to find the solutions of the first problem which is reduced to solving three equations (19), (20) and (21) with respect to *p, w* and *s*

$$\frac{\partial BW}{\partial s} = 0 \tag{19}$$

$$\frac{\partial BW}{\partial w} = 0 \tag{20}$$

$$\frac{\partial BW}{\partial p} = 0 \tag{21}$$

To avoid these complex calculations, we employed a numerical search algorithm which explores the design space looking for the maximal points. This algorithm uses the bandwidth expression we derived. Tables 3 and 4 summarises some of results obtained from this analysis, note that *w* and *s* are multiple of the minimum width $w_{min.}$

It should be noted here that the figures in Table 3 and 4 were calculated for a link with a width (129*wmin) and 10 wire length. The wire sizes were those of a standard UMC CMOS 90nm technology.

Problem 2: find p at which BW reaches its optimum points for a specified geometry (w, s)
In this case the only variable in the bandwidth expression (18) is the coupling factor *p*; the latter can be tuned by applying deferent crosstalk avoidance methods. Finding a solution to this problem is reduced finding the root of (21).
Closed form expressions of the roots of this equation have been found for the following cases:

1. Un-Buffered buses with Linear CAC's (see (22)), and with non-linear CAC's (24)
2. Buffered buses with linear CAC's (23) and non-linear CAC's (25).

For optimum buffering, no solution exist, but the bandwidth was found to achieve its maximum point at *p=4*.
These results indicate that the coupling factor which maximise the throughput of a physical link depends on the interconnect length, its structures (wire width, spacing, etc) and on the strength (*H*) and number (*K*) of the inserted buffers. Note that *Lambertw* is the inverse function of $f(x) = xe^x$ where e^x is the natural exponential function and x is any complex number [17].
Problem 3 find (w, s) at which BW reaches its maximum or maximum values for a channel with specified crosstalk requirements.
The analytical solution to this problem is found by solving equation (19) and (20). It has been found that there exist a clear optimum of the wire dimensions which maximise the link throughput. This optimum solution depends on the coupling factor and interconnects length. The full analysis for this problem is not going to be mentioned here due to page limitations, however some of
the results are shown in Tables 3 and 4.

5. Simulations

In order to verify our findings, we compared them with results obtained by the simulations in *spectre* for a standard *umc cmos 90nm* technology.
A three wire bus was considered, the wire thickness was set to be two times the minimum wire width (t = *0.41um*) and so was the dielectric height (*h = 0.41um).* 10 mm wires were considered. The output resistance of a minimum driver (Rd) was found to be *9 kΩ* and its input capacitance *3.15 fF*. The width of the wire was varied between w_{min} to $6*w_{min}$ and the wire spacing between w_{min} to $6*w_{min}$.
For all possible combinations of wire width and wire spacing (36 in this case), the delay of the middle line was measured for all four coupling factors. This has been done by applying different testing patterns to obtain the crosstalk cases (2-5) described in Table 1. These experiments were performed for Un-buffered lines; a buffered line with K=5 and H=30 and for an optimally buffered line. The number and size of the repeaters for optimum buffering were obtained from equations (14) and (15).
The delays of the lines obtained form the simulations were used to calculate the throughputs of a channel with a fixed width ($cw = 129*w_{min}$). These figures were employed to determine the following:

1) The wires dimensions (w, s) and the coupling factor *p*, at which the throughput of the considered channel reaches its maximum. This was found to be at (p, w, s) = (4, 5, 3).
2) The coupling factor at which the throughput of a specified geometry is maximised.
3) The wire dimensions at which a link with a pre-determined coupling factor gives a maximum bandwidth.

The results obtained by the simulations were in agreement with the closed form solutions summarised in Tables 3 and 4.

6. Conclusions

Interconnects are rapidly becoming a bottleneck for the performance and cost in high-speed VLSI circuits. This paper has explored the design tradeoffs of area -constrained links. New models of the throughput have been derived which incorporate the interconnect structures (wire width, thickness and spacing), its length and the wiring overheads incurred by crosstalk avoidance methods. These expressions were then used to investigate the best combination of wire sizing solutions and crosstalk avoidance techniques that yield the maximum throughput for given metal resources. For throughput-centric buses with un-buffered wires, the optimisation of wire dimensions was found to be sufficient to achieve the maximum throughput, however; for links with buffered lines crosstalk avoidance codes were found to be useful in increasing the bandwidth. For latency-centric buses, it has been found that there is a clear optimum of the maximum capacitive coupling factor on the channel at which the throughput is maximised; this optimum can be calculated using the closed form expressions we derived. The significance of this result comes from the fact that it indicates that crosstalk avoidance methods may improve the link throughput in addition to its latency, this depends on the interconnect structures and the number of buffers and their sizes. Our derived formulae of the optimum coupling factor can be utilized by the designer as a quick tool to establish whether or not employing CAC's help improve the bandwidth. For reliability-constrained buses our analysis proved that there are configurations of wire sizes at which the link bandwidth reaches its maximum value, the optimum solutions of wire dimensions have been found mathematically and the results were confirmed by the simulations in spectre. Finally for links with optimally buffered wires, our analysis indicated that the minimum wire spacing and width achieve the maximum throughput of the communication link, employing crosstalk avoidance methods seems to have a rather negative effect on bandwidth in this case. The results we have presented in this article can conveniently be used to optimise on-chip buses.

$$p = 2.7886 - \frac{Cg}{Cc} \tag{22}$$

$$p=2.788-\left[\frac{(\frac{0.7RdK}{H})^2(\frac{Cg}{K}+HCd)+R(\frac{0.4Cg}{K}+0.7HCd)}{(\frac{0.7RdCc}{H})+(\frac{0.4RCc}{K})}\right] \tag{23}$$

$$p = exp\ (lambertw\ (1/\ (_{Cc\ /Cg}\ )*exp\ (-41/10000))\ +41/10000) \tag{24}$$

$$p=exp(lambertw(1/Cc/(7RdK+4RH)*(7RdKCg+7RdK^2HCd+4RHCg+7RH^2CdK)*exp(-17/4145))+17/4145) \tag{25}$$

Table 3: Analytical Solutions for Throughput-Centric Optimisations of Fixed width RC Links with Non-Linear CAC's

Buffering Type	***The Global Maximum Points (p, w, s)***	***The Values of the Worst-Case Coupling Factor at the Maximum Point for Specified Wire Dimensions***				***Optimum wire dimensions (w, s)for predefined p***			
		(w, s) = (1,1)	***(w, s) = (2,1)***	***(w, s) = (3,2)***	***(w, s)= (4,2)***	***P=1***	***P=2***	***P=3***	***P=4***
No Buffers	*(4, 5.4, 3.3)*	*1*	*2*	*2*	*2*	*(5.7, 4)*	*(5.6, 3.9)*	*(5.4, 3.4)*	*(5.4, 3.3)*
Constantly Buffered Lines	*(2,1,1)*	*4*	*2*	*3*	*3*	*(1, 1)*	*(1,1.3)*	*(1,1.5)*	*(1,1.6)*
Optimally Buffered Lines	*(4, 1, 1)*	*4*				*(1, 1)*			

Table 4: Analytical Solutions for Throughput-Centric Optimisations of Fixed width RC Links with Linear CAC's

Buffering Type	***The Global Maximum Points (p,w,s)***	***The Values of the Worst-Case Coupling Factor at the Maximum Point for Specified Wire Dimensions***				***Optimum wire dimensions (w, s) for predefined p***			
		(w, s) = (1,1)	***(w, s) = (2,1)***	***(w, s) = (3,2)***	***(w, s)= (4,2)***	***P=1***	***P=2***	***P=3***	***P=4***
No Buffers	*(4, 5.4, 3.3)*	*1*	*1*	*4*	*4*	*(5.7, 4)*	*(5.6, 3.9)*	*(5.4, 3.4)*	*(5.4, 3.3)*
Constantly Buffered Lines	*(4,1,1.6)*	*4*	*4*	*4*	*4*	*(1, 1)*	*(1,1.3)*	*(1,1.5)*	*(1,1.6)*
Optimally Buffered Lines	*(4, 1, 1)*	*4*				*(1, 1)*			

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