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Characteristics of Gated Diode Based DRAM under Low Voltage

Xuefu Zhang, Delong Shang, Fei Xia and Alex Yakovlev

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Contact:

xuefu.zhang@ncl.ac.uk

delong.shang@ncl.ac.uk

fei.xia@ncl.ac.uk

alex.yakovlev@ncl.ac.uk

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School of Electrical, Electronic and Computer Engineering,

Merz Court,

University of Newcastle upon Tyne,

Newcastle upon Tyne, NE1 7RU, UK

http://async.org.uk

Xuefu Zhang, Delong Shang, Fei Xia and Alex Yakovlev

Microelectronics System Design Group, Newcastle University, UK

Abstract

Energy harvesting systems suffer variable power supply from time to time. Ultra low power supply or even a very short period without power supply may cause very serious consequences. In the case of system memories, important data may be lost. A gated diode based DRAM can be a potential memory solution as a dynamic backup storage to meet these challenges. However, before exploring this solution, such DRAMs need to be studied under low and variable Vdd situations and this paper investigates these problems. Gated diodes can be used in DRAM cells and sense amplifiers on the read bit-lines. These give the DRAM significantly long retention time and improve memory reading speed.

This paper investigates the performance of two existing DRAM structures, 2T1D and 3T1D, working under low and variable Vdd. In addition, a novel sense amplifying method which works correctly under very low Vdd is developed. The performances of DRAMs with the novel sense amplifiers, with typical sense amplifiers, and without sense amplifiers are characterized with a comparative study.

Key Words — Gated diode, DRAM, energy harvesting, sense amplifier.

I. Introduction

One of the most significant characteristics of energy harvesting systems is variable power supply. This variance can have large ranges. When power supply recovers, all processed data stored in memories could have been lost and the system has to repeat previous computations. This wastes time, power and reduces efficiency. To overcome this problem, the system may use a backup memory to store important information when there is sufficient power. Dynamic

Random Access Memory (DRAM), with its comparatively long retention time, may be suitable for this purpose in the energy harvesting context.

Since the typical 1T1C DRAM memory cell suffers destructive read, it is not the ideal structure for data error checking and correcting during the backup process. In contrast, the gated diode based DRAM cells with non-destructive read, without requiring frequent refresh, and better performance at very low Vdd have the potential of being used as this kind of backup memory.

Using 3T DRAM for energy harvesting systems was first suggested in [1]. However, the paper was limited to a general concept without further details on the DRAM performance in energy harvesting systems. Novel 2T1D and 3T1D DRAM cells with internal voltage gain were presented in [2]. The performance of the 2T1D DRAM cells was explored at Vdd=1.2V and the comparison between 2T1D and 3T1D was discussed. More specifically, the performance of 3T1D DRAM in terms of retention time, access time, and word-line delay can be found in [3]. It was studied under Vdd=0.8V-1.4V. In [4], it was claimed that although the 3T1D cell has large size than the 2T1D cell, the former has quicker access time and significant lower active power and standby power. Paper [5] illustrates main advantages of 3T1D DRAM comparing with traditional 6T SRAM and also argues that since 3T1D is an asymmetrical structure, it has a higher process variation tolerance than symmetrical structures. In [4] and [5], the working Vdd was assumed to be around 1V.

Up to now, the behavior of 2T1D and 3T1D DRAM with Vdd below 1V has not been investigated. And no evidence shows that 3T1D structure performs absolutely better than 2T1D structure when Vdd is much below 1V. However, very low Vdd is exactly the environment most relevant to energy harvesting applications. This means that for an exploration on using gated diode based DRAM as the backup memory for energy harvesting systems, many questions need be addressed. These include: 1. whether the normal 2T1D and 3T1D cells and existing sense amplifiers work at Vdd much below 1V; 2. whether the 3T1D

structure performs better than the 2T1D structure at low Vdd; 3. whether the use of sense amplifiers in general is a good idea for low power under low Vdd.

A. Contributions and Organization

In this paper, our main contributions include 1. comparing the performance of 2T1D and 3T1D DRAM structures under variable Vdd from 0.19V to 1V, 2. pointing out a drawback of 3T1D working under low Vdd, 3. developing a new sense amplifying technique to improve pre-charging and reading speed, and 4. comparing and analyzing 2T1D DRAM with and without sense amplifiers in terms of system latency and energy consumption.

The remainder of the paper is organized as follows: Section II presents the basics of the gated diode based DRAM structure, the principle of gated diode, and performance comparison between 2T1D and 3T1D. Section III introduces a novel sense amplifying method for energy harvesting systems. Section IV presents the comparison and analysis between the 2T1D DRAM with and without sense amplifiers in terms of pre-charging time, reading time and energy consumption. Finally, summary and conclusion are provided in section V.

II. Gated Diode Based DRAM Structure

A. Basic Structures

Figure 1 (a) shows the structure of 2T1D and 3T1D and Figure 1 (b) shows the structure of an N-type gated diode. In Figure 1 (a), both 2T1D and 3T1D cells have dual bit-lines. BLw is the write bit-line signal and BLr is the read bit-line signal. These two structures are composed of one write access gate (wg), one read access gate (rg) and one gated diode (gd). The 3T1D structure has an extra read select gate (rs). Gates wg and rs are controlled by WLw and WLr respectively. WLw is the write word-line signal and WLr is the read word-line signal. Gated

diode gd can be implemented using a transistor in which only the gate and source of the transistor is used and the drain is not used as shown in the middle of Figure 1 (b) or all three of gate, source and drain are used but the source and drain are connected together to form two diodes in parallel [2] as shown in the right hand side of Figure 1 (b).

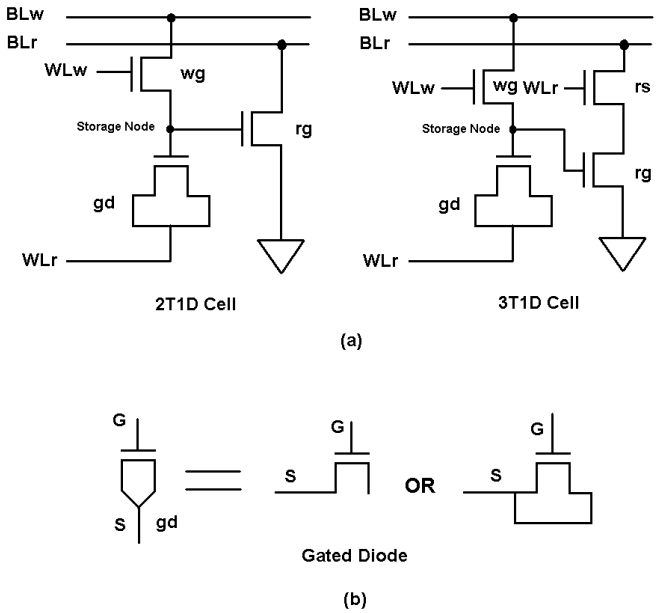


Figure 1. (a) 2T1D and 3T1D structure. (b) Gated diode structure. [2]

The DRAM works as follows (see Figure 2): rg is controlled by the voltage at the storage node. When a "1" is stored at the storage node, once gd is triggered by WLr, the voltage at the storage node can be pumped up even higher than Vdd. At the same time, rg is switched on by the highly pumped-up voltage. Thus, rg connects the read bit-line to ground (GND). Therefore, the pre-charged VBLr (shown in Figure 2) is pulled down to GND and there is a "1" produced at Dout. On the other hand, if a "0" is stored at the storage node, the voltage can only be pumped up slightly, with rg still closed and the read bit-line isolated from GND. Thus, the pre-charged VBLr is maintained at the read bit-line and a "0" is produced at Dout. There is a significant voltage difference at the storage node for reading "1" and "0". Simulation results and discussion of the voltage difference is shown in Section III.

gd is not only adopted as part of a signal amplifier but can also be used as a capacitor to temporarily store data during short periods in which the power supply is ultra low or even totally lost [6]. According to our investigation, for the purpose of reaching long retention time, the size of gd needs to be larger than that of other transistors in the cell to increase the capability for holding more charges. On the other hand, the size of wg and rg should be kept as small as possible to decrease charge leaking from gd. Keeping wg and rs (or rg in 2T1D) small also decreases the capacitances on the write and read bit-lines with potentially improved power and latency.

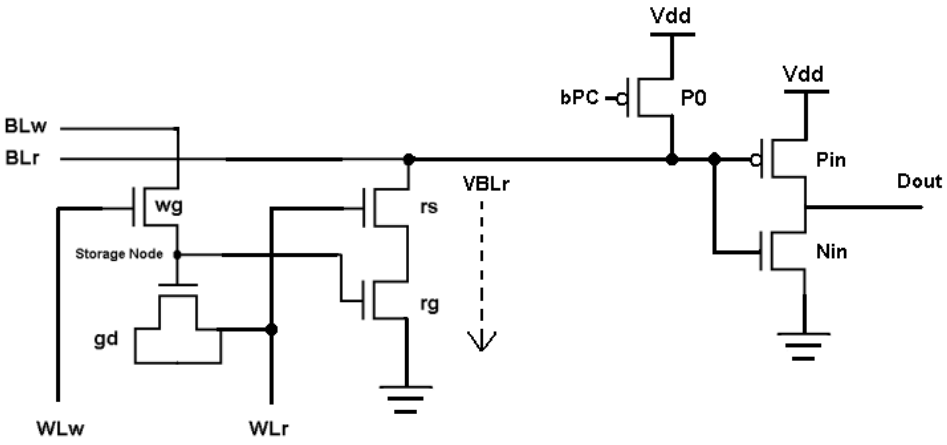


Figure 2 Basic 3T1D DRAM structure (without sense amplifiers)

B. Performance Comparison: 2T1D Vs 3T1D

According to [2] and [4], compared to the 2T1D structure, the 3T1D structure has high gate overdrive in the read path as the source of rg is biased lower. This improves reading procedure. However, this conclusion was drawn without studying ultra-low Vdd behaviors. In Figure 2, when Vdd is below 1V, even V_{gd} (the voltage at the storage node) can be pumped up higher than Vdd, rs and rg may not be switched on normally. And the current pull-down ability is limited by the influence of rs and rg at low Vdd. Because reading "1" needs switching rg and rs on and reading "0" keeps these two gates off, it is harder and takes longer

to read "1" than "0" at low Vdd with the 3T1D structure. And this situation will be worse with Vdd further decreasing.

The 2T1D structure in Figure 1 (a) does not have the rs and there is only the rg on the read path (which connects the read bit-line to GND). As a result, the current pull-down ability of the 2T1D structure at low Vdd may be much stronger than that of 3T1D with its two gates on the read path. Therefore, the gate rs in 3T1D cell may behave as a current pull-down barrier rather than a reading driver when Vdd is low.

To verify this conjecture, the performances of the 2T1D and 3T1D structures are tested under various Vdds from 0.19V to 1V. The test is based on analogue simulations using Spectre in the Cadence Analog Design Environment with the UMC CMOS 90nm technology. (All simulations in this paper employ this same tool set and technology. The detailed simulation parameters studied in this paper are listed in Appendix I Table 1.) Two memory blocks (2T1D and 3T1D) are tested in the simulation. Each memory block contains one DRAM bank (64-word x 16-bit) and two binary-tree-like address decoders [7] for write word-lines and read word-lines access control (the delay of the address decoder is listed in Appendix I Table 2). The basic 3T1D DRAM structure without sense amplifiers shown in Figure 2 is adopted in the simulation. 2T1D DRAM is similar to that. For writing "1", V_{gd} in both 2T1D and 3T1D cells is charged to 0.07V as "1". When V_{gd} drops to 0.06V after the retention period, reading is preformed and "1" is read out. In this study, with a large gated diode (6um/2.6um), the retention time is approximately 3.5us.

Through the simulations, it is obvious that the pull-down ability of 2T1D for reading "1" is significantly stronger than that of 3T1D at Vdd varying from 0.19V to 1V. Figure 3 shows an example of the simulation when reading "1" is performed in 2T1D and 3T1D memory blocks at Vdd=0.3V (the width of rs and rg is 0.12um). (a) and (b) show the V_{gd} waveforms. Since large size gated diode is adopted in the memories to gain long retention time, the drive ability of read address decoder is limited at low Vdd. Thus, there are obvious rising and falling delay shown in (a) and (b). Once the V_{gd} is pumped up, the rg in both 2T1D and 3T1D

cell is switched on and the read path should connect the read bit-line to GND. For the 2T1D structure, when V_{gd} rises beyond 0.2V, the read path pulls the pre-charged VBLr down to GND immediately, shown in (c). However, for the 3T1D structure, only slight pull-down ability is shown in (d) during V_{gd} being pumped up.

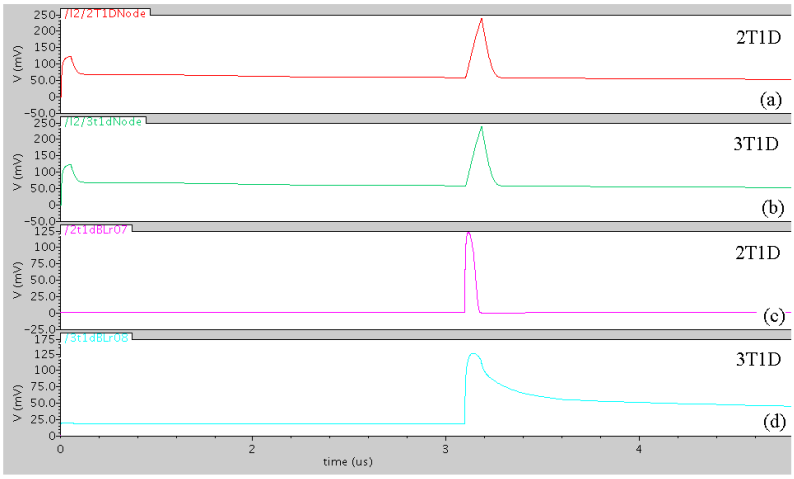


Figure 3 Pull-down ability of 2T1D and 3T1D structure when reading "1" is performed at Vdd in 0.3V (the width of rs and rg is 0.12um).

In order to further explore the difference of pull-down ability between the 2T1D and 3T1D structures, reading "1" is preformed at different Vdds varying from 0.19V to 1V. Since the simulations preformed on these two memory blocks employ the same timing, the reading for each memory block begins simultaneously. And the reading period is set to end when the 2T1D cell completely pulls the pre-charged VBLr down to GND. At the end of the reading period, the VBLr in 3T1D memory block is recorded and shown in Figure 4. In the simulation, rg and rs in the 3T1D structure adopt different widths (0.12um, 0.24um, 0.48um and 0.72um) and no choice of the width can force the 3T1D cell to pull the pre-charged VBLr to GND successfully with the same reading period as the 2T1D cell did.

In this regard, 3T1D structure is not the best choice for the DRAM memory working at low Vdd. Since the 2T1D structure performs better than the 3T1D structure at Vdd below 1V, the 2T1D structure is chosen to be further investigated in the rest of the paper.

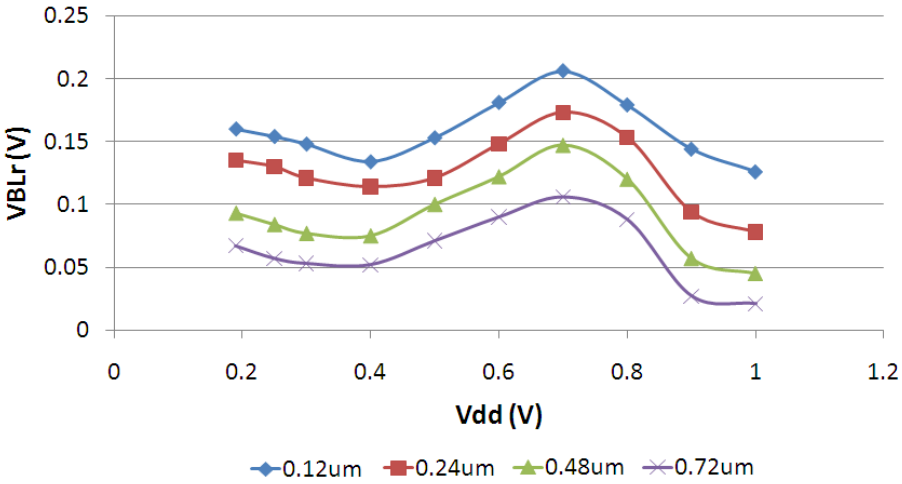


Figure. 4. VBLr in the read bit-line of 3T1D memory block recorded after the end of reading period in which 2T1D cell completely pulls the pre-charged VBLr down to GND.

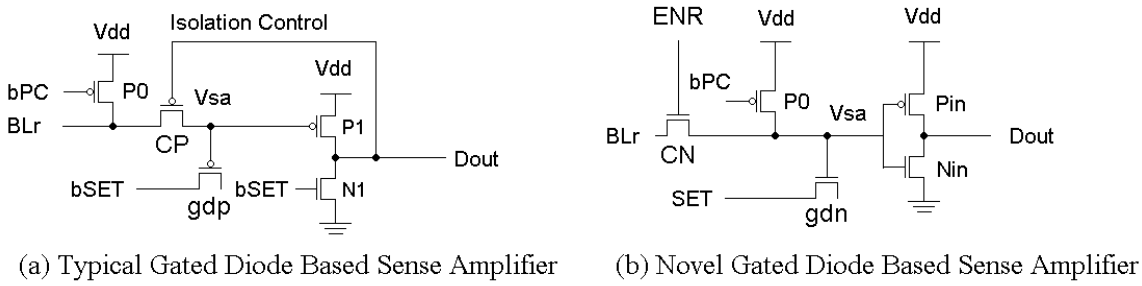
III. Gated Diode Based Sense Amplifiers

A. Typical Sense Amplifier

In general, bit-line sense amplifiers improve reading speed. In 2T1D or 3T1D DRAM, Gated Diode Based Sense Amplifiers (GDSAs) are normally adopted. A dynamic version of GDSA was introduced in [8], shown in Figure 5 (a). This typical GDSA is employed to cooperate with 3T1D DRAM bank working at Vdd in 1.2V. In the structure, gated diode (gdp) and control gate (CP) are based on P-type transistors. The typical GDSA employs a dynamic output feedback to control the isolation device (CP). Thus, the sense amplifier block can be isolated from the influence of the read bit-line automatically during reading "1".

Before reading, bSET is maintained high during idle period. Thus, N_1 is kept on and connects D_{out} to GND. In this case, the isolated sense amplifier is opened by asserting "0" to CP. This connects the sense amplifier to the read bit-line. When pre-charging is performed, V_{sa} (shown in Figure 5) is amplified immediately by gdp (gdp has the ability to maintain V_{sa} when bSET is changed to low). Thus, P_1 is switched off by V_{sa}. During the reading period,

bSET is in low and N_1 is also switched off. Although D_{out} is isolated from GND, it still can be kept low by the effect of the work load behind the output of the memory block (in the simulation, a two-inverter based keeper is adopted in place of the work load to maintain the present status and also provide feedback to control the sense amplifier). When reading "1" is performed, V_{sa} (temporally stored at gdp) is pulled down to GND by the pull-down read path connected to GND. Thus, P_1 is switched on again. Since bSET is low and N_1 is shut, D_{out} is charged to high and "1" is read out. At the same time, CP is switched off by the feedback control signal "1". This isolates the sense amplifier from the read bit-line. For reading "0", since there is no pull-down read path connected to GND, V_{sa} is high and D_{out} is maintained at low. Therefore, "0" is read out.



(a) Typical Gated Diode Based Sense Amplifier (b) Novel Gated Diode Based Sense Amplifier

Figure 5 Gated Diode Based Sense Amplifiers

However, when Vdd is low and with a heavy work load connected to D_{out}, the drive ability of the feedback control is significantly decreased. In this case, the feedback control will have a very low reaction speed or even cannot work reliably. In addition, the typical GDSA structure suffers an apparent drawback. Since gdp and N_1 are controlled by bSET, there is always high voltage asserted to gdp and N_1 during the idle period. In this case, N_1 is always switched on. If V_{sa} is low, P_{in} is also switched on. Therefore, a current will exist from Vdd to GND and this causes a large amount of energy to be consumed during the idle period.

Besides, employing P-type gated diode also causes worse performances at very low Vdd (below 0.4V in our case). Compared to the N-type transistor, the P-type transistor has a lower electron mobility characteristic which gives P-type gated diode longer retention time and less

leakage current at normal Vdd. However, at very low Vdd, it is very difficult to pre-charge the P-type gated diode high enough to maintain data until the reading process is completed. Therefore, at very low Vdd, when reading "0" is performed, the gdp cannot hold V_{sa} high enough to keep P_1 shut in reading. The simulation result is discussed in Section IV

B. Novel Sense Amplifying Method for Energy Harvesting Systems

In order to deal with the problems discussed above, we propose a new pre-charge method with a different sense amplifier structure shown in Figure 5 (b). It works faster under low Vdd and even can works correctly at Vdd in 0.19V. CN can be considered as a switch between the bit-line and the sense amplifier. The signal ENR which controls CN is from the read address decoder. ENR is the signal that enables the read address decoder to select one of the word-lines in the memory bank to implement reading. During pre-charging, CN is switched off. The gated diode (gdn) is isolated from the read bit-line. Since C1 is pre-charged directly, it quickly stores enough charge for sense amplifying. During reading, CN is switched on so that the bit-line and the sense amplifier are connected together. And the read bit-line will share an amount of charge from the gated diode.

The dynamic voltage variation is different between reading "0" and reading "1". For reading "0", since the charge sharing influence from the read bit-line provides weaker pull-down ability, the voltage falling speed at the gate of gdn is slower. On the other hand, for reading "1", the voltage of read bit-line is pulled down quickly by connecting the pull-down read path to GND. Intuitively, the voltage pull down ability in reading "1" is much stronger than that in reading "0" Therefore, the voltage falling speed at the gate of gdn is significantly faster when the system implements reading "1". Once the amplified V_{sa} is higher than the threshold voltage of the inverter in (b), "0" is produced at D_{out}. Otherwise, "1" is shown at D_{out}.

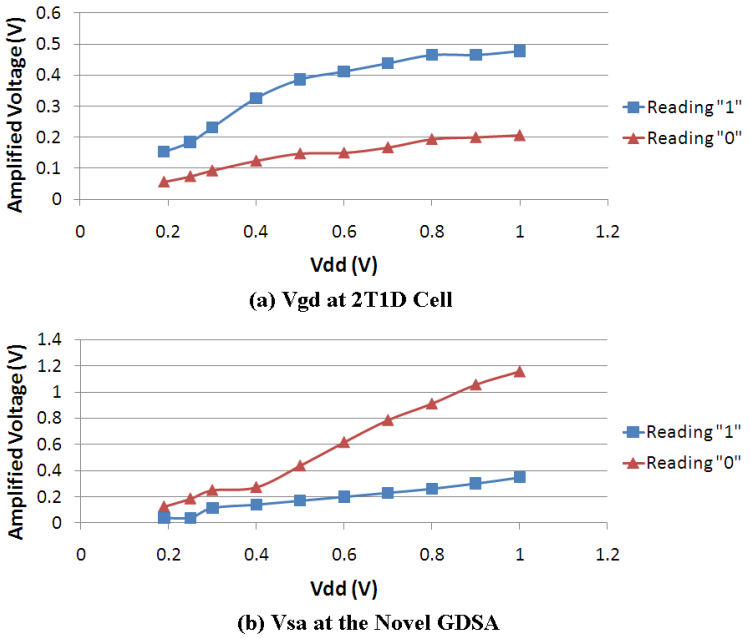


Figure 6. Amplified Vgd (at 2T1D cell) and Vsa (at the Novel GDSA) in terms of reading "1" and reading "0".

By employing the gated diode based 2T1D structure in the DRAM bank and the novel GDSAs, the proposed 2T1D DRAM can work correctly at Vdd varying from 0.19V to 1V. Figure 6 shows the performance of the gated diode employed in 2T1D cells and the novel GDSAs. There are obvious voltage gaps in (a) and (b) between reading "1" and reading "0". Another benefit of employing the 2T1D DRAM and the novel GDSAs at low Vdd is time and energy saving. Normally, once V_{gd} or V_{sa} is triggered to high, the voltage level should be higher than the triggering voltage level (suppose the triggering voltage level is the same as Vdd). Actually, it is obvious that, in (a), the amplified voltage for reading "1" is not higher than the triggering voltage. Since amplifiers are used, the read bit-line does not require being fully pre-charged. Therefore, V_{gd} in the 2T1D does not have to be fully pumped up to Vdd. For reading "1", during the period in which the pumped-up V_{gd} rises to high, the channel of rg is gradually opened. And at a certain voltage level while V_{gd} is rising, the VBLr has been already pulled down to GND. Therefore, the reading process can be considered finished and there is no need to continue pumping V_{gd} up until rg is fully opened. Besides, to drive 16 big size gated diodes fully opened, it will consume a large amount of energy.

IV. Performance Comparison in Terms of the 2T1D DRAM with and without Sense Amplifiers

A. Pre-charging and Reading Time

To further investigate the performances of the 2T1D DRAM with and without sense amplifiers, comparisons in terms of pre-charging and reading time and energy consumption are studied. Simulations show that only the 2T1D DRAM with the novel GDSAs can work correctly at Vdd below 0.4V. With the typical GDSAs or without sense amplifier, the DRAM cannot work at Vdd below 0.4V.

In Table 3 (in Appendix I), the novel GDSA has the shortest pre-charging and reading time. The typical GDSA performs slightly slower than the novel GDSA in terms of pre-charging and reading time. It is obvious that the memory without amplifiers has longest pre-charging and reading time. Although the DRAM with the novel GDSAs has significantly slow performances at Vdd in 0.19V (with pre-charging time 100ns and reading time 550ns), it presents good tolerance ability under variable Vdd. And this extreme situation can be considered as the worst case. Therefore, the 2T1D DRAM with the novel GDSAs has better performance in robustness.

When Vdd is above 0.3V, the novel GDSA employs small size gated diode (1um/0.4um). When Vdd drops to 0.3V, larger size gated diode (1.3um/0.7um) is adopted. At Vdd in 0.25V, only the gated diode with the size in 2um/0.9um enables the novel GDSA to work correctly. In the extremely low Vdd (0.19V), the gated diode in 4um/1.7um has to be adopted. Through the simulation, at the same Vdd and in the same pre-charging time, the larger size gated diodes can store more charges than the smaller ones. At very low Vdd, since the drive capability from the read address decoder is limited and there is very long address decoding delay, only the large gated diode has the ability to maintain the data being valid after reading is completed.

As discussed above in Section III A, P-type gated diodes employed by the typical GDSA decreases the performance at very low Vdd. Since P-type gated diode has obviously lower electron mobility than N-type one, it is hard to charge it high enough at very low Vdd. Longer charging time means longer time required for reading "1". Also, it is very difficult to keep V_{sa} high to maintain "0" at D_{out} until the reading is completed. Therefore, the typical GDSA cannot work at Vdd below 0.4V by simply increasing the size of P-type gated diode. In the simulations, five different size P-type gated diodes were tested and none of them can work under 0.4V (2um/0.9um, 3um/1.3u, 4um/1.7u, 5um/2.2um, 6um/2.6um).

For the 64x16 2T1D DRAM without sense amplifiers, the total capacitance on the read bit-line is limited and it is too weak to maintain information at very low Vdd until reading is completed. Therefore, it is very difficult to work when Vdd is below 0.4V, without adding large volume N-caps on each read bit-line or increase the quantity of word-lines in the memory.

B. Total Energy Consumption

In Figure 7, the total energy consumptions in terms of the 2T1D DRAM with and without sense amplifiers are shown. The energy consumption contains the energy consumed in pre-charging, reading and the period in which data are valid at output for 20ns. For the DRAM with the novel GDSAs, the lowest energy point is at 0.25V with the gated diode size in 2um/0.9um. In the figure, there are two cross points labeled as A and B. Point A is approximately at Vdd=0.5V and Point B is close to Vdd=0.93V. For the DRAM without sense amplifiers, below Vdd=0.5V, it consumes slightly more energy than the DRAM with the novel GDSAs. At Vdd=0.5V, the DRAM without sense amplifiers and the one with novel GDSAs have the same energy consumption. When Vdd is above 0.5V, the DRAM without sense amplifiers consumes significantly less energy than the one with the novel GDSAs. When Vdd is below 0.93V, the DRAM with typical GDSAs consumes more energy than the others. However, the energy consumption of the DRAM with the novel GDSAs has a

dramatic increasing trend when Vdd is above 0.6V. Finally the energy consumed by the DRAM with the novel GDSAs goes beyond the energy consumed by the DRAM with the typical GDSAs when Vdd is 0.93V. From the energy consumption figure, the novel GDSA is ideal for the DRAM working at Vdd varying from 0.3V to 0.6V for less energy consumption. And the typical GDSA may be better for the DRAM working at Vdd higher than 0.93V. If efficiency is less important, the DRAM without sense amplifier also can be employed for working at Vdd higher than 0.4V.

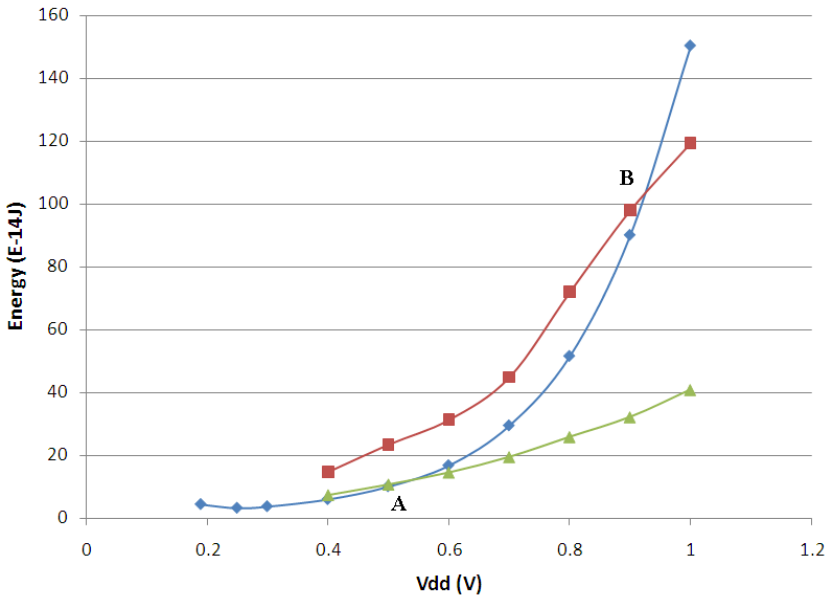


Figure. 7. Total energy consumption of pre-charging and reading in terms of 2T1D DRAM with sense amplifiers and without sense amplifiers. Amplifier A: Novel Gated Diode Based Sense Amplifier. Amplifier B: Typical Gated Diode Based Sense Amplifier.

V. Conclusion

Our investigation demonstrates that by employing the 2T1D structure and adopting a new sense amplifying technique, the 2T1D DRAM can work under Vdd varying from 0.19V to 1V with high efficiency. And it also has ideal performance in energy consumption when the memory works at Vdd varying from 0.3V to 0.6V. Working correctly at very low Vdd

enables the 2T1D DRAM with novel GDSAs to obtain better system robustness and tolerate extreme variations in the power supply. Since the memory working voltage range is most relevant to energy harvesting systems, this clears the way for the 2T1D DRAM of this type to be considered as backup memory to store important data for energy harvesting systems.

In this paper, the investigation was focused on the performance of the gated diode based DRAM of different structures and using different sense amplifying choices. In order to properly demonstrate the validity of using such DRAM as backup memory, holistic design and analyses need to be carried out together with backup memory controllers, refreshing control circuits and peripheral timing circuits.

Our future work also needs to consider the influences of the variation of environment, such as temperature variation. Since the sub-threshold leakage current through the transistors strongly depends on the temperature variation, the leakage of a memory cell may be highly related to temperature variation. To cope with the temperature variation, it is necessary to develop a simple and low power leakage sensor to measure the leakage current and compensate the backup DRAM memory employed for energy harvesting applications. In order to implement temperature variation compensation, new analysis for the characteristics of leakage current influenced by the temperature variation should be also considered in the future.

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Appendix I

TABLE 1
PARAMETERS OF THE SIMULATIONS IN THIS PAPER

2T1D Cell		3T1D Cell	
wg	0.12um/0.08um	wg	0.12um/0.08um
rg	0.12um/0.08um	rg	x/0.08um (1)
gd	6u/2.6u	rs	x/0.08um
		gd	6um/2.6um
Inverter			
		Pre-charge Device	
P_{in}	0.24um/0.08um		
N_{in}	0.12um/0.08um	P_0	0.24um/0.08um
Gated Diode		Control Device	
gdn	α/β (2)	CP	0.24um/0.08um
gdp	1um/0.4um	CN	0.12um/0.08um
		Memory Size	64-word x 16 bit (1K)
Address Decoder			
P_{AD}	0.24um/0.08um	T	27°C
N_{AD}	0.12um/0.08um		

(1) In Section II, the width of rg and rs in 3T1D cell is variable. x=0.12um, 0.24um, 0.48um, 0.72um.

(2) In Section IV, at Vdd varying from 0.4V to 1V, α=1um, β=0.4um. At Vdd=0.3V, α=1.3um, β=0.7um. At Vdd=0.25V, α=2um, β=0.9um. At Vdd=0.19V, α=4um, β=0.17um

TABLE 2
ADDRESS DECODER DELAY

Vdd (V)	0.19	0.25	0.3	0.4	0.5	0.6	0.7
Delay (ns)	60	15	6.5	1.8	0.8	0.5	0.35
Vdd (V)	0.8	0.9	1				
Delay (ns)	0.3	0.25	0.23				

In the simulation, the delay begins when the enable signal (EN) is asserted to the address decoder and the delay ends when the voltage of the address signal reaches Vdd.

TABLE 3
PRE-CHARGING TIME AND READING TIME

Pre-charging Time					
Vdd (V)	**0.19**	**0.25**	**0.3**	**0.4**	**0.5**
With Amplifier A (ns)	100	20	6	2	0.7
With Amplifier B (ns)	N/A	N/A	N/A	2.2	0.77
Without Amplifier (ns)	N/A	N/A	N/A	4.5	1.9
Vdd (V)	**0.6**	**0.7**	**0.8**	**0.9**	**1**
With Amplifier A (ns)	0.35	0.21	0.13	0.1	0.08
With Amplifier B (ns)	0.39	0.23	0.14	0.11	0.09
Without Amplifier (ns)	0.71	0.44	0.27	0.22	0.17
Reading Time					
Vdd (V)	**0.19**	**0.25**	**0.3**	**0.4**	**0.5**
With Amplifier A (ns)	550	150	70	24	12
With Amplifier B (ns)	N/A	N/A	N/A	29.5	14.7
Without Amplifier (ns)	N/A	N/A	N/A	37.2	16.5
Vdd (V)	**0.6**	**0.7**	**0.8**	**0.9**	**1**
With Amplifier A (ns)	7	5	4	3	2.5
With Amplifier B (ns)	8.6	6.15	4.95	3.7	3.1
Without Amplifier (ns)	10.3	8.13	7.66	6.33	4.38

Amplifier A: Novel Gated Diode Sense Amplifier
Amplifier B: Typical Gated Diode Sense Amplifier

Appendix II

(Writing, Reading and Refreshing Time and Power Consumption)

A. 3T1D DRAM Specifications in Simulation.

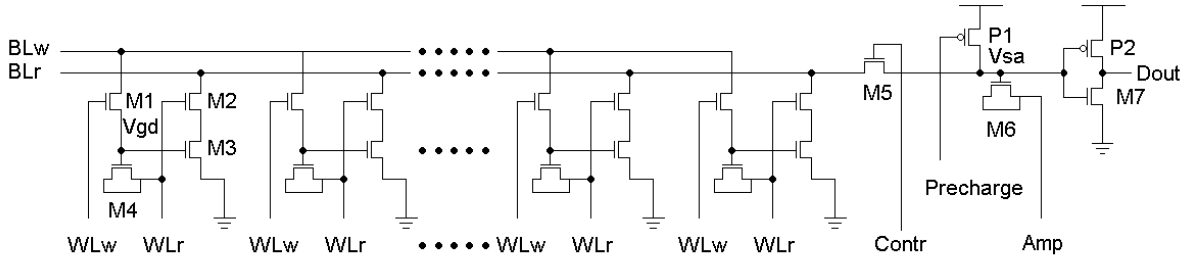

Figure 1. 3T1D DRAM with Sense Amplifiers. M1, M2 and M3 are access control gate. M3 is a high Vt type transistor. M4 is an N-type gated diode.

Table 1. 3T1D cell and memory size.

3T1D cell	
M1 N_10_SP	0.15um/0.08um
M2 N_10_SP	0.35um/0.08um
M3 N_10_SPHVT	0.35um/0.08um
M4 N_10_SP	7um/3um
Inverter	
Pin P_10_SP	0.3um/0.08um
Nin N_10_SP	0.15um/0.08um

Amplifier	
C0 N_10_SP	0.5um/0.08um
C1 N_10_SP	1.5um/1.3um
Precharge Device	
P0 P_10_SPHVT	1.5um/0.08um
Memory	64-word x 16-bit (1K)

B. Writing Time and Power Consumption (for processing 1 wordline × 16 bits)

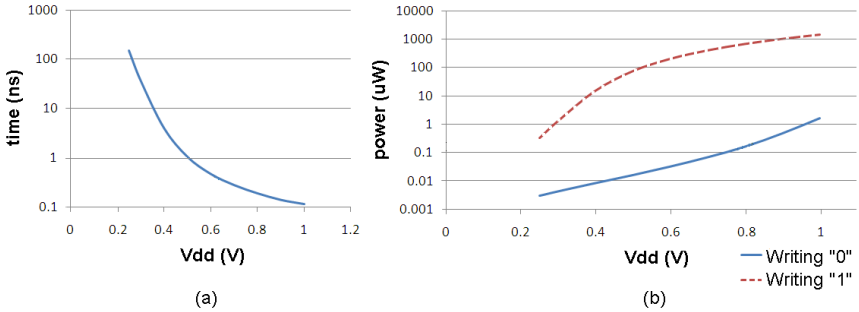

Figure 2. Writing time (a) and average power for writing (b)

C. Pre-charge Time and Read Time (for processing 1 wordline × 16 bits)

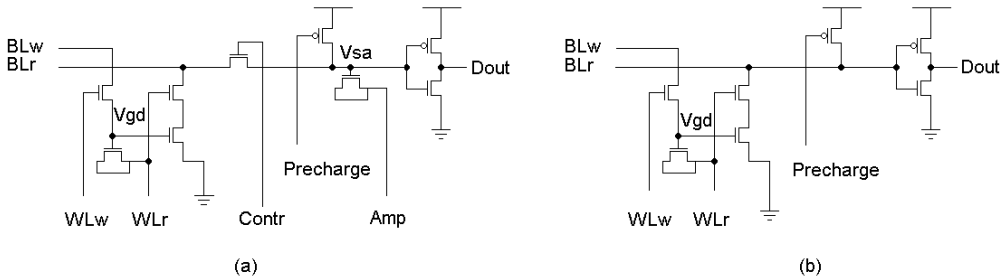

Figure 3. Circuit schematics for 3T1D DRAM using the sense amplifier (a) and without using the sense amplifier (b).

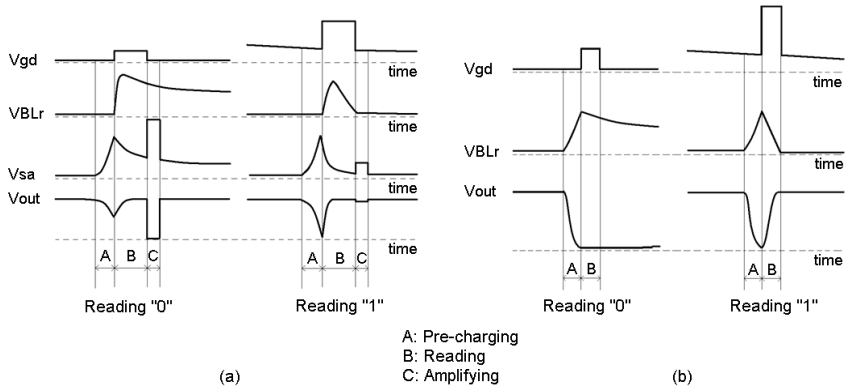

Figure 4. Voltage waveforms for 3T1D DRAM using the sense amplifier (a) and without using the sense amplifier (b).

Table 2. Comparison in terms of pre-charging time and reading time.

Pre-charge Time									
Vdd (V)	0.25	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1
With Amplifiers x_1 (ns)	35	11	2	0.7	0.35	0.21	0.13	0.1	0.08
Without Amplifiers x_2 (ns)	110	27	3.3	1	0.52	0.34	0.25	0.2	0.17
Difference Factor α	0.68	0.59	0.39	0.3	0.33	0.38	0.48	0.5	0.53
Read Time									
Vdd(V)	0.25	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1
With Amplifiers x_1 (ns)	100	42	10	4	2.3	1.6	1	0.9	0.8
Without Amplifiers x_2 (ns)	170	70	15.5	5.5	3.4	2.6	2.2	1.9	1.4
Difference Factor α	0.41	0.4	0.35	0.27	0.32	0.38	0.55	0.53	0.43

Table 3. Average power comparison for reading "1" and reading "0".

Reading "1"									
Vdd (V)	0.25	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1
With Amplifiers x_1 (uW)	0.08	0.25	1.56	6.7	15.7	19.4	14.7	19.5	35.6
Without Amplifiers x_2 (uW)	0.13	0.41	2.68	11.4	27.3	47.8	85.6	130	205
Difference Factor α	0.38	0.39	0.42	0.41	0.42	0.59	0.83	0.85	0.83
Reading "0"									
Vdd(V)	0.25	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1
With Amplifiers x_1 (uW)	0.08	0.24	1.47	6.21	14.5	18.4	14.6	20	36.9
Without Amplifiers x_2 (uW)	0.09	0.27	1.9	8.1	18.4	31.1	55.6	81.3	118
Difference Factor α	0.11	0.11	0.23	0.23	0.21	0.41	0.74	0.75	0.69

D. Whole Refresh (64x16 bits) Time and Power Consumption

Table 4.. Time and Power Consumption for Whole Refresh

Vdd (V)	0.25	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1
Energy (nJ)	0.22	0.24	0.32	0.44	0.61	0.78	1.04	1.33	1.60
Time (ns)	27584	8704	1568	515	312	248	185	163	129
Power (mW)	0.008	0.027	0.201	0.852	1.94	3.12	5.64	8.18	12.4

Appendix III

(3T1D 64×16 Bits DRAM Memory Layout Area)

A. 3T1D DRAM Layout Area

Table 1. Layout Area of 3T1D 64x16 Bits DRAM with Sense Amplifiers.

GatedDiode M4 W/L (um)	3/3	4/3	5/3	6/3	7/3	8/3
GatedDiodeArea (um²)	13.63	17.58	21.53	25.48	29.43	33.38
3T1D CellArea (um²)	16	19.45	23.9	27.85	31.8	35.75
64x16MemoryArea (mm²)	0.017	0.021	0.025	0.029	0.033	0.037
GatedDiode M4 W/L (um)	9/3	10/3	11/3	12/3	13/3	
GatedDiodeArea (um²)	37.33	41.28	45.23	49.78	53.13	
3T1D CellArea (um²)	39.7	43.65	47.6	51.55	55.5	
64x16MemoryArea (mm²)	0.041	0.045	0.049	0.053	0.057	

LayoutArea M1 (150n/80n) (um²): 0.68; LayoutArea M2 (350n/80n) (um²): 0.85;
LayoutArea M3 HTV (350n/80n) (um²): 0.84; LayoutArea SenseAmplifier (um²): 10.07;

B. Retention Time vs Layout Area

In the simulation, the retention time starts when the storage node of 3T1D cell is charged to 600mv and ends when the voltage at the storage node drops to 60mv.

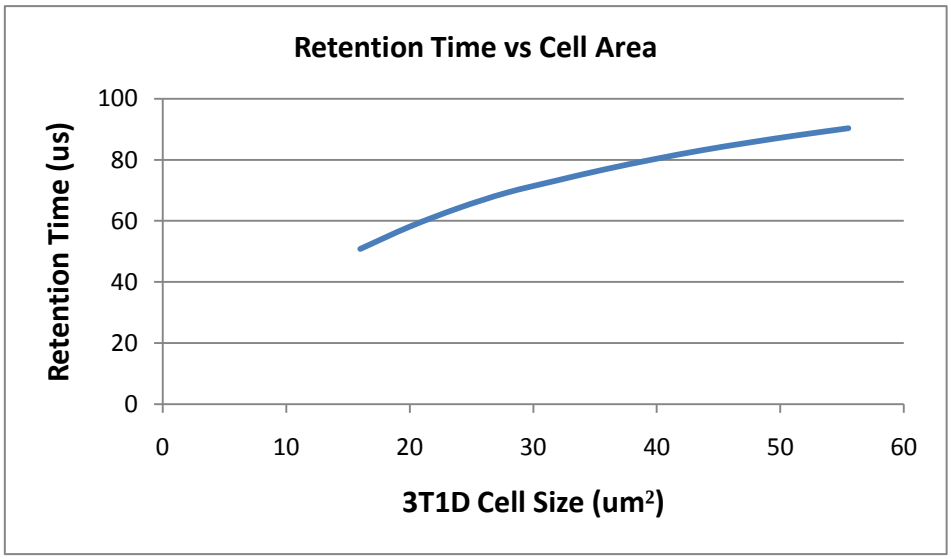

Figure 1. Retention Time vs 3T1D Cell Layout Area

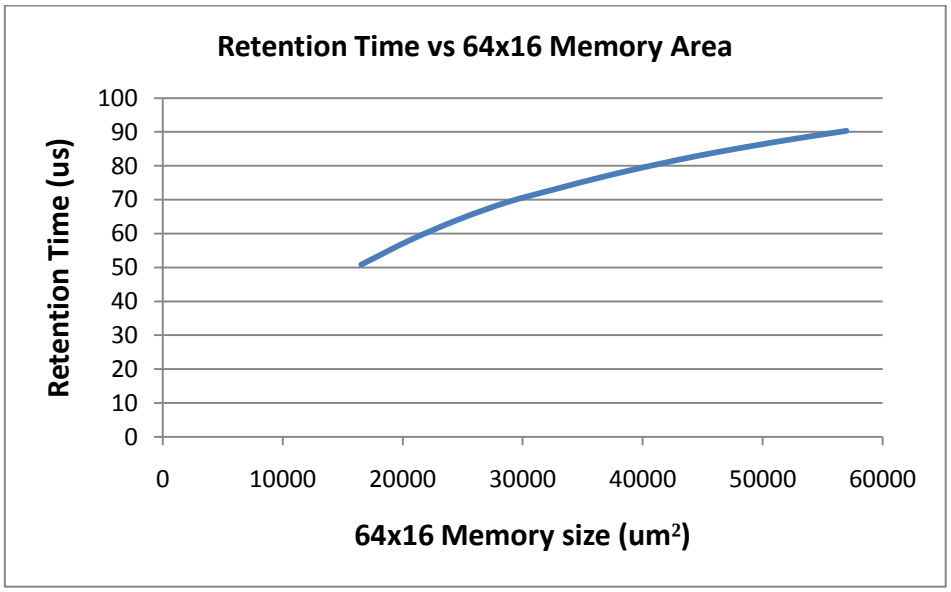

Figure 2. Retention Time vs Layout Area of 3T1D 64x16 Bits DRAM with Sense Amplifiers

Appendix IV
(Gated Diode Based DRAM for Ultracapacitor Switching Operation Deployed in Energy Harvesting Systems)

A. Memory Backup System for Power Switching Operation

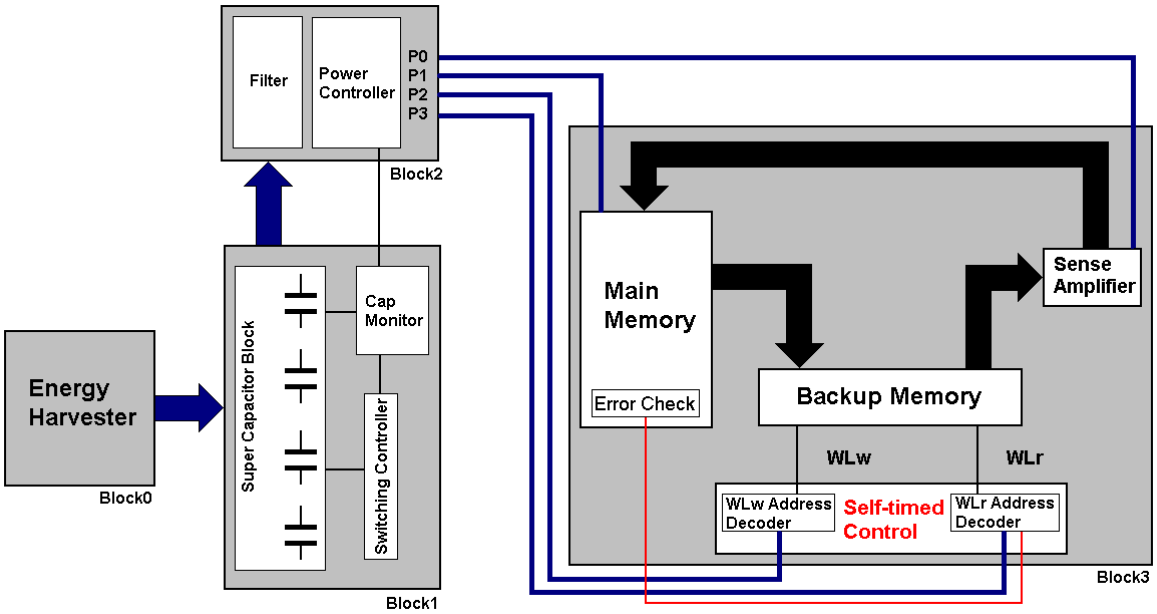

Figure 1. Memory Backup System. Complete Memory backup process without DRAM refresh. Ultracapacitor Switching conditions:1. Current ultracapacitor nearly runs out of energy. 2. System needs high performance.

B. Retention Time Required by the cells on each wordline

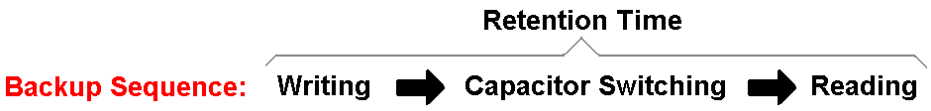

Figure 2. Backup Sequence

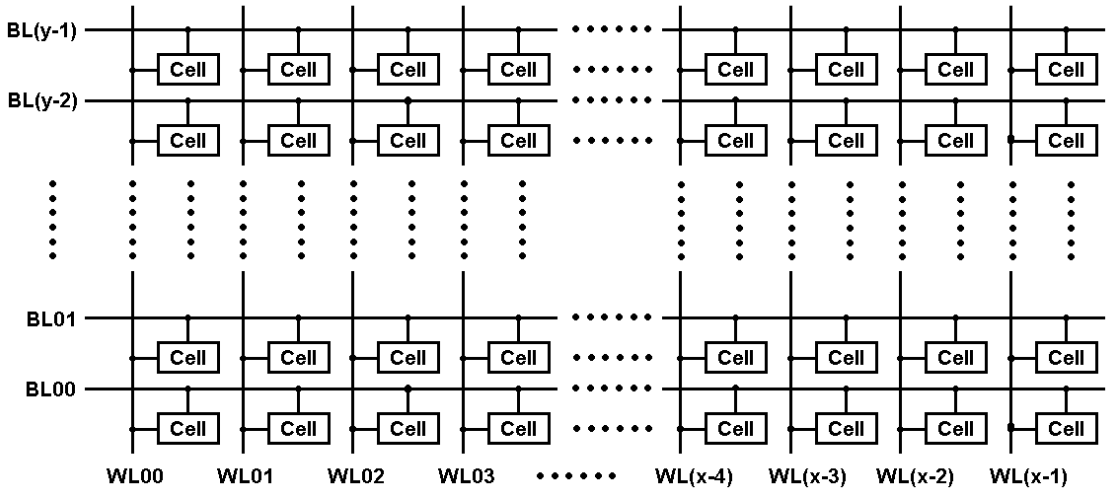

Figure 3. Memory Array

WLα: $T_{RET} \geq (x-1-\alpha)T_W + T_{SW} + \alpha T_R$ (1-1)

WL00: $T_{RET00} \geq (x-1)T_W + T_{SW}$ (Worst Case) (1-2)

WL(x − 1): $T_{RET(x-1)} \geq T_{SW} + (x-1)T_R$ (1-3)

Tw: Writing time for every single word-line.

T_R: Reading time for every single word-line.

T_{sw}: Ultracapacitor Switching Time.

C. Time Left for Ultracapacitor Switching Operation (Based on the Worst Case)

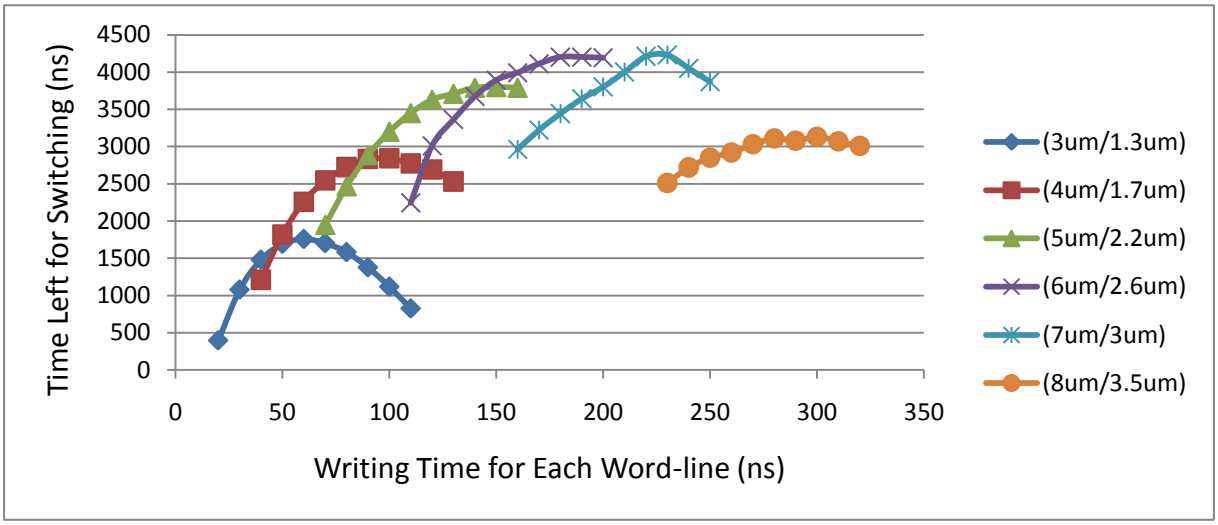

Figure 4. Time Left for Ultracapacitor Switching Vs Writing Time for Each Word-line (Vdd 300mV)

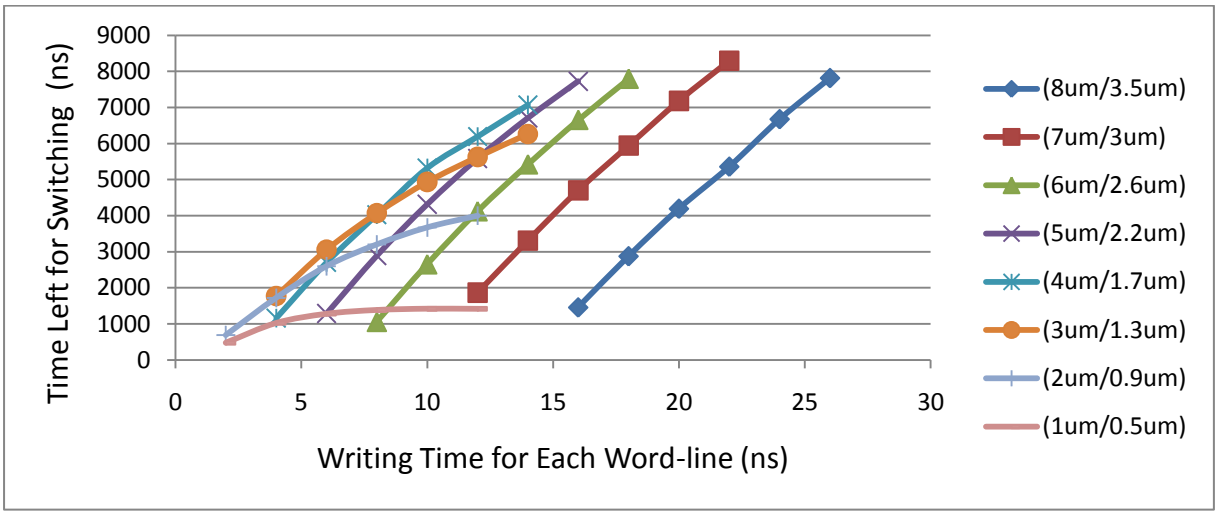

Figure 5. Time Left for Ultracapacitor Switching Vs Writing Time for Each Word-line (Vdd 400mV)

D. Simulation Data (Time Left for Ultracapacitor Switching Operation)

Table 1. Simulation Data (Deploying different size of gated diode under variable Vdd). T_{EN}: Writing Time; T_{RET}: Retention Time; T_{SW}: Time Left for Ultracapacitor Switching.

Width/Length	8um/3.5um						Vdd	400mV
T_{EN}(ns)	16	18	20	22	24	26		
T_{RET}(us)	2.55	4.09	5.54	6.83	8.27	9.54		
T_{SW}(us)	1.46	2.88	4.19	5.36	6.67	7.81		
Width/Length	7um/3um						Vdd	400mV
T_{EN}(ns)	12	14	16	18	20	22	24	
T_{RET}(us)	2.70	4.27	5.79	7.16	8.53	9.77	10.96	
T_{SW}(us)	1.46	2.88	4.19	5.36	6.67	7.81	9.36	
Width/Length	6um/2.6um						Vdd	400mV
T_{EN}(ns)	8	10	12	14	16	20	22	24
T_{RET}(us)	1.63	3.36	4.94	6.38	7.74	9.01	10.23	11.36
T_{SW}(us)	1.06	2.65	4.12	5.42	6.65	7.79	8.89	9.89
Width/Length	5um/2.2um						Vdd	400mV
T_{EN}(ns)	4	6	8	10	12	14	16	18
T_{RET}(us)	1.48	3.15	4.60	6.02	7.04	8.03	9.03	9.83
T_{SW}(us)	1.16	2.70	4.03	5.32	6.19	7.07	7.94	8.61
Width/Length	4um/1.7um						Vdd	400mV
T_{EN}(ns)	4	6	8	10	12	14	16	18
T_{RET}(us)	1.48	3.15	4.60	6.02	7.04	8.03	9.03	9.83
T_{SW}(us)	1.16	2.70	4.03	5.32	6.19	7.07	7.94	8.61
Width/Length	3um/1.3um						Vdd	400mV
T_{EN}(ns)	4	6	8	10	12	14	16	
T_{RET}(us)	2.09	3.50	4.65	5.64	6.46	7.23	7.87	
T_{SW}(us)	1.77	3.06	4.07	4.94	5.63	6.27	6.78	
Width/Length	2um/0.9um						Vdd	400mV
T_{EN}(ns)	2	4	6	8	10	12	14	
T_{RET}(us)	0.88	2.04	3.05	3.78	4.38	4.83	5.17	
T_{SW}(us)	0.69	1.72	2.60	3.20	3.67	4.00	4.21	
Width/Length	1um/0.5um						Vdd	400mV

T_{EN}(ns)	2	4	6	8	10	12				
T_{RET}(us)	0.67	1.34	1.73	1.96	2.12	2.25				
T_{SW}(us)	0.47	1.02	1.28	1.38	1.42	1.42				
Width/Length		8um/3.5um							Vdd	300mV
T_{EN}(ns)	230	240	250	260	270	280	290	300	310	320
T_{RET}(us)	17.41	18.26	19.03	19.74	20.49	21.21	21.82	20.49	21.21	21.82
T_{SW}(us)	2.51	2.72	2.85	2.92	3.03	3.11	3.08	**3.13**	3.07	3.01
Width/Length		7um/3um							Vdd	300mV
T_{EN}(ns)	160	170	180	190	200	210	220	230	240	250
T_{RET}(us)	13.33	14.23	15.09	15.93	16.73	17.47	18.82	19.08	19.54	20.00
T_{SW}(us)	2.96	3.22	3.44	3.64	3.80	4.00	4.21	**4.23**	4.05	3.87
Width/Length		6um/2.6um							Vdd	300mV
T_{EN}(ns)	110	120	130	140	150	160	170	180	190	200
T_{RET}(us)	9.41	10.82	11.81	12.76	13.62	14.36	15.12	15.85	16.49	17.12
T_{SW}(us)	2.25	3.01	3.36	3.67	3.89	4.00	4.11	**4.20**	4.20	4.19
Width/Length		5um/2.2um							Vdd	300mV
T_{EN}(ns)	70	80	90	100	110	120	130	140	150	160
T_{RET}(us)	4.61	5.25	5.88	6.53	7.17	7.81	8.45	9.09	9.73	10.37
T_{SW}(us)	1.95	2.47	2.89	3.20	3.45	3.63	3.71	3.79	**3.80**	3.79
Width/Length		4um/1.7um							Vdd	300mV
T_{EN}(ns)	40	50	60	70	80	90	100	110	140	150
T_{RET}(us)	3.90	5.15	6.23	7.15	7.97	8.72	9.37	9.94	10.50	10.98
T_{SW}(us)	1.21	1.82	2.26	2.55	2.73	2.83	**2.84**	2.78	2.69	2.53
Width/Length		3um/1.3um							Vdd	300mV
T_{EN}(ns)	20	30	40	50	60	70	80	90	100	110
T_{RET}(us)	1.80	3.13	4.17	5.02	5.73	6.31	6.83	7.27	7.65	7.99
T_{SW}(us)	0.40	1.08	1.48	1.70	**1.76**	1.71	1.58	1.38	1.12	0.83
Width/Length		2um/0.9um							Vdd	300mV
T_{EN}(ns)	10	20	30	40	50	60	70	80	90	100
T_{RET}(us)	0.71	1.95	2.77	3.33	3.76	4.10	4.37	4.60	4.83	4.95
T_{SW}(us)	-0.06	0.54	0.72	0.64	0.43	0.13	-0.24	-0.65	-1.06	-1.58
Width/Length		1um/0.5um							Vdd	300mV
T_{EN}(ns)	10	20	30	40	50	60				

T_{RET}(us)	0.69	1.21	1.46	1.62	1.74	1.85				
T_{SW}(us)	-0.08	-0.20	-0.57	-1.07	-1.59	-2.12				
Width/Length		6um/2.6um							Vdd	250mV
T_{EN}(ns)	150	160	170	180	190	200	210	220	230	240
T_{RET}(us)	2.76	3.28	3.80	4.23	4.73	5.18	5.62	6.03	6.44	6.83
T_{SW}(us)	-6.97	-7.09	-7.21	-7.42	-7.56	-7.75	-7.95	-8.17	-8.41	-8.67
Width/Length		5um/2.2um							Vdd	250mV
T_{EN}(ns)	150	160	170	180	190	200	210	220	230	240
T_{RET}(us)	3.34	3.85	4.28	4.76	5.15	5.63	6.00	6.45	6.80	7.18
T_{SW}(us)	-6.39	-6.52	-6.73	-6.89	-7.13	-7.30	-7.56	-7.76	-8.04	-8.31
Width/Length		4um/1.7um							Vdd	250mV
T_{EN}(ns)	150	160	170	180	190	200	210	220	230	240
T_{RET}(us)	4.92	5.13	5.50	5.81	6.15	6.45	6.78	7.00	7.31	7.51
T_{SW}(us)	-4.81	-5.34	-5.51	-5.83	-6.14	-6.47	-6.79	-7.21	-7.54	-7.98