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Wide-Range, Reference-Free, On-Chip Voltage Sensor for Variable Vdd Operations

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***Abstract*—In future systems with relatively unreliable and unpredictable energy sources such as harvesters, the system Vdd may become unstable. For power efficient operation, Vdd is an important parameter in any meaningful system control mechanism. Reliable and accurate on-chip voltage sensors are therefore indispensible for the power and computation management of such systems. Existing voltage sensing methods are not suitable because they usually require a stable and known reference (voltage, current, time, frequency, etc.), which is difficult to obtain in this environment. This paper describes a reference-free voltage sensor implemented using a speed independent SRAM cell and an inverter chain. It can work under a wide range of Vdd, from 200mV to 1V in 90nm CMOS technology, and provides accurate measurements of Vdd over this operating range with a precision of 10mV. Unlike existing methods, the voltage information is directly generated as a digital code without any analog circuits. This is realized by exploiting the inherently different latency behaviors of different types of circuits under different Vdd.**

1 INTRODUCTION

Microelectronic system design is becoming more energy conscious, because of limited energy supply (scavenged energy or low battery) and excessive heat with associated thermal stress and device wear-out [12]. At the same time, the high density of devices per die and the ability to operate with a high degree of parallelism, coupled with environmental variations, create almost permanent instability in voltage supply (cf. Vdd droop), making systems highly power variant. In the not so long past *low power design* was targeted merely at the reduction of capacitance, Vdd and switching activity, whilst maintaining the required system performance. In many current applications, the design objectives are changing to maximizing the performance within the dynamic power constraints from energy supply and consumption regimes. Such systems can no longer be simply regarded as low power systems, but rather as power-adaptive or power-resilient systems. It is also possible now to imagine designs where systems are optimized to work under both dynamic power, especially scavenged power, and performance constraints [13].

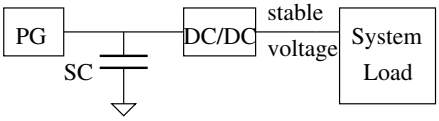

FIGURE 1 GENERAL MECHANISM OF ENERGY HARVESTOR.

Energy harvesting systems have emerged as a prominent research area and continue to grow at a rapid pace. Figure 1 shows a general energy harvesting system, in which there are a power generator (PG), a super capacitor (SC) acting as a substantial energy store, and a DC/DC converter. The generator obtains energy which is stored in the super capacitor. After a certain amount of energy has been accumulated, the DC/DC converter produces a stable voltage for the digital computation system (load). Most digital systems nowadays need stable voltage (Vdd) as the source of energy [14].

This mechanism has a number of disadvantages: 1) the super capacitor, if it is to store a reasonable amount of energy, needs a lot of time to charge; 2) current DC/DC blocks usually have lower bound requirements for their input voltage, say 2.0V, which is substantially higher than the normal working Vdd of current digital computation circuits – in other words, such an input voltage could already comfortably power digital computation directly, if the digital load can tolerate voltage variations to a high degree; 3) the mechanism as a whole has a significant power overhead.

System power efficiency can be greatly improved if the requirement for a DC/DC block is removed or if the system supports working modes in which the DC/DC block is bypassed. This in turn means that the digital load needs to be able to draw power directly from energy storages such as super capacitors, and tolerate Vdd variations to a high degree. Some type of control mechanism is needed to schedule computation to fit the current power status. For example, a low power voltage sensor was introduced in [1] to monitor the voltage at the super capacitor. The load is scheduled into operation only when the voltage is over a pre-set threshold.

1.1 Techniques for working under variable power

The focus here is thus power efficiency and not just low power when working under non-deterministic and low Vdd variable over time (probably within a known and wide range).

Asynchronous circuits [10] can work under this kind of variable Vdd [2]. Using such circuits in the load, it is possible to improve the energy efficiency of energy harvesting systems by freeing the system from having to have a single big super capacitor and a DC/DC block.

For example, instead of a single big super capacitor which will take a long time to charge, resulting in very coarse power management time intervals, the power supply mechanism illustrated in Figure 2 can be adopted. In this a certain number of small super capacitors with different capacitances are charged one by one (with each taking a relatively short time to charge) by the power generator based on load (computation task) requirements, and then the capacitors are used as power supplies directly. By dividing the energy storage and computation load (B1, B2, …, Bn) into a number of discrete blocks this method provides for the switching in/out of these blocks to fit computation into power profiles at a finer grain. More sophisticated power switching is also possible.

To improve power efficiency, a good power management mechanism is required to control such charge/discharge and switching in/out procedures. Difficulties faced by such a control mechanism include the necessity to manage blocks and capacitors in real time to cope with problems such as capacitor leakage and energy and task matching under non-deterministic power and task environments.

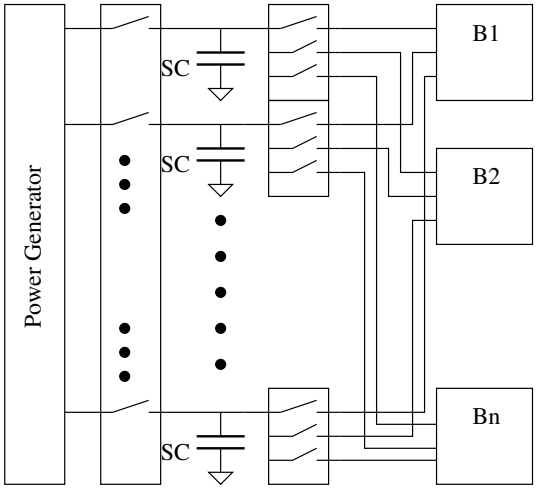

FIGURE 2 THE PROPOSED MECHANISM.

High-quality power management generally requires high quality power monitoring. Generally, such monitoring is best implemented with voltage sensors. For example, with real-time voltage information on all the SC's and task information supplied by all the Bi loads, a good feedback power control can be easily implemented for the system in Figure 2. However, existing voltage sensing techniques are not suitable for the energy harvesting environment (See Section 2).

1.2 Contributions of this paper

The main contributions of this paper include the proposal of a wide-range reference-free on-chip voltage sensor, the sensing method which is an important novelty of the paper, hardware implementation methods and solutions, and related discussions.

The remainder of the paper is organized as follows: Section 2 investigates existing voltage sensors, explaining their main disadvantages in the energy harvesting environment; Section 3 describes the proposed reference-free voltage sensor and presents hardware implementations and discussions; Section 4 shows the simulation results of several possible solutions; Section 5 concludes the paper and discusses potential future developments.

2 EXISTING VOLTAGE SENSORS

Voltage sensors, sometimes also called voltage detectors, are sensors used to detect the presence of electricity in a wire. In a simple voltage sensor, a reference voltage is pre-set, when the input voltage is over that reference voltage, the output is high, otherwise it is low [7].

Off-chip voltage sensors are well known. There exist a large number of commercial voltage detectors in market, such as Microchip's TC54 [8]. One of the most popular voltage sensor based applications is to build a voltage detector into a small screwdriver, which confirms the presence of voltage of the right level in a wire by lighting up an LED.

On-chip solutions have also been proposed [1,3,4,5]. Two different voltage sensor architectures were proposed in [3,4]. One is based on a differential stage, and is called Model Selector (MS) [3]. The other is based on the charging time of a capacitor, and is called Power On Reset (POR) [4]. A low power solution based on modified MS and POR voltage sensors was then described in [1].

Paper [5] introduced a process-invariant voltage sensor architecture with flexible threshold voltage controllability. This solution consists of a band gap reference, a comparator, a resistor divider and a CMOS output driver.

These voltage sensors detect a single fixed and usually pre-set value of voltage.

In the case of power-efficient energy harvesting systems without or with bypassed DC/DC blocks, the working range of Vdd needs to be wide for the digital load. As a result, a sensor detecting a wide range of voltage in real time with good precision is required by any intelligent energy management. Apart from sensing whether the stored voltage in a super capacitor has surpassed a set value or has reduced below another set value, a much larger number of voltage values needs to be monitored in real time.

A set of multiple voltage detectors with different pre-set voltage references can be used to realize a wide range voltage sensor. An ADC mechanism, commonly known as flash ADC, can also be used under the same principle (Figure 3).

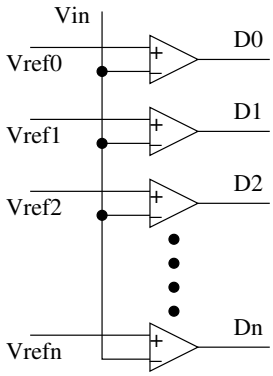

FIGURE 3 BLOCK DIAGRAM OF FLASH ADC.

This solution uses a number of comparators and reference voltages. Vin is compared with these reference voltages separately, and then the output is generated in digital codes.

Both of these methods are awkward and highly costly for high-precision sensing, requiring multiple analog reference values of high accuracy. In addition, in the energy harvesting environment, the system Vdd may become non-deterministic. Assuming that the entire system relies on such a variable power supply, it will be next to impossible to generate stable reference voltages within the system.

The only realistic Vdd-independent method of generating a stable and reliable voltage reference is by using transistor thresholds or different energy states (band gap). One drawback of this approach is that detectors based on this cannot be directly extended to high-precision sensing because fine-tuning thresholds of multiple transistors on a single chip is unrealistic. Another problem with this approach is that the digital load of energy harvesting systems may be controlled to track the minimum energy per operation region [6], which is very close to or below the normal threshold of the logic, making a voltage sensor based on the threshold useless. It is also possible to make use of other reference values such as current, time or frequency. However, out of these only

frequency (and by extension, time) can be reliably generated independently from Vdd by using additional oscillators. Off-chip oscillators tend to consume a high amount of energy to run, and on-chip Vdd-independent oscillators (e.g. based on MEMS) usually require significant modifications to the standard CMOS design flow and certainly cannot be implemented with standard system design techniques. In other words, requiring stable and reliable references of any kind presents severe difficulties to high-precision and wide-range on-chip voltage sensing. Solutions based on the ADC mechanism have additional major problems as they need a constant Vdd and may suffer metastability [11], which will consume more energy.

Furthermore, all these existing sensors depend on analog circuits, which do not work normally when Vdd is reduced to the subthreshold region [6].

3 Reference-free voltage sensing

In principle, there may not be an absolute need for a stable and known external hard reference if an internal relative reference can be generated. For instance, if two circuits behave differently over a Vdd range and this difference also changes with Vdd, the Vdd value can be inferred by observing this difference. This is illustrated in Figure 4 where the difference between the behaviors of Circuit 2 and Circuit 1 can be used to determine the Vdd.

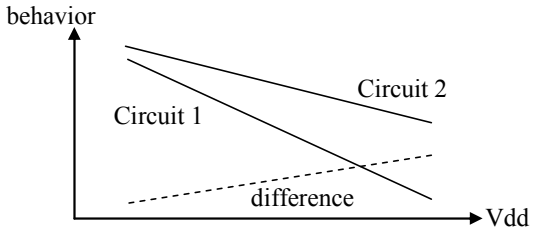

Figure 4 Two circuits behaving differently over Vdd range.

The main aim of this paper is to find a method for the design of reference-free voltage sensors. These sensors should operate under a wide range of Vdd variation and produce accurate Vdd measurements at run time to a high precision.

Specifically, such voltage sensors should work in a Vdd range of between 0.2V and 1V for 90nm CMOS technology, in order to match the requirements of highly efficient energy harvesting systems.

In addition, these sensors should avoid the use of analog circuits or non-standard CMOS elements (e.g. MEMS) in order to reliably function below the normal threshold, reduce power consumption and design and implementation difficulty.

3.1 Method fundamentals

In previous research, we noticed that when Vdd changes, the latencies of different types of circuits change at different rates [2], and this difference in latency change is significant between memory and "regular" logic cells such as inverters.

Figure 5 shows the difference. The experiment attempts to bundle an SRAM cell with an inverter chain, both operating under the same variable Vdd. A *start* signal triggers reading/writing operations of the SRAM cell. This *start* signal is also connected to the inverter chain as its input signal. We measure the number of inverters the *start* signal has passed through when the reading/writing operation finishes. In reading, under the lowest Vdd (0.2V) the SRAM is about 3 times slower than under normal Vdd (1V) in terms of the number of inverters. In writing, under the lowest Vdd the memory is about twice slower than under the normal Vdd in terms of the number of inverters. In other words, inverter chain type delays do not directly track memory operation delays when both are under the same variable Vdd so should not be used as delay bundling devices for memory.

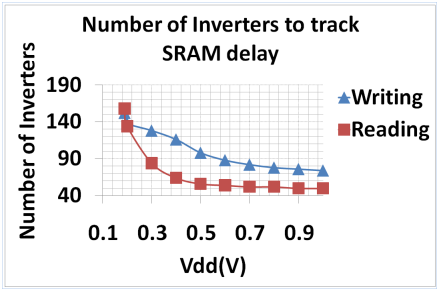

Figure 5 Latency difference of different kind of circuits.

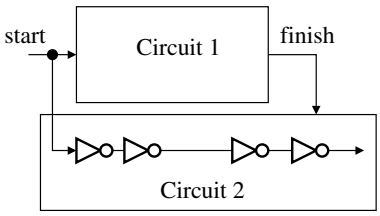

Figure 6 The reference free sensor mechanism.

This difference, however, makes it possible to design voltage sensors without references in the following way.

1) Use two different types of circuits, which have significant latency change difference under different Vdd (e.g. an SRAM cell and an inverter chain), power them from the same Vdd which is the voltage being sensed;

2) Execute a set of events on the slower circuit (e.g. SRAM reading/writing) and provide a "finish" signal when the event set completes;

3) Start the faster circuit at the same time as 2), measure the number of events in the faster circuit (e.g. the number of inverter flips) when the finish signal from 2) appears;

4) This number of events measured in 3) is a direct indication of the Vdd being measured.

The basic system structure is illustrated in Figure 6. The start signal triggers both Circuit 1 and Circuit 2. Normally, Circuit 1 is heavy and slow compare to Circuit 2. When Circuit 1 completes the pre-determined events, the finish signal is generated. At the moment when the finish signal is generated, the numbers of inverters in Circuit 2 which the *start* signal has passed through encodes the tested voltage directly.

The key to this method is that Circuit 1 needs to provide a finish signal without any timing assumptions, i.e. the finish signal should be based on true completion detection. This is because Circuit 1 *must* be of a type which departs from the latency behavior of normal logic under variable Vdd [2].

3.2 Hardware implementation

Asynchronous speed independent (SI) circuits [10] usually function without timing assumptions and generate finish signals from true completion detection. The availability of a true SI SRAM cell from [2] provides a sound basis here.

In this section, an SI 6T SRAM cell [2] is chosen as Circuit 1 and an inverter chain as Circuit 2.

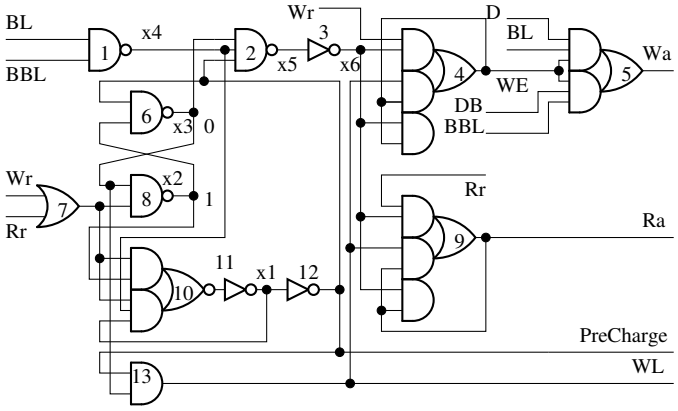

FIGURE 7 SI CONTROLLER FOR 6T SRAM CELL.

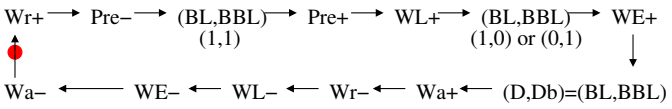

FIGURE 8 SI CONTROLLER IN STG.

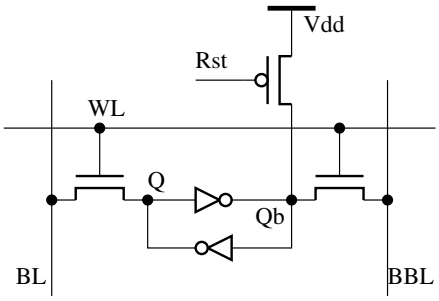

FIGURE 9 MODIFIED 6T SRAM CELL.

We slightly modify the standard 6T SRAM cell and add initialization logic for the SRAM cell as shown in Figure 9. Initially, the cell is reset to logic 0. When detecting voltage, the cell is triggered by writing logic 1 and 0 alternatingly. The key part of the SI SRAM is the SI controller which guarantees correct operation without timing assumption. This controller, shown in Figure 7, covers both writing and reading. As this sensor implementation only uses the writing operation, the controller can be simplified by removing gate 9. The STG [9] specification of the writing operation is shown in Figure 8.

The writing works as follows: when Wr is issued, the signal passes through gates 10, 11, 12 to generate the PreCharge signal. This signal opens the precharge mechanism to charge the two bit lines (BL and BBL). Only when these two bit lines are fully charged to high, x4 will become low and after PreCharge toggles the SR-latch (gates 6 and 8), PreCharge is reset to high. Then WL becomes high to open the pass transistors (see Figure 9) to read the data stored in the cell. After reading, one of the bit lines will be discharged. That makes x4 high and then the WE signal high to open the writing driver and write a new data item into the cell. Only after the new data has been written ((D,Db)=(BL,BBL)), the writing operation will finish. The Wa signal is then generated to indicate this finish.

As the SI SRAM cell uses dual-rail logic, theoretically there is no latency difference between writing 0 and 1. A set of consecutive complete alternating writings of 0 or 1 can be taken as a Circuit 1 event set. This event set is triggered by the Wr signal for the first write, and its completion is indicated by the finish signal (Wa) of the last write.

In practice, there may not be a need to write the SRAM cell too many times to form a Circuit 1 event set. More writing rounds will help increase measurement precision at the expense of power and latency costs. One or two rounds may produce enough measurement precision for most applications. In many cases even partial rounds may suffice, allowing the use of some internal signal to indicate "*start*" (e.g. the signal going up) and "*finish*" (the signal coming down).

We investigate such a low-power, low-latency solution using the internal signal WL as the indicator and measure the numbers of inverter flips (Circuit 2 events) at the WL+ signal (end of the Circuit 1 event set). The original function of the WL signal is to open the pass transistors in the 6T SRAM cell (Figure 9).

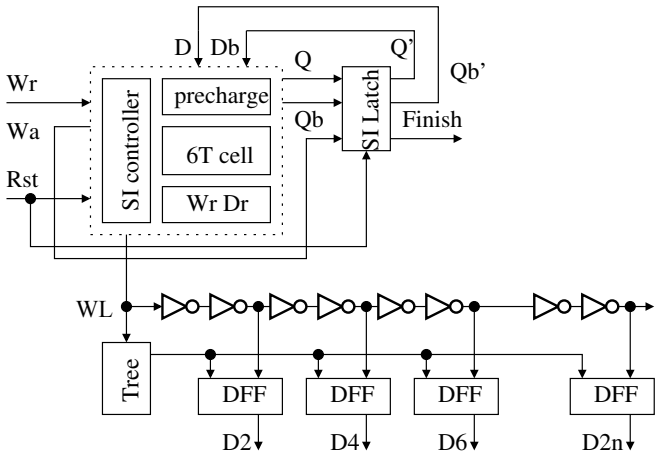

FIGURE 10 BLOCK DIAGRAM OF THE PROPOSED SENSOR.

The block diagram of the implemented sensor is shown in Figure 10, in which an SI controller, a modified 6T SRAM cell, a precharge and writing driver, and an SI latch are used as Circuit 1; a tree structure for balancing the WL signal, an inverter chain, and D Flip-Flops are used as Circuit 2. Both Circuit 1 and Circuit 2 are powered by the monitored voltage.

Initially, the SRAM cell, SI latch and D Flip-Flop (DFF) registers are reset to 0. When the voltage needs to be sensed, the Wr signal is issued. After that the data (inversed Q, we connect Qb' to D and Q' to Db) is written into the cell. Then the new data stored in the cell is written into the SI latch for the next voltage sensing round. This guarantees that alternating logic "1" and logic "0" are written. Meanwhile the WL signal, generated in the middle of the writing, goes to the inverter chain and the tree logic as well to balance the signal in order that all inverter data can be latched at the same time to

form digital codes (D2n, …,D6,D4,D2) when WL goes down (WL-). A Dj bit will be "1" if the WL+ signal passed through its corresponding inverter before WL-, and "0" otherwise. The voltage is encoded in the number of "1" bits along the Dj sequence. Metastability may happen when latching inverter data into DFF registers at WL-. However this can only happen at a single DFF register (corresponding to the last "1" or first "0") with no effect on logical correctness and precision.

This thermometer code can be directly read out to represent the voltage value. After that only the WL signal goes through all inverters to reset for the next voltage measuring round.

An SI counter can be used for Circuit 2 in order to produce a more compact code. We also tried other circuits as Circuit 1. Comparisons will be made in the next section.

4 Simulation Results and Discussions

The sensor was implemented in UMC 90nm CMOS technology using Cadence toolkits.

The Spectre analog simulator of the Cadence toolkit was used to verify the functionality of the sensor. The verification experiment consisted of issuing the Wr signal and then counting the numbers of "1" bits latched in the DFF registers when the simulation is completed at the appearance of the signal Finish, repeated under $0.2V \le Vdd \le 1$.

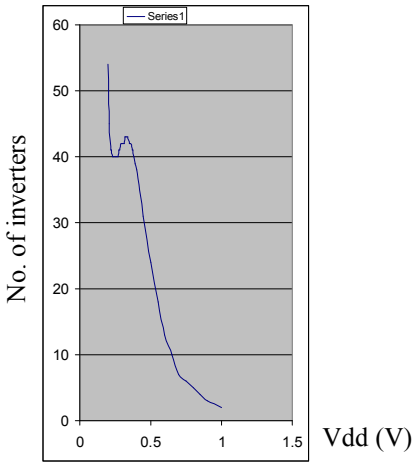

Figure 11 Vdd vs. inverter count.

The results are shown in Figure 11. For example, when Vdd is 1V there are 2 "1" bits, and when Vdd is 600mV there are 13 "1" bits. The curve changes monotonically from 1V to 0.32V and the numbers of "1" bits can directly represent the Vdd values in this range. However, the abnormality from 0.32V to 0.25V means that direct encoding does not exist in this range.

Reducing Vdd increases latency. As our sensing method is based on the latency difference between two different circuits, the relationship between the latencies of these two circuits is of paramount importance and requires investigation.

The inverter count in Figure 11 increases in the range of 1V to 0.32V because Circuit 1 slows down at a faster rate than Circuit 2 when Vdd is reduced. The abnormality below 0.32V is the result of Circuit 2 suddenly "catching up" and slowing down at a comparatively faster rate. The inverter count is influenced by the difference between the *factors of change* of the two circuits. This change factor is defined in (1).

$$f_{v2,v1} = latency(v2)/latency(v1) \quad (1)$$

Here $latency(v)$ is the latency at Vdd=v. The latency change factor in the range between $v2$ and $v1$ is the ratio between the circuit latency at Vdd=$v2$ and the circuit latency at Vdd=$v1$.

An investigation on latency change factors was carried out by measuring the latency of the WL signal and 50 inverters under different Vdds. The step was 10mV. So $\Delta v = v1 - v2 = 10mV$. The experiment results confirm that the latency change factors of both Circuit 1 (SRAM) and Circuit 2 (inverter chain) increase with reducing Vdd. The relationship is illustrated in (2).

$$\begin{aligned} &f(Circuit\ 1) > f(Circuit\ 2); Vdd \in [1V, 0.32V) \\ &f(Circuit\ 1) < f(Circuit\ 2); Vdd \in [0.32V, 0.25V) \\ &f(Circuit\ 1) > f(Circuit\ 2); Vdd \in [0.25V, 0.2V] \end{aligned} \quad (2)$$

A monotonous relationship between f(Circuit 1) and f(Circuit 2) is needed for a good sensor setup. We found that this is possible by using low threshold transistors in the inverter chain which eliminates the anomaly. Figure 12 shows the new measurement results. The curve is monotonous in the entire working range from 1V to 0.2V.

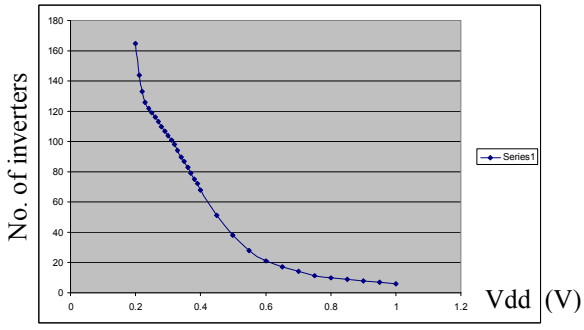

Figure 12 Measurement results for modified threshold inverters.

Table 1 shows some measurement results. For example, 1V corresponds to 6 inverters and at 1V, each measurement round takes 1.85ns in time to complete and costs 1.44pJ in energy. As Vdd is reduced, the number of inverters and measurement time increase but energy consumption reduces first then increases, reflecting the energy per operation curve to some degree [6]. Energy consumption stays low over the entire range.

Table 1 Measure result.

Vdd (V)	Inverters	Measurement Time (ns)	Energy(pJ)
1	6	1.85	1.44
0.8	10	2.63	0.89
0.4	68	28.00	0.32
0.3	104	112.20	0.27
0.25	119	270.30	0.15
0.2	165	872.00	0.43

The measuring resolution (Δv corresponding to a single inverter) is 50mV above 0.7V, and 10mV or better below. The relatively long measurement latency under very low Vdd is not necessarily a problem in operation as the digital load will also slow down significantly making slow control tolerable.

Other types of circuits such as an SI counter and a ring oscillator were also tried as Circuit 1. These should normally behave similarly to the chain of inverters in Circuit 2 but with low threshold transistors in Circuit 2 and normal ones in Circuit 1 some variations were observed. The results based on a

50 inverter ring oscillator as Circuit 1 is shown in Figure 13.

The precision of this sensor solution is much worse than the first sensor based on SRAM. For example, in the range from 1V to 0.7V, the resolution is 100mV and in the important range between 0.4V and 0.7V the resolution may not be enough for fine-grain energy management. However, this sensor is small in size and has a relatively fast measurement speed.

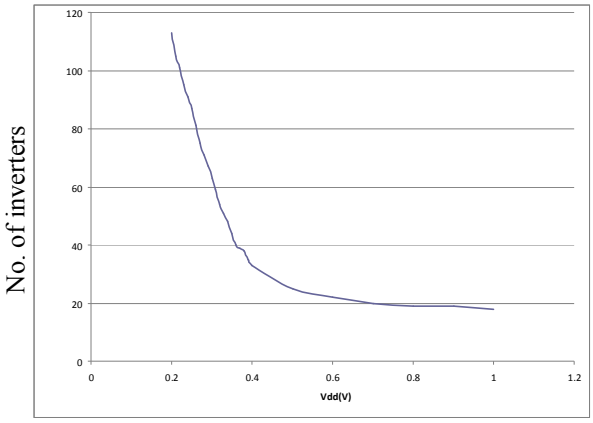

FIGURE 13 MEASUREMENT RESULT.

As all results were obtained from the Cadence Spectre analog simulation toolkit, and during simulations no other factors such as process variation were considered, the first sensor should be preferable as its better precision should translate to better control system robustness in operation.

5 CONCLUSIONS AND FUTURE WORK

In energy efficient energy harvesting systems which remove or bypass the DC/DC block, reliable references can be very hard to find. In addition, in such systems there is a need for wide-range, high-precision voltage sensors. The overt use of analog circuits should also be avoided to improve energy efficiency and low-voltage operability. To meet these requirements, a wide-range, reference-free, high-resolution voltage sensor is developed without using analog circuitry. The sensing method is based on the latency difference between two different circuits under different Vdd.

The key to this method is to find a circuit with appreciably different latency behavior from "normal" logic. An SI version of this circuit with completion detection needs to be designed to act as the event set generator (Circuit 1) of the sensor. An additional counting circuit (Circuit 2) based on normal logic, such as an inverter chain, completes the sensor. The time spent on executing an event set from Circuit 1 measured in terms of the corresponding number of events in Circuit 2 will then directly encode the current Vdd being measured.

Measurement precision depends on how different Circuit 1 behaves in terms of latency from Circuit 2 when Vdd changes. SI SRAM cells are demonstrated to be good candidates for Circuit 1 if simple inverter chains are used as Circuit 2.

A reference-free voltage sensor solution was designed by combining an SI SRAM cell as Circuit 1 and an inverter chain as Circuit 2. The sensor was implemented in UMC 90nm CMOS technology using the Cadence toolkit. Further investigations were carried out on other possible candidates for Circuit 1 with variable results.

Simulation results show the sensor based on an SI SRAM cell working as expected. The Vdd voltage can be sensed by counting the number of "1" bits latched in DFF registers. The sensor demonstrates very good precision, in the range of [1V, 0.7V], the resolution is 50mV and below 0.7V the resolution is finer than 10mV.

Meanwhile, the detection speed and power consumption are also measured. The response time is less than 2ns when voltage is 1V and less than 900ns when voltage is 200mV. The energy consumption per measurement stays low across the entire working range between 200mV and 1V, closely tracking the energy per operation curve as expected.

All experiment results were obtained through analog simulations using Cadence toolkits, without considering such factors as process variation, temperature, etc. Because of the high precision and inherent robustness of SI design it is expected that sensors of this type should be resilient under adverse conditions. However this leaves scope for future work to investigate the validity of such expectations.

In the future, we plan to analyze the proposed sensor technology with these additional factors and to test the concept through a fabricated device. It will also be very interesting to investigate the precise reason for the abnormality in Figure 11.

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