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Voltage Sensing Using an Asynchronous Charge-to-Digital Converter for Energy Harvesting Circuits

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Abstract

Energy harvesting generators deliver nondeterministic power density over a range of explicit environmental conditions. To mitigate the variability of power provided by the harvesters, this paper presents a novel energy-proportional design approach, in which the computational circuit is driven by input power so that its switching activity is a function of this power. Such an approach realizes an autonomous power gating, as the circuit starts to compute only when input power has arrived. We present a voltage sensor to exemplify the energy-proportional design principle, and such a sensor can be readily adopted in energy harvesting systems for on-chip dynamic power management. This sensor is driven by the charge from a capacitor that samples the measured input voltage to subsequently power up the asynchronous counter, which performs charge-to-digital conversion. We also present an analytical model that characterizes energy-proportional properties of the proposed voltage sensor. SPICE simulation results show that the proposed sensor design outperforms conventional voltage sensor circuits in terms of robustness and energy efficiency.

1 Introduction

Energy dissipation is one of the most important design criteria in electronic systems. Although battery is a traditional and convenient energy source, it is recently challenged by various applications with perennial operation requirements. To mitigate this challenge, research efforts have been devoted to seek alternative and renewable energy sources, such as thermal, natural vibration and solar, for micro-electricity generation[1].

Recent advancement in microelectromechanical ($MEMS$) technology presents novel design and manufacturing processes that enable integration of self-powered devices into micro-packages and integrated circuits [2]. Numerous studies have been carried out to improve the energy harvesting efficiency [3]. Such an energy harvesting system provides a promising alternative to battery-powered systems and creates an opportunity for architecture and design innovation for the exploitation of an ambient energy source. The battery-based system benefits from a relatively predictable metric of energy residual, which suffices to characterize the energy availability, and is seemingly an unbounded power supply. The design criteria for systems using an energy harvesting source are fundamentally different from those using a battery. In such a system the harvested energy supply from the ambient source is stochastic in nature and, thus, an on-line adaptation to the power supply and robust computational architecture are required to ensure a reliable system.

Previous work on energy-harvesting systems can be categorized into two main groups. In the first group, research focuses on the system-level optimization. New methods and algorithms have been introduced for effective power management [4, 5, 6, 7]. One of the major objectives is to characterize the energy supply from the ambient environment. Note that energy supply modelling is out of scope in those papers. In the second group, studies are focused on circuit-level design [8, 9, 2]. Novel analogue and power electronic circuits are proposed. Very often, it is necessary to measure energy utilization at either the load or storage, for which simple analogue-to-digital converters (ADC) are used [2]. Alternatively, one

may use an oscillator that can first convert the input voltage value to the frequency of oscillations, which is later converted into the binary code by using a counter [9]. The major issue about this approach is that stable voltage is required to power the oscillator and the counter. The stability of this voltage is necessary due to the fact that the counter is a synchronous circuit, which makes this sensor not energy-optimal for energy harvesting power sources. Thus, in our research we are motivated by finding an alternative way of building a fully autonomous voltage sensor that is better optimized for energy harvesting.

Dynamic adaptation is crucial to energy harvesting circuits because the harvester power efficiency can be maximized by varying the computational loads according to the scavenged energy at run-time. To achieve this goal, a sensor circuit is needed to measure the supplied power from the harvester in order to schedule activities in the computational circuitry. The challenge is that this sensor is also powered by the same harvester, where the power supply is either unreliable or unstable in terms of its voltage levels. This paper proposes a new approach to voltage sensing, which we later call energy-proportionality. It is based on the use of a sampling capacitor, which converts input voltage to a certain amount of energy contained in the form of a charge stored on this capacitor, plus a charge-to-digital converter that provides reliable conversion of the stored energy to a binary code on the output. This converter is built using asynchronous techniques which frees it up from an additional clock generator and stable power supply, which are normally used in conventional sensors. In this method, electric charge in the sampling capacitor is converted to the binary code as a single step. To implement that an asynchronous counter is designed to act as both an oscillator and a counter, thereby combining the two main functionalities in one circuit: converting charge to frequency and integrating frequency to code. It is crucial that every signal transition in the asynchronous counter contributes to the formation of the output code from the sensor, and each such transition consumes a certain quantum of energy taken from the sampling capacitor. Thus, the switching activity and output of the counter virtually becomes proportional to the input energy 'invested' into this computation. This constitutes what we call energy-proportional computing as discussed in the next section.

The major contributions of this work are following:

- An energy-proportional design approach as a new alternative in certain applications is introduced.
- A charge (of a sampling capacitor)-to-digital converter circuit for measuring energy which exemplifies the energy-proportional design principle is presented. The proposed sensor is based on an asynchronous counter, which operates as an oscillator and frequency divider at the same time, thereby generating the binary code that is proportional to the charge stored in the sampling capacitor.
- An analytical model is developed to capture the energy-proportional characteristics of the converter. The model characterizes the energy efficiency and relationship between the input initial voltage of sampling capacitor and output code.

2 Energy proportional computing

Most digital circuits have a set of input signals, power supply input and output signals. Power supply is usually considered independent of the information paths in the circuit. It is therefore seen as a resource that 'is always there', and hence circuits do not normally count the amount of energy taken from this resource in some explicit form. The idea of an energy-proportional circuit (EPC) is that the input energy for the circuit is somehow 'metered' in such a way that the amount of energy supplied to the circuit determines, in a proportional way, the amount of computation activity in the circuit, and can even be directly reflected in the output values produced by the circuit. From the signalling point of view, an EPC is designed in such a way that the energy supply can be extracted from the input signal. One possible way of extracting energy is to use sample and hold devices such as capacitors which can buffer energy taken from the input signal as a charge. Consequently, in this way, the EPC will operate as long as the

sufficient charge remains on the buffer capacitor. The voltage sensor considered in this paper is a type of circuit in which the design principle of energy proportionality can be readily applied.

The essential feature of the operation of an EPC connected to a particular source of energy (e.g. sampling capacitor) is that the energy taken from this source is not wasted on activities that do not directly contribute to the computations in the EPC. On the other hand, all computational activities that take place in the EPC are entirely powered by the given energy source and not supported by additional sources. The EPC concept allows us to: (a) estimate the computational activity of the circuit from the knowledge of the input energy (power, voltage), and vice versa (b) derive the amount of 'invested' energy resource into the circuit from the computational activity characteristics. As will be shown in this paper, the use of an asynchronous counter in the charge-to-digital converter meets the requirements of EPC, and we can relate the input voltage to the binary code in a proportional way. The number of signal transitions occurring in the circuit acts as a connecting factor in this relationship.

3 Voltage sensor operation

A voltage sensor is a key component in energy-aware or energy-adaptive systems. The voltage sensor provides an estimate of energy residue in the battery or energy buffer in such a way that the computational load or system power supply could be adjusted accordingly.

3.1 Sampling Circuit for Voltage Sensor

Figure 1 shows a general architecture of a voltage sensor circuit and its interconnection with the power converter and harvester [10]. The sampling circuit in this figure works in two states. In the first state or charging state S_1 is on and S_2 is off in a way that C_{sample} will be charged to $V_{in} - V_{s_1}$, where V_{s_1} is the voltage drop across S_1. In the second state or discharging state S_1 is off and S_2 is on. In this state V_{dd} which is $V_{in} - V_{s_1} - V_{s_2}$ is applied to the load which in this case is our counter, where V_{s_2} is the voltage drop across S_2.

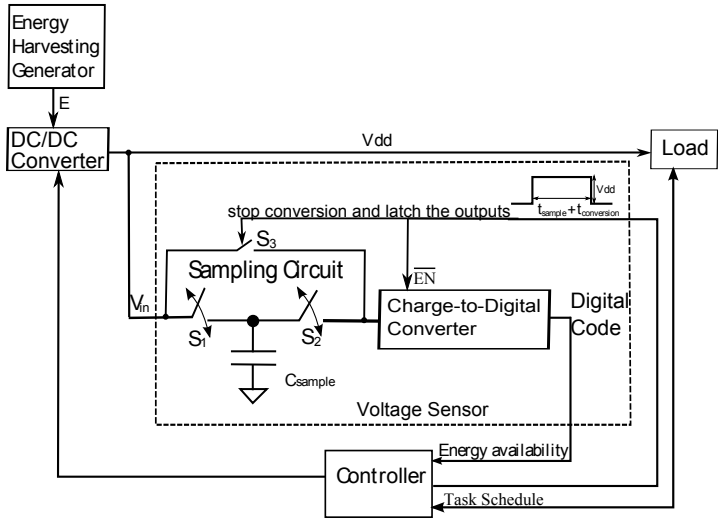

Figure 1: A system overview of a voltage sensor and its interconnection with a harvester and power converter.

The voltage sensor aims to convert the energy stored in the sampling capacitor into a digital code by a converter. One of the proposed techniques is to use a counter to count while the capacitor is discharged. At the end of discharging the output of the counter represents the amount of energy stored in the capacitor. Specifications of the counter for this voltage sensor depend on the system which sensor is used in. Systems with sufficient power budget can provide fixed voltage and fixed clock frequency. In such systems any

type of counter can be employed. But for the systems with limited power budget, such as systems using harvester as power supply, fixed voltage is not guaranteed therefore, the fixed clock frequency cannot be provided. In the latter group of systems the functionality of the synchronous counters, which directly depends on the clock frequency, might be affected. However, in case of asynchronous counters operation is clock-less. The asynchronous counter proposed in this work uses a sampling capacitor as a power supply. It counts the pulses that are generated by itself until the sampling capacitor has a sufficient charge.

3.2 Asynchronous Charge-to-Digital Converter using Toggle Logic

The binary counter is built from toggle logic blocks shown in Figure 2 and each block corresponds to a data bit. Therefore, for an n-bit counter we need n toggle blocks. The idea of a binary counter is that each bit should toggle twice more than the bit in the next stage, thus signals among the logic blocks are connected to each other in such a way as to provide the binary code in the bits with a progressively increasing weight (as power of two). The solution here is to apply Reset (R) signal from next weight bit to the feedback path and use the invert version of $\overline{Q}$ to reset bit in the next weight.

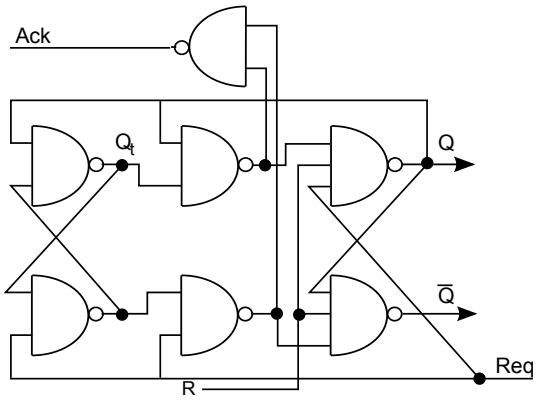

Figure 2: Schematic of an asynchronous toggle circuit which is the basic building block for the charge-to-digital converter.

In line with [11] the toggle logic takes the advantage of a flip flop design to generate Q and Q_t as shown in Figure 2. Any changes in the internal state are captured to make a transition on the Reset signal, R, to reset Q and $\overline{Q}$. As shown in Figure 2, feedback paths send Q and $\overline{Q}$ back to the flip-flop in the front part of the logic, which modifies the internal state to trigger another count. Similarly, the logic keeps toggling as long as there is enough charge (voltage level) to drive the circuit.

The schematic of an n-bit asynchronous counter is shown in Figure 3. The counter contains n stages of toggle logic, which is represented by the rectangular block TL_i, $i = 0, 2, \ldots, n-1$, and $n-1$ inverters. The outputs of the counter are Q_t0, Q_t1, ..., Q_tn-1. The V_{dd} input provides the power supply to the circuit. The counter begins to count once the supply voltage V_{dd} is applied and the counting stops when V_{dd} has decayed to a very low level, well below the MOSFET threshold voltage.

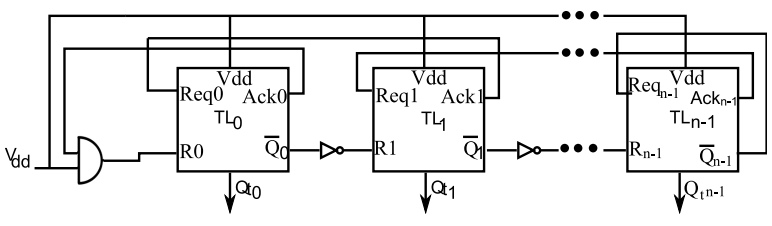

Figure 3: A general n-bit asynchronous counter based on toggle logic. This counter serves the charge-to-digital purpose in a sensor application, if the input is connected to a sampling capacitor.

4 Circuit Analysis

The counter used in the voltage sensor is the component that converts a sample of input voltage to the corresponding digital value. In this section, the relationship between the total number of counts and V_{in}(minus $V_{s1} - V_{s2}$) in Figure 1 is derived. The analytical expression for this relationship counter will be derived in two steps: (i) the number of gate transitions for each value of count, (ii) The number of transitions as a function of initial voltage. Consequently, we will be able to formulate the output of the counter as a function of initial value of input voltage V_{in}(minus $V_{s1} - V_{s2}$).

4.1 Number of transitions for each value of count

A single increment in a counting process requires several signal transitions. These transitions take place in all those toggle blocks that flip their bits during this increment action. The aim of this section is to derive a relationship between the number of transitions and the value of count. Since count is an integer, it can be expressed as follows:

$$Count = \sum_{i=0}^{n-1} b_i \cdot 2^i, \forall b_i \in \{0, 1\} \tag{1}$$

Thus, the number of transitions for each count ($NT(Count)$) is an aggregation of the number of transitions for each power of two factors in Equation 1 ($NT(2^n)$). Therefore, we can express the count using the cumulative code, which represents the number of transitions corresponding to each binary code. Hence, the number of transitions for $2^n$is:

$$NT(2^n) = \sum_{i\,=\,0}^{n-1} NT(C_i^+) + NT(C_i^-) \tag{2}$$

where $NT(C_i^+)$ is the number of logic gate transitions corresponding to the total number of times bit i flipped from 0 to 1. Similar to that $NT(C_i^-)$ is cumulative number of gate transitions for bit i flipped from 1 to 0 (see Appendix).

In order to obtain the number of transitions for the circuit presented in the previous section, we evaluate the number of transitions for all the logic gates in one of toggle block which consists of two 3-input NAND gates, five 2-input NAND gates and one inverter. For simplicity, we do not differentiate these transitions, however for a more accurate analysis they can be considered separately (e.g. as a vector). Therefore, the total number of transitions when counting to 2^n equals to:

$$NT(2^n) = 2^n \cdot 18 + \sum_{i=0}^{n-1} 2^i \cdot 20 = 38 \cdot 2^n - 20 \tag{3}$$

As we can see from the above equation, the number of transitions is a function of the word-length. Hence, the total number of transitions for any arbitrary count is:

$$NT(Count) = \sum_{i=0}^{n-1} b_i \cdot NT(2^i) \tag{4}$$

By substituting Equation 3 into Equation 4, we have:

$$NT(Count) = 38 \cdot \sum_{i=0}^{n-1} b_i \cdot 2^i - 20 \cdot \sum_{i=0}^{n-1} b_i \tag{5}$$

4.2 The Number of Transitions as a Function of Voltage

The eventual goal for this section is to determine the relationship between the initial input voltage (V_0) which used to charge the sampling capacitor and the value of output count. To achieve this goal in the first step the initial voltage is used to find the delay propagation of each gate in two regions; super-threshold and sub-threshold. Then the frequency of counter is determined by using the delay propagation of gates. Eventually, the integration of the frequency of the counter over time for the mentioned regions will give us the relationship between the initial voltage and the number of transitions which can be determined by using Equation 4.

In this sensor, input voltage is used to charge the sampling capacitor. After that the capacitor is disconnected from input voltage and used as a power supply for the counter. Therefore, the voltage sensor (sampling capacitor and counter) can be modeled as a parallel RC circuit shown in Figure 4. For this circuit we have:

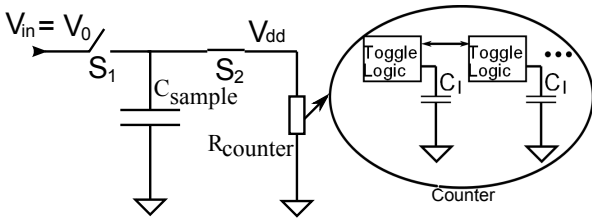

Figure 4: Electrical model of proposed charge-to-digital voltage sensor.

$$V_{dd} = V_0 e^{-\frac{t}{R_{counter} \cdot C_{sample}}} \tag{6}$$

In this equation C_{sample} is the capacitor used in the sampling circuit, $R_{counter}$ is the input resistance of the counter. It is known that there is an inverse relationship between $R_{counter}$ and V_{dd}. $R_{counter}$ can be readily obtained by calibrating the circuits. This equation shows that at fixed $R_{counter}$ and C_{sample}, V_{dd} is a function of initial voltage (V_0) which is used to charge C_{sample}. In the line with the assumption in the previous section, we consider 3-input NAND gate the same as 3 inverters and 2-input NAND gate the same as 2 inverters in terms of delay propagation. Therefore, the delay propagation of an inverter is used to find the delay propagation of the counter. We use the delay propagation models provided by [12, 13] for super-threshold and sub-threshold regions, so we have:

$$t_{p=} \begin{cases} t_{p1} = \frac{kC_l V_{dd}}{(V_{dd}-V_T)^\alpha} & V_{dd} > V_T \quad (Super-threshold) \\ t_{p2} = \frac{kC_l V_{dd}}{I_0 e^{\frac{V_{dd}-V_T}{nV_{th}}}} & 0 < V_{dd} \leq V_T \quad (Sub-threshold) \end{cases} \tag{7}$$

In these equations, V_{dd} is the supplied voltage of inverter, C_l is the output capacitance, k is delay fitting parameter, α is technology dependent parameter which is 2 in our case, V_T is the threshold voltage, V_{th} is the thermal voltage ($V_{th} = kT/q$), n is the sub-threshold slope factor and I_0 is the drain current when $V_{GS} = V_T$. Thus the delay propagation (t_p, which is either $t_{sup-threshold} = [0, t_1]$ or $t_{sub-threshold} = [t_1, t_2]$) of the inverters becomes the function of V_0. Afterwards, the frequency of the counter obtained based on the Equation 7 compared to the frequency of the counter obtained in simulation is plotted in Figure 5(a). This figure shows that using the delay propagation of an inverter to analysis the counter is a reasonable assumption.

In line with [14] the frequency of the counter, f, can be obtained using Equations 2 and 7:

$$f = \frac{Count}{t_p \cdot NT(Count)} \tag{8}$$

Then the frequency is used to determine the value of count:

$$Count = \int_0^{t_2} f dt = \int_0^{t_2} \frac{Count}{t_p \cdot NT(Count)} dt \tag{9}$$

This equation is consistent with the following relationship, which is a natural consequence of integration of the transition rate $1/t_p$ over time in order to obtain $NT(Count)$:

$NT(Count) = \int_0^{t_2} \frac{1}{t_p} dt$

$$NT(Count) = \int_0^{t_1} \frac{dt}{t_{p1}} + \int_{t1}^{t_2} \frac{dt}{t_{p2}} \tag{10}$$

By substituting Equations 7 and 6 into 10 we obtain Equation 11 (for simplicity we use C and R instead of $C_{sample}$and $R_{counter}$, respectively).

$$NT(Count) = \frac{1}{kC_l}\left[\frac{-2t_1 V_T V_0 + RCV_T}{V_0}\right] + \frac{2I_0}{kC_l}\left[\frac{-RCe^{\frac{-V_T}{nV_{th}}}[f(t_2) - f(t_1)]}{nV_{th}}\right] \tag{11}$$

where $f(t) = Ei(\frac{V_0 e^{\frac{-t}{RC}}}{nV_{th}})$, Ei is exponential integral.

Equation 11 shows the number of transitions as a function of V_0. From this expression we can see that the number of transitions also depends on several device relating parameters. In order to obtain the relationship between the count and input voltage, we can use Equations 11, 5 and 1.

5 Results and discussions

The theoretical expressions obtained in the previous section are examined and compared with the results from simulation. Also, the design of the counter proposed in this paper is compared with several different counters in this section.

5.1 Theoretical versus Simulation Results

In this section simulation results are used to support the theoretical discussion in the previous sections. Cadence tools at $90\,nm$ technology process is used for simulations. Figure 5(a) shows the frequency of the counter in equation 8 compared to the frequency obtained in simulation. Although this model of delay propagation has small difference to the simulation results, it shows this model is accurate enough to be used in analyzing the counter.

Figure 5(b) shows the number of transitions obtained by Equation 11 compared to the simulation results for the voltage sensor when $C_{sample} = 5pF$. The theoretical results captured for the voltage sensor have about 7% error to the simulation results. The difference in the results can be explained by the following reasons: (i) the delay of an inverter is used as a generic delay of each gate in the counter, (ii) an approximate equation is used for the delay propagation of an inverter, (iii) the relationship between the number of transitions and the count is non-linear, and (iv) several additional signal transitions may occur between two successive counts. It adds uncertainty to the actual number of transitions occurred in the counter whereas in our analytical model all transitions are rigidly defined.

5.2 Comparison with Synchronous Designs

The energy consumption, performance and accuracy of the voltage sensor highly depend on the counter as the converter part of the voltage sensor. Since the voltage sensor has a simple structure, different

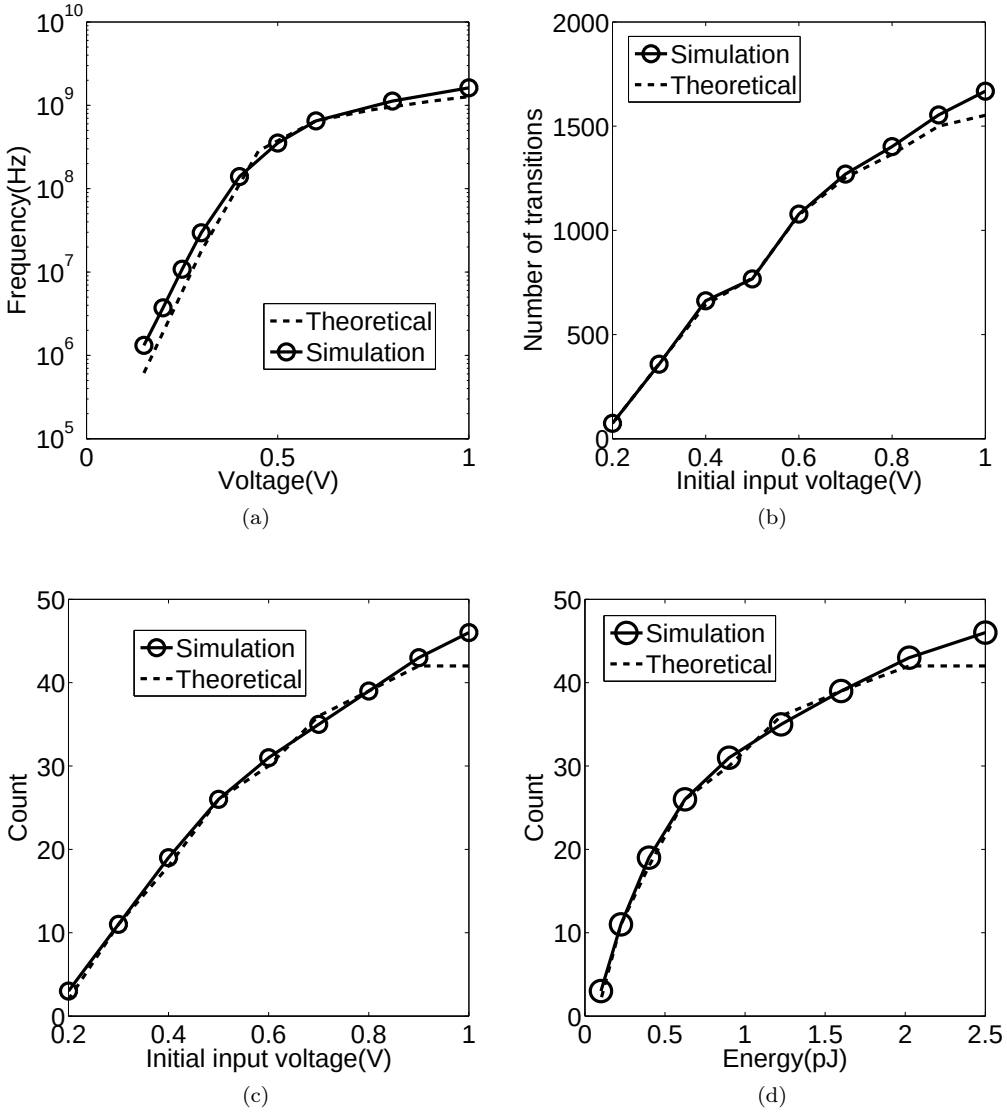

Figure 5: Comparisons between SPICE simulation and theoretical analysis illustrate the relationship between (a) frequency of counter and input voltage, (b) number of transitions over the initial input voltage, which corresponds to the supplied energy, (c) values of count against the initial input voltage, and (d) values of count against the input energy.

types of counters can be used instead of our proposed counter. In this section three different counters are designed and compared with the counter proposed in this paper. The first one is an 8-bit counter based on a JK flip flop. Unlike our counter, which does not need a clock pulse, this counter needs a clock generator. In this simulation a ring oscillator is employed to generate the clock signal for the counter. Figure 6(c) shows that the counter and clock generator are powered by the sampling capacitor. It is known that the output frequency of the ring oscillator is modulated by the V_{dd} (power supply of the ring oscillator). Therefore, by dropping V_{dd} the frequency is decreased and counter operates at a lower speed.

The second counter, is a simple 8-bit synchronous counter shown in Figure 6(a). The clock pulse for this counter is provided either by a fixed clock generator, regardless of V_{dd} or by a ring oscillator. In case of using a fixed clock generator we have a pure synchronous counter. And, if a ring oscillator is used to generate the clock pulse we refer to this counter as a semi-synchronous counter which is shown in Figure 6(b).

Based on the previous arguments, the asynchronous counter is a self-oscillating counter. Therefore, it consumes less energy to operate. Figure 7(a) shows the energy consumption of each counter to generate

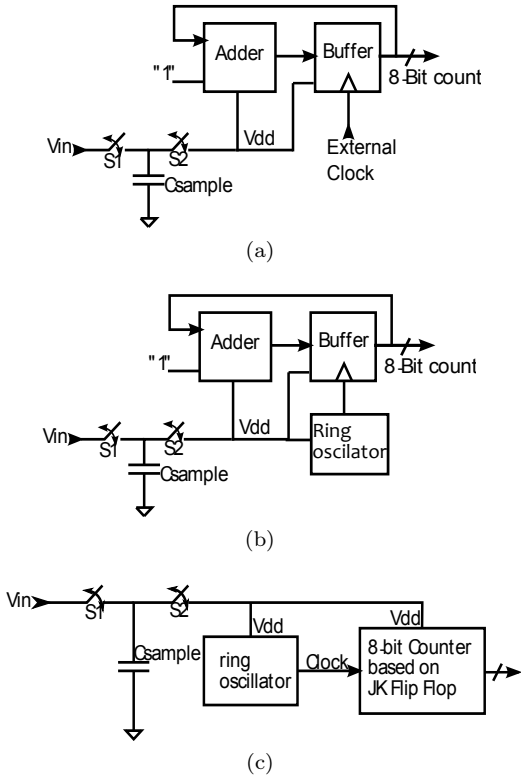

Figure 6: Benchmark circuits in the circuit comparison. All these circuits are supplied by the C_{sample}, (a) synchronous counter with an external clock, (b) semi-synchronous counter with a ring oscillator, (c) a counter based on the JK flip flop and ring oscillator.

a count at stable V_{dd}. It is seen that the asynchronous counter consumes the least energy per count compared to the other counters. The semi-synchronous counter has the highest energy consumption in this comparison. The energy consumed by the external clock generator for the synchronous counter is not included, therefore it has lower energy consumption than the semi-synchronous one, being very close to the counter based on the JK flip flop, and higher than the asynchronous counter.

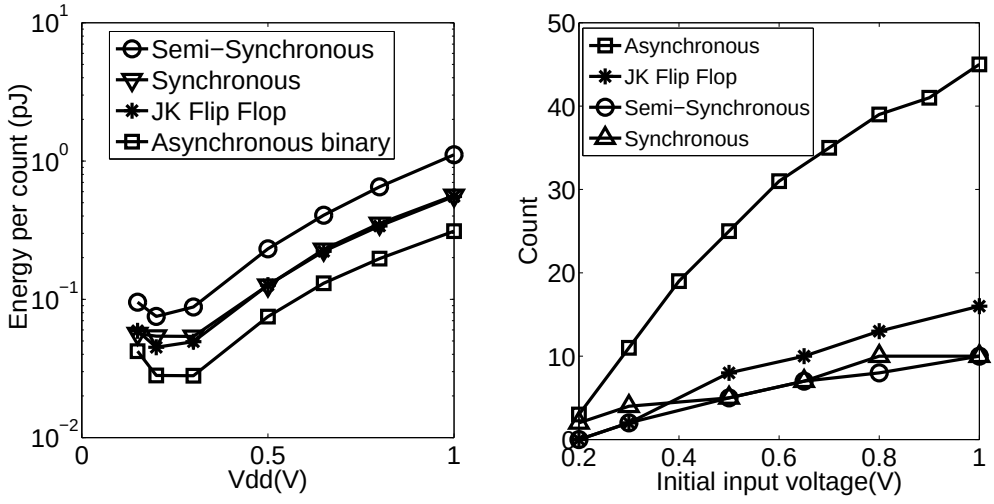

Figure 7: Comparisons of energy efficiency and circuit operating range for the different designs (a) energy per count for each counter against a fixed V_{dd}, (b) output of the counters against initial voltage, which is the energy supplied to the circuit.

The counter in the voltage sensor is in charge of converting the input voltage into a digital value.

Therefore, the output count based on the input voltage is a key parameter of performance of the voltage sensor. To measure the performance of the voltage sensor with different counters, C_{sample} in Figure **??** is charged to different values (V_0 from $1V$ down to $200mV$). Then the counters are connected to this capacitor to operate. We developed a test to make a fair comparison for all the counters considered in this paper. In this test at the first step for the asynchronous counter the frequency of the counter is captured for each input voltage (stable V_{dd}). In the next step the frequency captured in the first step is used to set the clock generator for the synchronous counter and also the ring oscillator for the semi-synchronous and JK flip flop counter. At the last step we charge $5\,pF$ sampling capacitor in Figure **??** to the voltage corresponding to the frequency which has been set for the counter. This experiment sets up a relatively fair comparison for all the counters. In this experiment all of the counters have the same amount of energy at their input and then they start operating at the same frequency. Figure 7(b) shows a wider range of output for the asynchronous counter. This implies the better use of energy to generate the count or, in other words, better performance in the sense of converting input energy to output count.

6 Conclusion

This paper presents a novel design of a voltage sensor for energy harvesting circuits based on a charge-to-digital converter. This voltage sensor consists of a capacitor-based sampling circuit and an asynchronous toggle counter circuit. The binary counter is working according to the charge stored in the sampling capacitor which is determined by the residual energy from the energy harvester. This counter does not require a separate clock, as it relies on the asynchronous hand-shaking protocol under the principle of semimodular circuits [11]. The key feature of this method is that the whole sensor is powered entirely by the energy of the charge obtained from the voltage it measures. No additional power sources or clock are needed.

An analytical model for the voltage sensor is presented. Interesting relationships between the operating frequency, output counts, number of transitions and propagation delay are derived. They are all the function of the measured voltage V_{in} and illustrate the energy proportionality of the proposed solution. Results from the analytical models have been compared with the SPICE simulation results. The relative error of the analytical model is 7% which leads to the credence of the theory. Besides, the asynchronous sensor was compared with three other conventional sensor counters where the charge-modulated pulse generation is considered separately from the counting function. It is found that the asynchronous sensor presents a wider operating range in term of voltage supply and lower power consumption. The principle presents an unique opportunity to design robust and reliable energy harvesting circuits.

7 APPENDIX

When analyzing the number of transitions for a particular count, the binary code has to be converted into cumulative code, which states the quantity of the transitions.

Table 1: Conversion from binary code to cumulative code

Count	Cumulative code (C_i^+, C_i^-)			Binary code		
0	0(0, 0)	0(0, 0)	0(0, 0)	0	0	0
1	1(1, 0)	0(0, 0)	0(0, 0)	1	0	0
2	2(1, 1)	1(1, 0)	0(0, 0)	0	1	0
3	3(2, 1)	1(1, 0)	0(0, 0)	1	1	0
4	4(2, 2)	2(1, 1)	1(1, 0)	0	0	1
5	5(3, 2)	2(1, 1)	1(1, 0)	1	0	1

Table 1 shows the value of the count in the form of binary and cumulative code for values from 0 to

5. The cumulative code shows the number of transitions quantitatively and which can be directly related to energy consumption.

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