
μSystems Research Group

School of Electrical and Electronic Engineering



**Power Delivery Mechanisms for Asynchronous Loads in
Energy Harvesting Systems**

Xuefu Zhang

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Power Delivery Mechanisms for Asynchronous Loads in Energy Harvesting Systems

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List of Publications

- **Journal**

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X. Zhang; D. Shang; F. Xia; A. Yakovlev; , "An Asynchronous-controlled On-chip Distributed Energy Delivery Method for Asynchronous Loads in Energy Harvesting Systems," Power Electronics, IEEE Transactions on, 2013 (under review).

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- **Technical Report**

Xuefu Zhang, Delong Shang, Fei Xia, Alex Yakovlev; , "A Novel Power Delivery Method for Asynchronous Loads in Energy Harvesting Systems," NCL-EECE-MSD-TR-2010-166, Microelectronic System Design Group, School of EECE, Newcastle University, December 2010.

X. Zhang; D. Shang; F. Xia; A. Yakovlev; , "Characteristic of Gated Diode Based DRAM under Low Voltage," NCL-EECE-MSD-TR-2010-157, Microelectronic System Design Group, School of EECE, Newcastle University, September 2010.

- **Demonstration**

Southampton University, July, 2012: Portable, Switched Capacitor DC/DC Converter Based Variable Vdd Powered Asynchronous Self-Timed SRAM Demonstrator (System controlled by microcontrollers).

Newcastle University, November, 2011: Energy Proportional Computing Based Hybrid Power Delivery Method Hardware Implementation and Verification for Asynchronous Loads in Energy Harvesting Systems (System controlled by FPGAs).

Abstract

For systems depending on *Energy Harvesting (EH)* methods, a fundamental contradiction in the power delivery chain has existed between conventional synchronous loads requiring a relatively stable Vdd and energy transducers unable to supply it. DC/DC conversion (e.g. *Switched Capacitor DC/DC Converter (SCC)*) has therefore been an integral part of such systems to resolve this contradiction. Asynchronous loads, in addition to their potential power-saving capabilities, can be made tolerant to a much wider range of Vdd variance. This may open up opportunities for much more energy efficient methods of power delivery.

This work firstly presents in-depth investigations into the behaviour and performance of different power delivery mechanisms driving both asynchronous and synchronous loads directly from a harvester source bypassing bulky energy buffering devices for extremely miniaturizing EH systems. A novel power delivery method, which employs a *Capacitor Bank Block (CBB)* for adaptively storing the energy from the harvesting circuit depending on load and source conditions, is developed. Its advantages, especially when driving asynchronous loads, are demonstrated through comprehensive comparative analysis.

Based on the novel CBB power delivery method, an asynchronous controller is developed for a modified CBB incorporating low-power threshold voltage sensing circuits to work with tasks. The successful asynchronous control design drives a case study that is in order to explore relations between power path and task path. Then a fundamental task and power scheduling method is developed.

To deal with different tasks with variable harvested power, systems may have a range of operation conditions and thus dynamically call for CBB or SCC type power delivery. Therefore, a new *Hybrid Capacitor Bank Blocks (HCBB)* using the same set of capacitors to form CBB or SCC is implemented with economic system size.

The power delivery mechanisms (SCC, CBB, and HCBB) is not only investigated and verified by simulations, but also by hardware implementations which are currently employed to help asynchronous-logic-based chip testing and micro-scale EH system demonstrations.

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Dr. Delong Shang, a “circuit wizard”, is an intelligent researcher in digital circuit design from large-scale (PCBs) to micro-scale (chips), from synchronous logic to asynchronous logic, and from microcontroller to FPGA. He is my friend and also my teacher. He broadened my vision in Microelectronics and has given me hundreds and thousands ideas and suggestions within recent four years.

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Acronyms

ADC	Analogue to Digital Converter
AMS	Analogue Mixed Signal
CB	Capacitor Bank
CBB	Capacitor Bank Block
CBSL	Capacitor Bank Voltage Sense Line
CC	Charge Capacitor
CEN	Capacitor Enable
ChSen	Charge Sense
ChFin	Charge Finish
ChSL	Charge Sense Line
ChSLRes	Charge Sense Line Reset
ChSwOn	Charge Switch On
CN	Change Notice
DFF	D-type flip-flop
DsChComp	Discharge Complete
DsChFin	Discharge Finish
DsChSen	Discharge Sense
DsChSL	Discharge Sense Line
DsChSLRes	Discharge Sense Line Reset
DsChSLSet	Discharge Sense Line Set
DsChSwOn	Discharge Switch On
DVFS	Dynamic Voltage and Frequency Scaling
EDA	Electronic Design Automation
EDLC	Electric Double-layer Capacitor
EH	Energy Harvesting
EMC	Electro-Magnetic Compatibility
EOC	End of Conversion
EPSRC	Engineering and Physical Sciences Research Council
FPGA	Field Programmable Gate Array

FSM	Finite State Machine
HCBB	Hybrid Capacitor Bank Block
Ipwlf	Independent Piece-Wise Linear current Source Based on File
ITRS	International Technology Roadmap for Semiconductors
Li-ion	Lithium-ion
MEMS	Micro-Electro-Mechanical Systems
MIM	Metal Insulator Metal
MPP	Maximum Power Point
MSB	Most Significant Bit
MSD	Microelectronics System Design
NextPro	Next Process
NiCd	Nickel Cadmium
NiMH	Nickel Metal Hybrid
OTA	Operational Trans-conductance Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PDU	Power Delivery Unit
PEDOT	Poly (3, 4 – ethylenedioxy - thiophene)
POR	Power-on-Reset
PP	Power Path
PSS	Poly (4 - styrenesulfonate)
PVDF	Polyvinylidene Fluoride
PWM	Pulse Width Modulation
RF	Radio Frequency
RFID	Radio Frequency Identification
SCC	Switched Capacitor DC/DC Converter
SenOutA	Sensed Output A
SenOutB	Sensed Output B
SetChAv	Set Change Available
SetDsChAv	Set Discharge Charge Available
SOC	System-on-Chip
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
StaChPro	Start Charge Process

StaDsChPro	Start Discharge Process
STG	Signal Transition Graph
TaskComp	Task Complete
TG	Transmission Gate
UGI	User Guider Interface
VChSL	Voltage at Charge Sensing Line
VDsChSL	Voltage at Discharge Sensing Line
VL	Voltage Level
VRM	Voltage Regulator Module

Chapter 1

Introduction

1.1 Motivation

- **Energy Harvesting System Needs DC/DC Conversion**

In conventional energy-constrained electronic devices such as wireless sensors, the lifetime of the sensors is an important performance indicator, as the sensors are normally powered by fixed energy supplies (e.g. non-rechargeable batteries) that lead limited operational life [1]. Additionally, practical deployment of the above systems is usually limited by the need to change batteries, and remoteness of location and low frequency of maintenance [2].

Recently, *Energy Harvesting (EH)* method with growing popularity has become an appealing solution to prolong the lifetime of electronic devices. For instance, EH method begins to be employed in large-scale, sensor-based *Wireless Sensor Networks (WSNs)* for structural health monitoring and human health monitoring [3]. Unlike non-rechargeable battery powered WSNs, EH WSNs potentially have an unlimited energy supply by harvesting environment energy from a variety of natural and man-made sources [4], such as solar, wind, vibration, and *Radio Frequency (RF)* energy.

However, in EH systems, output voltage of EH transducers (e.g. piezoelectric energy transducers [5] [6]) typically depends on the designs of devices and conditions of the environment from which energy is harvested. It usually does not coincide with the correct Vdd level for load electronics. Therefore, DC/DC conversion units are normally needed to convert unstable Vdd from EH transducers to suitable Vdd levels for load electronics.

- **On-chip DC/DC Conversion Helps System Miniaturization**

To meet requirements of EH system miniaturization, **Micro-Electro Mechanical System (MEMS)** method has become a trend to design and manufacture micro-scale EH transducers to step over physical scaling barriers [7]. RF [8] and Piezoelectric [5] MEMS EH devices are the most popular choices. On the other hand, **System-on-Chip (SoC)** method, which effectively shrinks system size, improves system performance, and reduces total energy consumption, has emerged as a promising solution for miniaturizing mixed-signal electronic devices, such as wireless network systems [9].

Thanks research achievements in realms of MEMS and SoC, micro-scale EH systems has recently drawn a great deal of research attentions [10] [11] [12] [13]. Following this trend, in order to further scale down the size of micro-scale EH systems, DC/DC conversion units, employed between MEMS EH transducers and load electronics (SoC), may be also constructed onto the same chip where the load electronics located to meet whole EH system miniaturization requirements. This is because off-chip DC/DC converting units normally employ bulky elements such as passive filtering devices – capacitors and inductors that may consume large board area. Additionally, employing off-chip DC/DC conversion method lead locating a mass of decoupling capacitors on power delivery paths which may increase power path design difficulty and board area as well [14].

To replace off-chip DC/DC conversion units, the best existing solution is **Switched Capacitor DC/DC Converters (SCC)** which may have high conversion efficiency and can be fabricated on chip [15]. Due to the constant improvement on on-chip capacitor fabrication technologies – achieving high Q and high energy density [16] [17], SCCs are predicted to be more and more popular for on-chip DC/DC conversion applications in future.

- **Multiple DC/DC Conversion Increases Load Efficiency**

For load electronics with SoC methods, more and more workloads may be placed on the same die and the system may have ability to perform multiple task computations in parallel. However, the power demands of various workloads on the same die may be different and may change with time, depending on the task (e.g. priority, deadline, or both of them) that they may run.

Therefore, fully integrating DC/DC conversion units distributed on-chip to implement *Dynamic Voltage Scaling (DVS)* for each power domain may improve load regulation and eliminate load-transient spikes caused by inductances from package and global power grid [18].

Moreover incorporating distributed on-chip DC/DC conversion units may decrease IR drop and achieve better power management compared to the lumped *Power Delivery Unit (PDU)* design (employing an on-chip large central DC/DC conversion unit) [19]. Besides, locating PDUs as close as possible to workloads may increase their power delivery efficiency as well.

- **Possible to Bypassing Energy Storage Devices**

Generally in EH systems, harvested energy needs to be buffered in bulky off-chip energy storage devices (e.g. rechargeable batteries or supercapacitors), as the harvested energy is mainly influenced by EH targets – energy sources (e.g. solar and wind) that may be uncontrollable and hard to be accurately predicted. Thereby it is usually considered to be much challenging or even impractical to directly connect EH transducers to load electronics.

However, EH power delivery method presented in [20] may provide an opportunity to directly power load electronics with EH transducers. In this work, an energy-autonomous wireless multi-source and multi-sensor node (called Managy) is introduced and its system diagram is shown in **Figure 1**. The Managy integrates on the same chip with a power harvesting and management platform, an internal sensor unit using ADC interfaces, a rechargeable battery layer deposited on the micro-system IC, and a global asynchronous digital controller.

In order to increase the overall efficiency, the Managy provides a direct power path from the energy harvesters to internal loads bypassing the rechargeable battery when obtained energy is enough to supply the loads. If not enough power has been scavenged, the indirect power path through the rechargeable battery will be used to supply the internal loads.

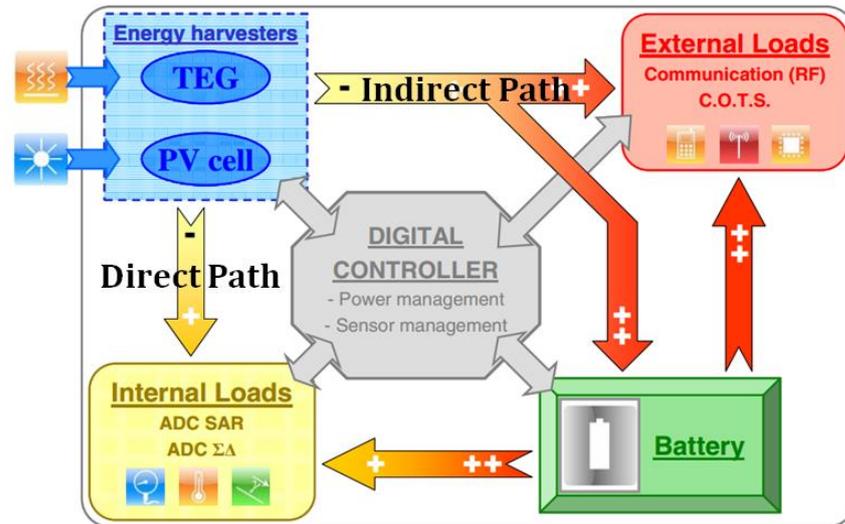


Figure 1. Managy micro-system overview [20].

Although this work has thrown light on the method of employing direct path to connect EH transducers to load electronics bypassing energy storage devices, incorporating **Low Drop Out (LDO)** linear regulators for the direct path may be not a sophisticated choice. Compared to LDO, on-chip switching DC/DC conversion units (e.g. SCC) may achieve obvious higher power delivery efficiency and more flexibility in DVS [21]. However, performances and problems of employing the switching DC/DC conversion units for such direct power path are still waiting to be investigated and crystallized. Besides, corresponding task and power scheduling method aiming for such direct power path have not been developed yet.

- **Energy Modulated Computing**

Energy-aware computations and energy-efficient systems have become popular topics of research, especially in EH systems where energy supply is nondeterministic. EH and the reality that computation is becoming more energy-bounded are some of the inspirations for the concept of energy-modulated computing [22].

EH and other energy sources employed in energy-modulated computing systems can be fundamentally different from conventional power supply method. Energy-modulated computing treats both energy availability and data/task requirements as system design variables and design objectives can span the entire range between finding the optimal task scheduling to spend a given energy profile and finding the best energy supply scheduling to best fulfil a task requirement.

For instance, in these systems the available energy may be viewed as infinite, with newer energy always available during system lifetimes but instantaneous power often unpredictable and nondeterministic, depending on the environment [22]. This has motivated various techniques in trying to smooth the power flow, including temporarily buffering harvested energy in energy storage devices, such as off-chip rechargeable batteries and supercapacitors [23], which may have a number of disadvantages [24]. On the other hand, directly delivering energy generated by harvesters to computational loads might be an alternative in some applications [25].

Energy-modulated computing aims to find better synergies between power supply and computational loads to achieve greater total energy efficiency. New ways of power supply and load design should both support more robust operation of the load under variable V_{dd} and allow the load to “scavenge” more computation from the energy provided by the power supply.

For synchronous loads, relatively stable power supplies are needed with minimum (5% to 10%) voltage variation allowed [26]. DC/DC conversion units may pass on instability in the EH voltage when an off-chip intermediate storage is not used, potentially leading to the load needing to be switched off or into sleep mode. To increase power output stability, certain DC/DC conversion designs can be dynamically switched among a number of different conversion rates at the expense of frequent mode switching. For example, variable power supply may cause frequent switching operations inside SCCs [27].

However, although the existing DC/DC conversion unit (e.g. SCC) may have an ability to regulate power from a variable power supply, the ability may be very limited. As usually existing DC/DC conversion units are originally designed for regulating power from a stable power supply that may have slight voltage variation (e.g. slight output voltage drop in a non-rechargeable battery with use time) to synchronous load electronics.

In EH systems, especially when bypassing energy storage devices and choosing the existing DC/DC conversion unit to directly regulate harvested power that may have large voltage variation or even have non-power gaps (in very short time), the

DC/DC conversion unit may not work efficiently and its performance and problems are still waiting to be explored and analyzed.

- **Asynchronous Circuits**

Asynchronous circuits are fundamentally different from synchronous circuits. Although the asynchronous circuits assume binary signals, there is no common and discrete time. The circuits incorporate handshaking between their components in order to perform the necessary synchronization, communication, and sequencing of operations. This difference gives asynchronous circuits many inherent advantages comparing with synchronous circuits [28] [29].

Except lower power consumption [30], higher operating speed [31], less emission of electro-magnetic noise [32], better composability and modularity [33], and no global clock distribution & clock skew problems [28], the asynchronous circuits also have satisfactory robustness towards variations in supply voltage [34] [35], temperature, and fabrication process parameters [36]. As Timing is based on matched delays and can even be insensitive to circuit and wire delay.

Therefore, computational loads with asynchronous logic being capable of tolerating wide voltage variations may make them good candidates for use in conventional EH systems (having energy storage devices) where the DC/DC converters may deliver regulated power but with a degree of voltage variation. However, bypassing energy storage devices and directly employing asynchronous loads to cooperate with EH transducer and DC/DC converters (without energy storage devices) has not been investigated so far. Therefore performance of the asynchronous loads running under such condition is still unknown. Besides problems arising from such power delivery path have not been crystallized. Additionally, new power delivery method especially aiming for asynchronous loads in the EH systems (bypassing energy storage devices) is still waiting to be investigated and developed.

1.2 Contributions

This research concentrates on method which deliver power directly from EH transducers via on-chip PDUs, bypassing energy storage devices, to asynchronous

computational loads to meet more and more popular trend of micro-scale EH systems and implement intelligent task and power scheduling according to novel energy modulated computing method.

Firstly, the most popular on-chip fully integrated DC/DC conversion unit – SCC is in-depth investigated by hardware implementation powering an asynchronous chip with a large output voltage range. In the investigation, the asynchronous chip shows satisfactory robustness against power supply (output of the SCC) voltage variations. It throws light on possibility of powering asynchronous loads with controllable voltage ranges rather than stable voltage levels. Additionally, microcontrollers are employed in the SCC investigation. For microcontroller programming, different control and parameter sampling methods are studied to improve the SCC performance.

Secondly, new power delivery method, based on an on-chip **Capacitor Bank Block (CBB)**, is proposed. It is aimed at providing a degree of programmability in the power delivery control so that power can be intelligently delivered under different EH source and load conditions for performance or efficiency goals. This method is comparatively investigated with a conventional SCC. The comprehensive analysis across the two different types of power delivery and synchronous and asynchronous loads represents the first attempt to systematically study the issue of on-chip power delivery directly from EH transducers to computational loads by passing bulky energy storage devices.

Thirdly, a preliminary asynchronous controller especially for CBB concept is designed. The asynchronous controller incorporating modified CBB structure and improved low-power threshold voltage sensing circuits works with voltage-variation-robustness asynchronous loads, leading the whole system getting rid of global clocks due to lots of disadvantages. Employing asynchronous logic and threshold voltage sensing technique enables energy consumption of whole **Power Delivery Unit (PDU)** to stay at a satisfactory level. Additionally, the PDU is able to implement high quality power regulation powered by V_{dd} varying in a small range. A case study targeting at relations between power path and task path is performed based on the proposed PDU. A fundamental task and power scheduling method is

developed. EH system optimization in harvested energy use or CBB PDU operational life can be achieved by incorporating this method.

Fourthly, a new ***Hybrid Power Delivery Method (HCBB)*** is designed and is able to use the same set of capacitors to form both CBB and SCC configurations which can be switched in and out at run time, effectively realizing a kind of dynamic reconfiguration of power delivery to deal with different tasks with variable harvested power. The HCBB (sharing the same set of capacitors to form CBB or SCC) effectively decreases system size and energy overheads, as on-chip capacitors for energy storage tending to be huge compared to logic. Additionally, the HCBB hardware implementation is realized. A HCBB controller is developed and verified by FPGA. The hardware is characterized with experiments using RC loads and then used as a power supply in our current variable VDD chip testing system.

The SCC, CBB, and more sophisticated HCBB concept are not only verified in simulation, but also verified by hardware implementation. The hardware implementation is used for on-chip DC/DC conversion and task and scheduling method investigation in this research. It is also employed as asynchronous chip testing platform delivering power with required voltage profiles. Additionally, achievement of the research in EH power delivery for asynchronous loads has been successfully demonstrated in Newcastle University Annual Research Conference, Holistic Energy Harvesting Adviser Board Meeting, and Energy Harvesting 2013 Forum.

1.3 Organization

The thesis is organised into eight Chapters and five Appendixes as follows:

Chapter 1 (Introduction) motivates necessity of developing an on-chip power delivery method for micro-EH systems to deliver harvested power directly to asynchronous loads bypassing bulky energy storage device. Contributions are also discussed in this chapter.

Chapter 2 (Background) presents a detailed introduction regarding a micro-scale EH systems including energy transducers, energy storage devices, and conventional power delivery method.

Chapter 3 (Baseline Research) introduces the state of art on-chip power delivery methods for multi-core systems and compares with off-chip power delivery methods. Then on-chip switching DC/DC conversion units are reviewed. Besides on-chip voltage sensing technologies are introduced and discussed.

Chapter 4 (Switched Capacitor DC/DC Converter Investigation) reports an investigation performed on SCC including SCC working principle, hardware implementation and verification with RC load and asynchronous self-timed SRAM chip.

Chapter 5 (A Novel Power Delivery Method) describes a novel on-chip power delivery method in a micro-scale EH system for directly powering asynchronous loads from an energy transducer bypassing traditional energy storage devices. Comparative studies have been done by separately employing the proposed CBB and a traditional SCC as the PDU in such EH system powering synchronous and asynchronous loads. The performance and behaviour of the PDUs and loads are compared and discussed.

Chapter 6 (Asynchronous Controller for Capacitor Bank Block) presents a preliminary asynchronous controller design cooperating with modified CBB and improved low-power threshold voltage sensing circuits in order to work with tasks. A case study has been done to develop fundamental task and power scheduling method based on the proposed PDU.

Chapter 7 (A Hybrid Power Delivery Method) introduces a design of a new HCBB using the same set of capacitors to behave like CBB or SCC for EH power delivery to implement a degree of task and power scheduling. The HCBB connection topology, control method, hardware implementation and verification are introduced. And the HCBB performance and potential of implementing task and power scheduling is presented and discussed.

Chapter 8 (Conclusion and Future Work) summarises the contributions of this thesis as presented in the previous chapters, and discusses areas of future work.

Appendix A (Photos & Pictures) includes photos and pictures regarding PDU hardware implementation and verification for demonstrations.

Appendix B (Program Flowcharts) shows different programming methods in program flowcharts for a microcontroller to implement different control for the SCC PDU.

Appendix C (EQN Files for CBB Asynchronous Controller Models) lists EQN files used to implement an asynchronous controller to incorporate a modified CBB structure and threshold voltage sensing circuit to work with tasks.

Appendix D (Recently Published SCC Results) reports specifications of recently published SCC work in a table.

Appendix E (Discharge Ranges of CBs with Different Capacitance Value) includes investigated data of a case study for developing a fundamental task and power scheduling method based on the proposed CBB concept.

Chapter 2

Background

This chapter provides fundamental introduction of incorporating *Energy Harvesting (EH)* methods to power micro-scale electronic systems in first Section. In second section, various ambient energy sources and transducers are introduced. Details of micro-scale piezoelectric energy transducers used as examples are reviewed in the same section. Energy storage devices, popular and widely used in micro-scale EH systems, are introduced in the third section. In the last section, conventional power delivery method for micro-scale EH systems are discussed.

2.1 Energy Harvesting Methods for Micro-scale Electronic Systems

In recent years, micro-scale electronic systems have evolved significantly due to on-chip circuit research advancing forward in direction of high frequency, high integration density and low power. However, in the trend of further shrinking and minimizing system size, the lifetime of battery-powered systems may meet a fundamental limitation due to slower development of battery technology, limited energy storing space and high cost of replacement [1]. Therefore, EH technology, scavenging energy from environment without generating any hazardous substances, has been explored to provide renewable energy for micro-scale electronic systems.

To meet requirements of system miniaturisation, EH methods to power up rechargeable battery or supercapacitor powered micro-scale electronic devices such as mobile devices and wireless sensor nodes has attracted immense research interests [37] [38] [39]. The amount of power required for those applications may reach a few hundreds of milliwatts. Some wireless sensor nodes have been successfully powered by energy scavenged from ambient sources such as solar, heat, and vibrations, for example EH powered sensor nodes (Heliomote [40],

Hydro Watch [41], Everlast [42], SolarBiscuit [43], Sunflower [44], Prometheus [45] and AmbiMax [46]).

A general block diagram of a micro-scale EH system is shown in **Figure 2** [47]. It contains five main blocks: micro-scale energy transducer, power converter, control unit, energy buffer, and application unit.

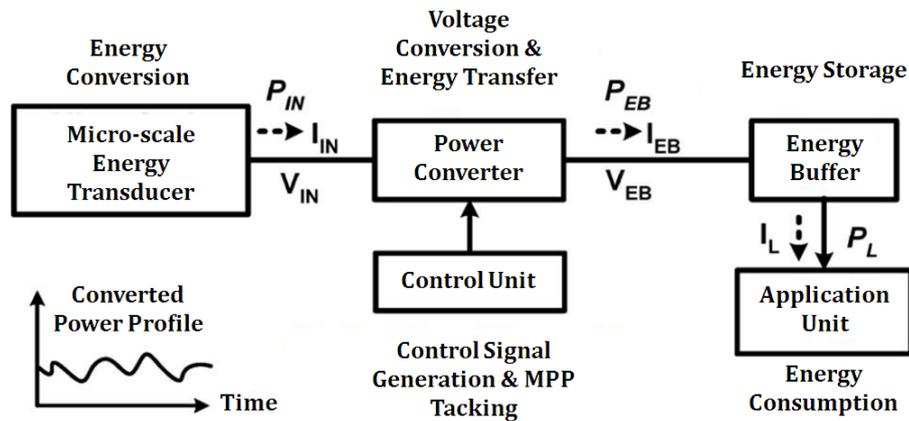


Figure 2. Block diagram of a micro-scale energy harvesting system [47].

For the micro-scale energy transducer, it is able to convert ambient energy to electrical energy. However, due to the change of environment, the converted power may not be stable and may vary in a large range with time. The converted power profile is shown in **Figure 2**. Besides the micro-scale energy transducer block may be based on a single energy conversion mechanism [48] [49] or a hybrid mechanism [50] [51].

The power converter is used to draw maximum power from the energy transducer and deliver the conditioned power to the energy storage or directly to the application unit with minimum power loss. To achieve high efficient power transfer and delivery, the control unit is employed to ensure **Maximum Power Point (MPP)** operation at all the times by running a tracking scheme, such as incorporating MPP tracking for electromagnetic energy transducers [52] and piezoelectric energy transducers [53]. Additionally, the control unit may have ability to tune the energy transducer as well. For example, tuneable piezoelectric EH system designs have been reported in [54] [55].

Usually, harvested energy will be buffered in energy storage devices such as supercapacitors or rechargeable batteries before delivered to the application unit.

As output power of energy transducers may be unstable and change with time, most of electronic devices with synchronous logic may be unsuitable to work with such variable power supply. It is normally considered to be much challenging or even impractical to directly use an energy transducer to power an application unit that is designed with synchronous logic.

2.2 Energy Transducer

Table I. Listing and characterization of energy sources [58].

Energy Source	Harvesting Technology	Amount of Energy Available	Conversion Efficiency	Amount of Energy Harvested
Solar [40]	Solar Cells	100 mW/cm ²	15 %	15 mW/cm ²
Wind [45]	Anemometer	-	-	1200 mWh/day
Finger Motion [59]	Piezoelectric	19 mW	11 %	2.1 mW
Footfalls [60]	Piezoelectric	67 W	7.5 %	5 W
Vibration in Indoor Environments [61]	Electromagnetic Induction	-	-	0.2 mW/cm ²
Exhalation [59]	Breath Masks	1 W	40 %	0.4 W
Breathing [59]	Ratchet-Flywheel	0.83 W	50 %	0.42 W
Blood Pressure [59]	Micro-Generator	0.93 W	40 %	0.37 W
Electromagnetic wave	RF Antenna	-	-	60 μ W [62] and 109 μ W [63]

The classification of EH can be organized on basis of the form of energy. The various sources for EH are photovoltaic cells, wind turbines, thermoelectric generator and mechanical vibration devices, **Radio Frequency (RF)** electromagnetic antenna and so on [56] [57]

Table I shows some of the harvesting method with their characterization [58]. For the listed harvesting methods, they can be categorized into two groups: 1) ambient energy source such as solar, wind, vibration and RF energy, and 2) human power harvested from body movements.

For the ambient energy source, most of them may be uncontrollable but predictable such as solar and wind energy. They only can be harvested whenever available. If the energy source is predictable then a prediction model that forecasts its availability can be used to indicate the time of next recharge cycle. For the human power, some of them may be fully controllable such as finger motion and

foot falls. In this case, energy may be harvested whenever required without any prediction on the energy source.

2.2.1 Piezoelectric Energy Harvesting

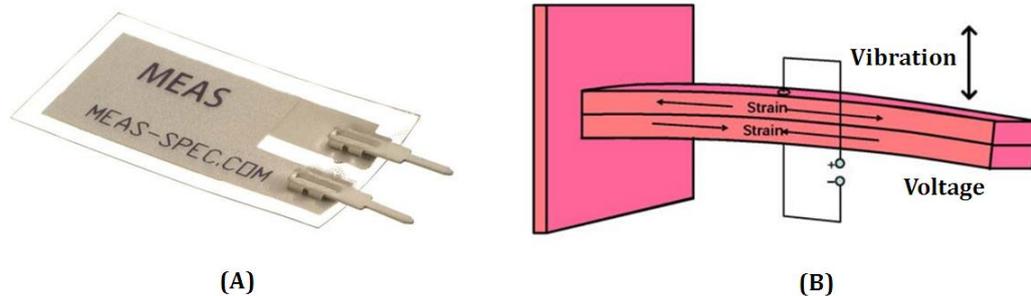


Figure 3. (A) Commercial piezoelectric film transducer [66] and (B) an example of using piezoelectric energy transducer [67].

Mechanical EH may be the most promising of several EH techniques – mechanical, thermal, light, electromagnetic, human body and so on [64]. The Mechanical EH uses piezoelectric components that are deformed by different means. The deformations are directly converted to an electrical charge via a direct piezoelectric effect. This electrical charge can be subsequently regulated and stored before using by the electronic devices where the replacement of batteries is impractical, such as the wireless micro sensor networks, implementable medical electronic, and tire pressure sensor system [65].

Figure 3 (A) shows a commercial piezoelectric film transducer. And an example of harvesting electrical energy from deformation of a piezoelectric energy transducer caused by vibrations is shown in **(B)**.

The electrical energy at the output of the transducer is a strong and irregular function of time; hence, an AC-DC rectifier is needed to produce a DC supply source for the EH system. There are two type of conventional rectifier: full bridge rectifier and voltage doubler. The limitations of the conventional piezoelectric EH architectures and replacements with higher power extraction efficiency are reported in [67] [68].

- **Piezoelectric Energy Harvesting Circuit Model**

A simple model of a piezoelectric EH circuit [69] is shown in **Figure 4 (A)**. This model consists of a sinusoidal AC source and a four-diode rectifier (full bridge

rectifier). The output waveforms of the model are shown in **Figure 4 (B)**. Here $i_p(t)$ is the AC generated from the piezoelectric element, $i_o(t)$ is the variable DC with obvious non-power gap flowing through load.

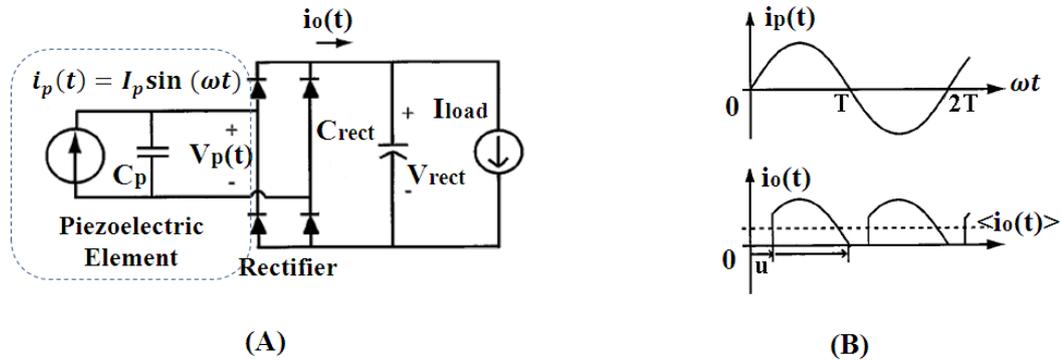


Figure 4. (A) Piezoelectric energy harvesting circuit model and (B) current waveforms.

- **Working in Wide Range of Frequency**

For the traditional piezoelectric energy transducers, the most common and widely employed piezoelectric material is Lead Zirconate titanate [70] [71]. It is usually brittle, thereby causing limitations in the applied strain. Additionally, when it is subjected to high-frequency motions, this material is susceptible to fatigue crack and can be easily damaged [72] [73].

To step over the limitation of the traditional piezoelectric energy transducers and improve their efficiency and flexibility, more flexible piezoelectric material such as **Polyvinylidene Fluoride (PVDF)** is developed and investigated in applications [74] [75]. Thanks new piezoelectric materials, the piezoelectric energy transducer is able to work with vibration sources in a range from a few tenth of Hz to tenth of kHz [64] [76] [77] [78].

Furthermore, a PVDF film coated with **Poly (3, 4 - ethylenedioxy - thiophene) (PEDOT)** and **Poly (4 - styrenesulfonate) (PSS)** electrodes was investigated in [73] [79]. The results showed that the PEDOT/PSS film is able to work with a 1 MHz vibration source without damage to the film and electrodes. Consequently, the electrodes have an important influence on the behaviour of the piezoelectric material. The results also showed that piezoelectric energy transducer can operate over a wide range of frequencies.

Besides, piezoelectric energy transducers have been widely employed to harvest energy not only from normal ambient vibrations and but also from aero-elastic vibrations [80]. Based on *Micro-Electro-Mechanical Systems (MEMS)* technologies, piezoelectric membranes [81] are employed for micro-scale EH transducers that can be fully integrated on ICs without traditional electrode connections thereby are able to work in a high frequency (up to MHz) [82].

Cranfield University, UK has reported a piezoelectric micro ultrasound transducer design working in MHz range is able to be used for EH applications [83]. The transducers was presented in Energy Harvesting 2013 [84] shown in Appendix A, **Figure 75**. Additionally, TIMA laboratory located at Grenoble, France [85] reports a fabrication of PZT/Si piezoelectric micro-machined ultrasonic transducers first designed for ultrasonic imaging applications [86] that can be used as a mechanical to electrical energy transformer for EH. This design is able to convert acoustic energy in a large frequency range (a few tenth of kHz to several tenth of MHz) to electrical energy.

2.3 Energy Storage

For energy storage, there are mainly three types: non-rechargeable battery, rechargeable battery and supercapacitor. This section comparatively introduces and discusses advantages and disadvantages of these energy storage devices.

2.3.1 Non-rechargeable Vs Rechargeable Batteries

For modern commercial batteries, there are two main kinds of batteries, primary batteries (non-rechargeable, such as alkaline and lithium) [87] and secondary batteries (rechargeable, such as *Nickel Cadmium (NiCd)*, *Nickel Metal Hybrid (NiMH)*, and *Lithium-ion (Li-ion)*) [88].

The primary battery is designed to be used once and discarded, and not recharged with electricity and reused. The electrochemical reaction occurring in the primary battery is not reversible. When the battery is in use, the electrochemical reaction uses the chemicals that generate the power. When the chemicals are exhausted, the battery stops producing electricity and the battery is

useless and only recycled. For secondary battery, the electrochemical reaction can be reversed by running a current into the battery with a battery charger to recharge it, regenerating the chemical reactants [89].

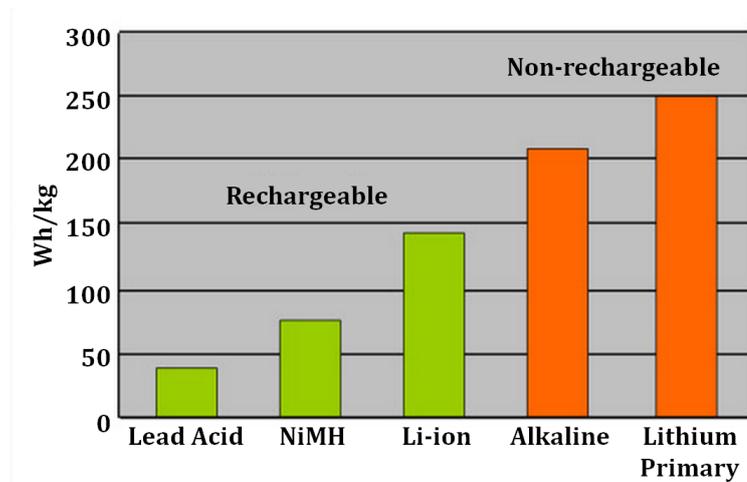


Figure 5. Specific energy comparison of secondary and primary batteries. [87]

Compared with secondary batteries, the primary batteries usually have higher energy densities [90]. Although secondary batteries have been improved, a regular household alkaline provides 50 percent more energy than lithium-ion. **Figure 5** compares the typical gravimetric energy densities of lead acid, NiMH, Li-ion, alkaline and lithium batteries. Additionally, the primary batteries also have lower self-discharge rate (alkaline 2-3 %per year, lithium 10% in five years) [91], much longer shelf life (alkaline 7-10 years and lithium 10-15 years) [92], and lower initial cost [93].

For primary batteries, compared with alkaline batteries, the lithium batteries are good at powering high drain devices [94]. On the other hand, alkaline batteries usually have lower self-discharge rate in room temperature. And powering low drain devices is able to maximize the longevity of the alkaline batteries.

2.3.2 Supercapacitors Vs Rechargeable Batteries

Supercapacitors (also known as ultracapacitors or **Electric Double-layer Capacitors (EDLCs)**) utilize high surface area electrode materials and thin electrolytic dielectrics to achieve capacitances several orders of magnitude larger than conventional capacitors [95] [96]. They are widely employed to 1) store harvested energy for many electronic devices such as wireless sensor nodes [4]

[97], 2) work as low-maintenance memory backup to bridge short power interruptions [98], 3) deliver high current to drive hybrid vehicles [99], and so on.

Table II. Performance comparison between supercapacitor and Li-ion [100].

Function	Supercapacitor	Lithium-ion (general)
Charge time	1 – 10 seconds	10 – 60 minutes
Cycle life	1 million or 30,000h	500 and higher
Cell voltage	2.3 to 2.75 V	3.6 to 3.7 V
Specific energy (Wh/kg)	5 (typical)	100 – 200
Specific power (W/kg)	Up to 10,000	1,000 to 3,000
Cost per Wh	\$20 (typical)	\$0.50 – \$1.00 (large system)
Service life (in vehicle)	10 to 15 years	5 to 10 years
Charge temperature	-40 to 65°C	0 to 45°C
Discharge temperature	-40 to 65°C	-20 to 60°C

Table II shows the performance comparison between supercapacitor and Li-ion rechargeable battery [100]. The supercapacitor has merit for application where charging or discharging with high current rates is needed for only a few seconds [101]. Additionally, the supercapacitor has extremely long life cycles (without any memory effect compare with the rechargeable battery) and long service life as well. It also has excellent low-temperature charge and discharge performance.

However, the supercapacitor has poor volumetric and gravimetric energy density compared with the rechargeable battery. It suffers higher self-discharge than most batteries. It also has high cost per watt.

The supercapacitor is able to be charged to 2.3 to 2.75 V and can withstand higher volts. However, voltage higher than 2.8 V will reduce the service life of the supercapacitor. To achieve higher voltages, several supercapacitors can be connected in series but the series connection decreases the total capacitance.

The discharge curve may be a disadvantage to supercapacitors. For electrochemical batteries, they deliver a steady voltage in the usable power band. However, the voltage of the supercapacitor decreases on a linear scale from full to zero voltage. This may reduce the usable power spectrum and much of the stored

energy may be left behind, as the voltage level at the supercapacitor may be lower than the cut-off voltage level of loads.

2.4 Conventional Power Delivery Method for Micro-scale Energy Harvesting Systems

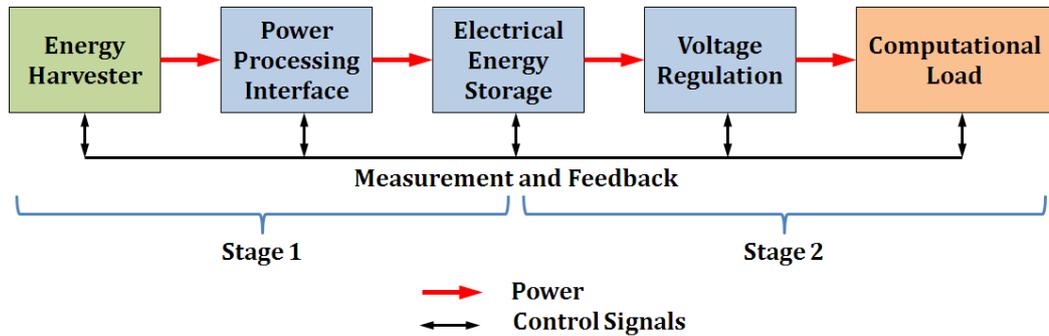


Figure 6. Typical micro-scale EH system [102].

A typical micro-scale EH system is shown in **Figure 6** [102]. The whole power delivery process is comprised of two stages. Stage 1 (energy accumulation) is from the energy harvester to the electrical energy storage and Stage 2 (energy use) is from the electrical energy storage to the computational load. For each block, voltage and current parameters will be measured and feedbacks will be employed as control references for the whole system.

In the system, an EH unit is incorporated to convert ambient energy to electrical energy. A power processing interface is employed to condition the harvested electrical energy for attaining an appropriate DC voltage to charge an electrical energy storage unit and tune the EH unit in order to draw maximum input power [103]. The electrical energy storage unit is used to buffer the harvested energy, as the ambient energy source may be uncontrollable and unpredictable. When the energy is needed by a computational load, a voltage regulation unit will be enabled to deliver power with a proper voltage level to the computational load.

2.4.1 Power Delivery Method for Stage 1

In **Figure 7** [104], a traditional power delivery method for Stage 1 is presented. A piezoelectric energy transducer is employed. The harvested energy with AC characteristic will be rectified by a full-bridge rectifier. A capacitor located at the

output of the rectifier is used to smooth the output voltage ripples varying in a large range.

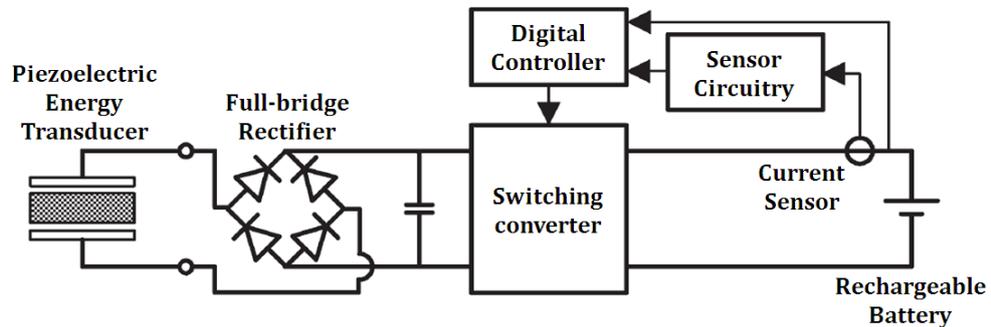


Figure 7. Conventional power delivery method for Stage 1 [104].

A switching converter is incorporated to regulate the harvested energy with acceptable voltage level to charge a rechargeable battery used as the electrical energy storage. The most popular switching DC/DC converters used for charging rechargeable batteries are buck-boost converters due to its mature technology and high efficiency [105] [106]. A digital controller cooperating a current sensor is able to maximize the extracted power by adjusting the control signal duty cycle (**Pulse Width Modulation (PWM)**) of the switching converter based on the monitored output current variations [107] [108] [109].

2.4.2 Power Delivery Method for Stage 2

A traditional off-chip power delivery method for stage 2 is shown in **Figure 8**. The harvested energy is delivered to an on-chip IC. Before the load (on-chip IC) starts computation, the system needs to buffer the conditioned harvested energy using the energy storage device (e.g. rechargeable battery).

Then a **Voltage Regulator Module (VRM)** (normally a buck converter chip with off-chip inductive and capacitive filters [110]) will be used to deliver power from the storage device in high voltage level to the target on-chip IC in a stable low voltage level, e.g. 1 V for UMC 90nm CMOS technology [111].

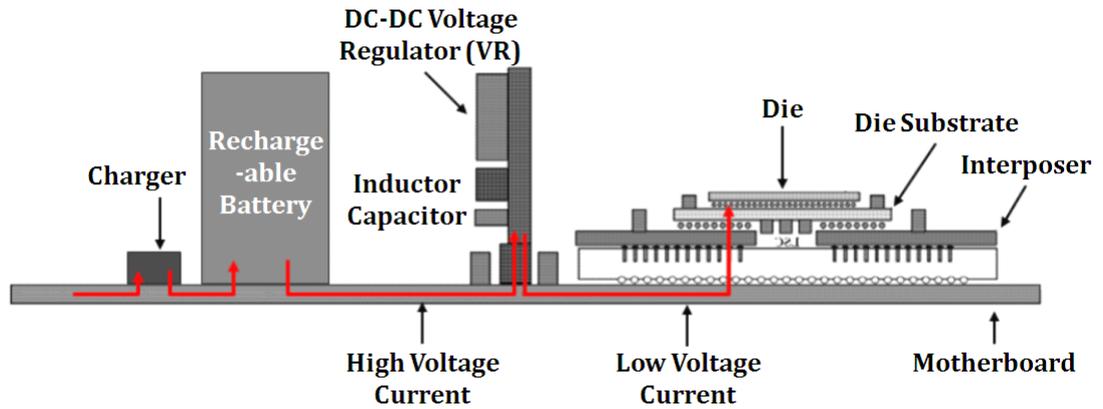


Figure 8. Conventional power delivery method for Stage 2.

However employing an off-chip VRM mounted on a motherboard, may have some foundational limitations in meeting future IC technology needs. One of the most critical problem of using off-chip VRM to power on-chip ICs is the long interconnect between the VRM and ICs. The parasitic inductance of the interconnect generates large di/dt noise, forcing the use of large numbers of decoupling capacitors at various locations along the power delivery path [14]. This may increase board area and design complexity.

Chapter 3

Baseline Research

This chapter presents the state of art researches in on-chip power delivery for multi-core systems. First of all, comparisons of on-chip and off-chip distributed power delivery methods for multi-core systems are introduced. Then, on-chip **Power Delivery Units (PDU)** such as buck converters and **Switched Capacitor DC/DC Converters (SCC)** are reviewed. Finally, on-chip voltage sensing methods that are very relevant to the on-chip power regulation are discussed.

3.1 On-Chip Power Delivery for Multi-core Systems

In order to effectively shrink system size, improve system performance, and reduce energy consumption, **System-on-Chip (SoC)** method emerges as a promising solution for mixed signal applications, such as SoC for wireless communication in ambient-Intelligence [112], neuroscience [113] and biomedical [114] applications.

In such systems, more and more cores may be placed on the same die [115] [116] and the system may have ability to perform multiple tasks in parallel [9] [117]. However, the power demands of various cores on the same die may be different and may change with time, depending on the task that they may run. In order to achieve high power efficiency, **Dynamic Voltage Scaling (DVS)** has been widely studied and many researches are attempted [118] [119].

3.1.1 Off-Chip Vs On-Chip Power Delivery for Multi-cores

- **Off-Chip Power Delivery**

In [120], an optimal design of **Power Delivery Network (PDN)** for multiple voltage-island SoCs is presented. In the system, power is regulated separately by four off-chip **Voltage Regulator Modules (VRM)**. The regulated power with different V_{out} is delivered to the chip where different components are integrated.

By using an on-chip power switch network (PMOS transistors), the regulated power with different V_{out} can be assigned to different components according to need of the system. In the system, a dynamic power management is implemented and it can effectively reduce the whole system power consumption.

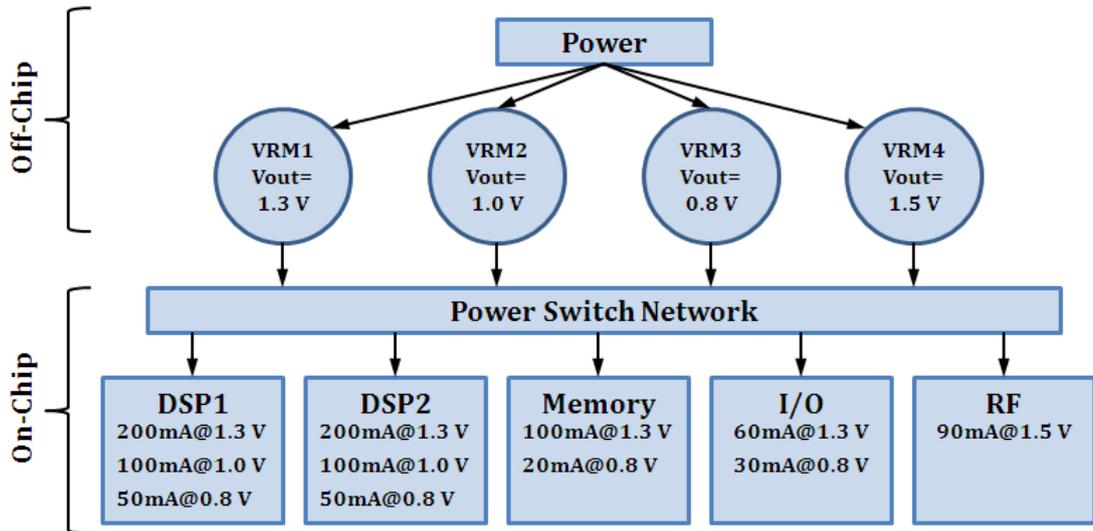


Figure 9. Architecture of a PDN to implement DVS [120].

However, employing multiple off-chip VRMs to implement multiple voltage rails to SoC requires lots of bond wire connections to the chip and needs high quality passive components, drawing additional consideration regarding *Electromagnetic compatibility (EMC)* specifications [121]. Additionally, the costs and sizes of such bulky modules severely limit their use for multiple voltage domain regulation. [18].

- **On-Chip Power Delivery**

In order to overcome the challenges mentioned above, there is significant interest in developing fully integrated on-chip voltage regulators. According to previous studies [122], on-chip regulators can significantly improve load regulation, reduce crosstalk, eliminate load-transient spikes caused by bond-wire and package inductances, and save board space as well as external pins. On the other hand, due to the small size, it is possible to integrate many voltage regulators on chip to implement fine-grained multiple power domains [123].

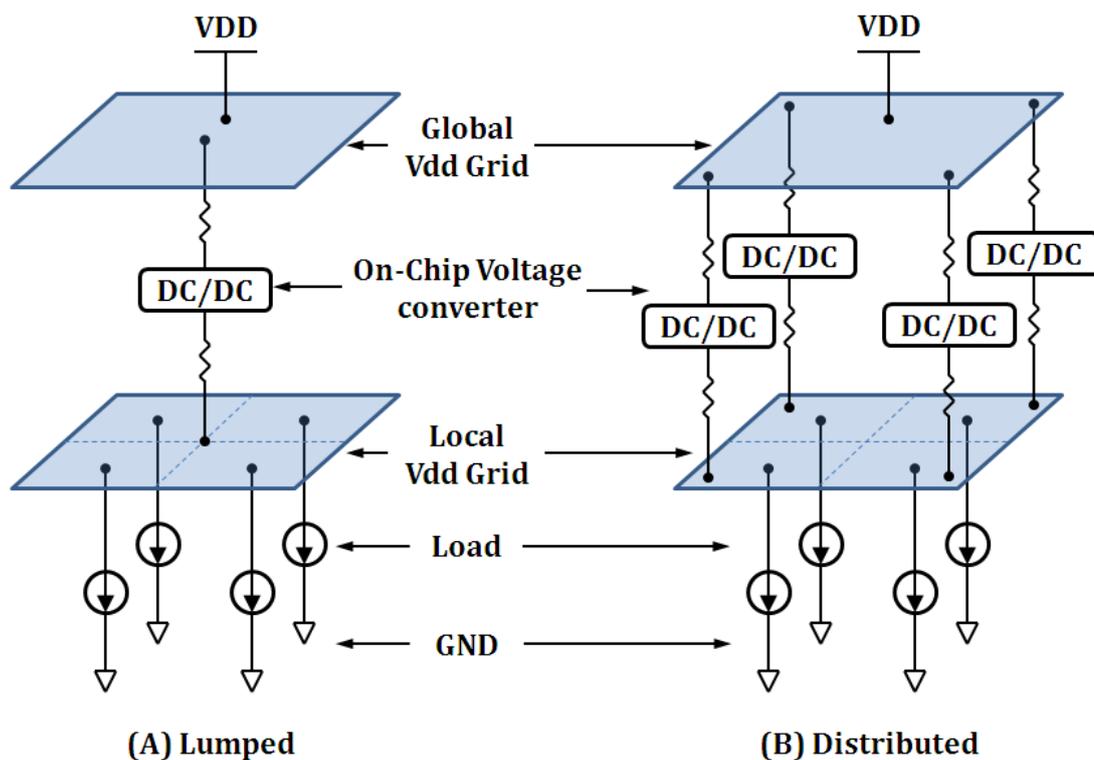


Figure 10. Lumped Vs. distributed on chip DC/DC converters [19].

In [19], an on-chip distributed PDN design employing fully integrated DC/DC converters are presented and compared with a traditional lumped PDN design (see Figure 10). In (A), a large central converter is used to deliver power to all the loads in the DVS cluster or the whole chip. In (B), several distributed smaller converters are employed to power nearby loads. In this work, the distributed PDN design effectively decreases up to 74% IR drop and achieves better power management compared to the lumped PDU design.

3.2 On-Chip Power Delivery Units

To implement on-chip power regulation, DC/DC converters are usually employed. The DC/DC converter designs range from low-dropout linear regulators to buck converters to SCCs [124].

In the past, on-chip voltage conversions were primarily implemented by using linear converters due to the ease of integration and the low area overhead. However, they normally have a maximum efficiency limit given by the ratio of output voltage to input voltage. Therefore, as on-chip digital supply voltages

continue to decrease, the growing difference between the digital supply and the off-chip supply makes the disadvantage of their efficiency more obvious [21].

Nowadays, compared with the linear regulators, incorporating switching mode converters (such as buck converters or SCCs) may be a better choice for on-chip DC/DC conversion, as switching converters are able to maintain high efficiency across a wide range of output voltages, thereby are prevalently studied and applied for on-chip power delivery.

3.2.1 Buck Converter

For on-chip buck converter designs, one of the main challenges is requiring a large, high quality inductor, which is difficult to integrate on-chip [124]. The value, physical size, and parasitic impedances of inductive elements to implement buck converters may be reduced by increasing switching frequency to compensate [125] [126]. Other solutions such as using 3-D stacking chip technologies and interleaved topologies are also employed to overcome this issue.

- **Buck Converter Implemented by Stacking Chips**

An on-chip buck converter which is implemented by stacking chips and suitable for on-chip distributed power supply systems is presented in [127]. The schematic of the buck converter is shown in **Figure 11 (A)**. For the operation principle of the buck converter, two power MOSFETs labelled as P1 and N1 are employed to generate an AC signal at Node1 by a non-overlapping switching action controlled by an off-chip controller through the ring oscillator and triangular wave generator. Then the AC signal at Node1 is applied to the LC output filter and the DC component of the AC signal will be delivered to loads through the output of the convertor. At the meantime, the off-chip controller will monitor the output and is able to implement close-loop control.

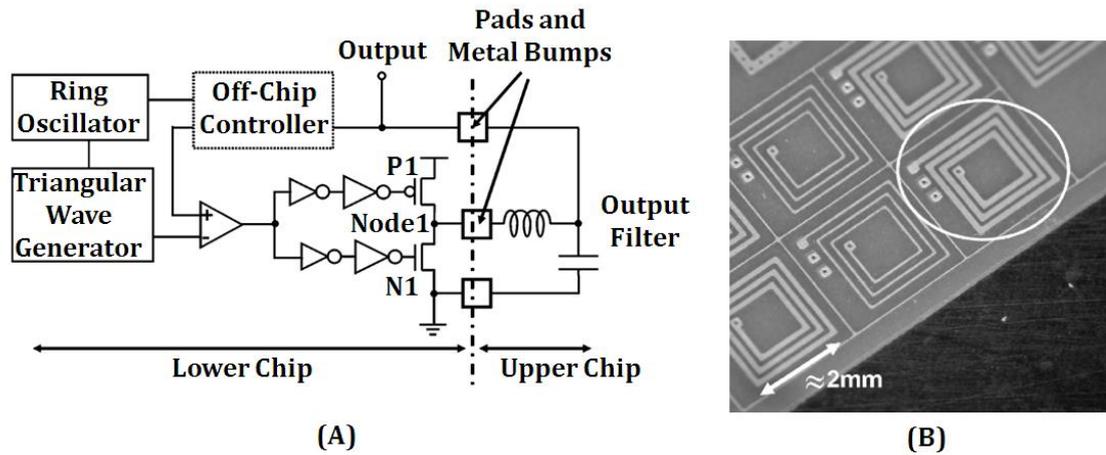


Figure 11. (A) Stacked-chip implementation of buck converter and (B) 2x2 mm on-chip LC output filter [127].

Based on using 3-D chip stacking technology, the buck converter is comprised of two chips both fabricated in 0.35 μm CMOS technology. The lower chip contains a ring oscillator, triangular wave generator and switching transistors of the buck converter and target circuits (loads). The upper chip contains LC output filter elements, shown in **Figure 11 (B)**. These two chips are stacked face to face and connected via metal bumps. The lower chip may be fabricated in an advanced technology and upper chip in conventional and cheap process technology. In this case, the on-chip distributed power supply systems may achieve a good balance for best cost and power trade-off.

However, it is a truth that non-fully-integrated switching DC/DC converter may still suffer energy dissipation caused by the parasitic impedances of interconnect between two devices (such as the filter inductor, filter capacitor, power transistors, and pulse width modulation circuitry) [128]. Therefore if the buck converter is fully integrated, the energy dissipated on interconnects may be further saved.

- **Buck Converter with Different Interleaved Topologies**

The standard interleaved topology, shown in **Figure 12 (A)**, is a well-know design for enabling lower inductance output filters that can respond more rapidly to changing of load condition than a signal-phase realization [129]. The standard interleaved converter is comprised of multiple buck converters that are connected in parallel and running out of phase of one another. The voltage ripples at the output can be partly removed by employing switching signal S_s and S_P whose timing diagrams are show in **Figure 12 (A)**. The number of phases and duty cycle

decides the effect of ripple cancellation. For example, a two-phase topology only implements complete cancellation at a 50% duty cycle. Thus, on-chip buck converters usually incorporate multiple-phase topologies to achieve required ripple cancellation effect. An improved design, shown in Figure 12 (B), employs a stacked interleaved topology and is able to perform complete ripple cancellation across all duty cycles [21].

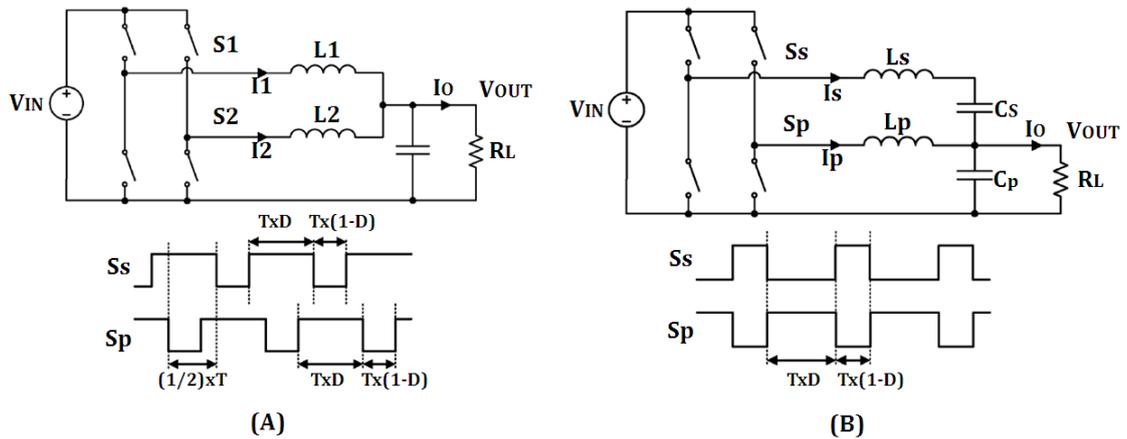


Figure 12. (A) Two-phase standard interleaved topology and timing diagram and (B) stacked interleaved topology and timing diagram [21].

For fully integrated buck converter implementation, it may meet more disadvantages compared with SCC implementation. First, presently fabricating large inductive elements on-chip in high quality is still hard and it is difficult to achieve high power densities [130]. Additionally, it is a trend to implement multi phase buck converter on chip, which may required multiple inductive elements, to reduce output voltage ripple range [124]. This may cause large area due to several inductors employed for one converter. Besides, small inductive element for each phase may reduce power delivery efficiency [131]. Second, normally both inductive and capacitive (for decoupling) elements are needed for buck converter based power delivery systems [132], [133]. However fabricating inductive and capacitive elements may require different materials and technologies. This may increase design and fabrication complexities. Compared with SCC based power delivery systems, only capacitive elements are required.

3.2.2 Switched Capacitor DC/DC Convertor (SCC)

In recent years, technology of on-chip capacitors is developed rapidly. This leads prevalent use in *Radio Frequency (RF)* circuits and mixed-signal integrated

circuits [134] [135]. Lots of researches aim at increasing on-chip capacitor dielectric constants (k) and decreasing leakage current [136] [137]. Among these designs, ***Metal Insulator Metal (MIM)*** capacitors may be the most popular choices [138]. It has been reported that its unit capacitance can be as high as $11.2 \text{ fF}/\mu\text{m}^2$ [139] which well meets the requirement in 2018 set by ***International Technology Roadmap for Semiconductors (ITRS)*** [140]. In [141], the MIM capacitor design achieves a satisfactory leakage current level and capacitance level of $14.6 \text{ fF}/\mu\text{m}^2$ that even have meet the ITRS requirement set for 2020.

The encouraging progress in on-chip capacitor integration drives many recent attempts in on-chip SCC designs. Incorporating the high performance capacitors in [142], both step-down and step-up SCC designs in 130 nm CMOS Technology are able to achieve high power efficiency (both above 80%). Additionally, the high performance capacitors bring SCC designs into a realm using more advanced integration technologies. A SCC with five fixed conversion ratios implemented with 65 nm Technology achieving above 75% efficiency while delivering from $10 \mu\text{W}$ to $250 \mu\text{W}$ of load power is presented in [143]. A SCC with one conversion ratio delivering sub-1 V power supply with efficiency as high as 69% and load current between $100 \mu\text{A}$ and 8 mA is implemented in 45 nm Technology [16]. A SCC fully integrated with 32 nm Technology is capable of achieving high efficiency (81%) with high power density ($0.55 \text{ W}/\text{mm}^2$) while supporting a wide range of output voltage levels using three step-down conversion ratios [17].

For SCC voltage regulation methods, except employing fixed conversion ratios that may limit the SCC output voltage levels, Fibonacci and binary methods are also used for SCC design in [144] [145]. The Fibonacci binary SCC is able to deliver multiple target voltages that may effectively achieve high capacitor charge efficiency [146]. However, due to complexity and high overhead of control, the methods are not prevalently used in on-chip SCC designs.

- **SCC with Fixed Conversion Topologies**

In [147], a fully integrated SCC is designed to have four conversion ratios that enable the SCC to regulate output power with a wide voltage range from 0.3 V to 1.1 V , drawing input power from a 1.2 V stable power supply.

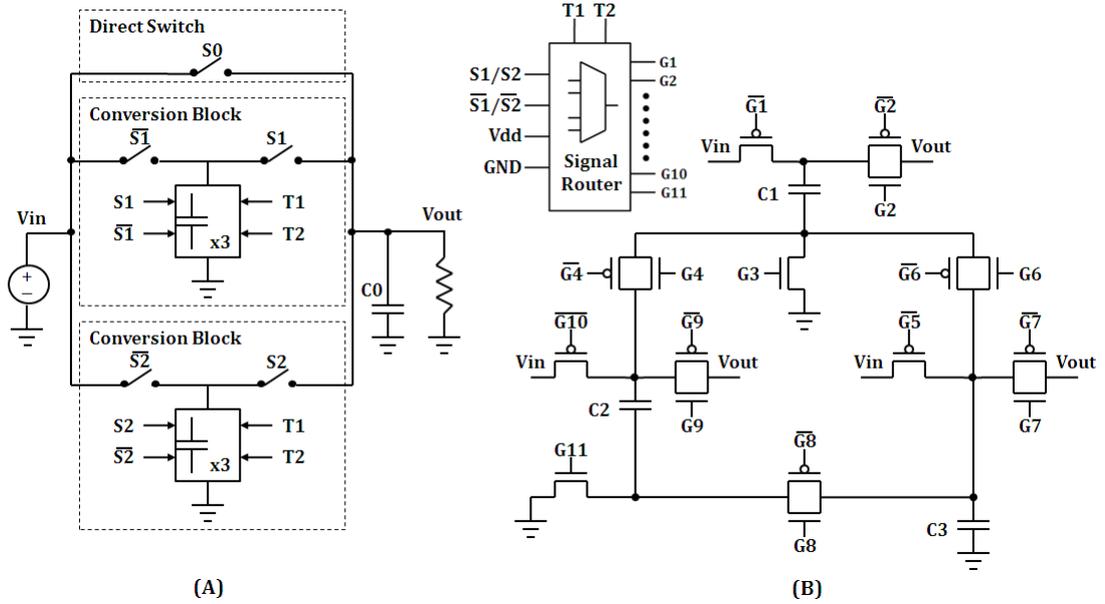


Figure 13. (A) Simplified architecture of SCC circuit and (B) switches and capacitors inside conversion block and signal router [147].

Figure 13 (A) provides an overview of the SCC circuit. It contains one direct switch and two conversion blocks. The direct switch is implemented by using a P-type CMOS transistor and is controlled by signal S0. Two conversion blocks are controlled by signals S1 and S2 respectively. S1 and S2 are not only employed to control the input and output switches, but also to control switching actions performed inside the conversion blocks. Each conversion block has three switched capacitors with the same value. C0 is an output capacitor connected to the load. In [147] the total capacitance value of each conversion block is three times the value of C0. T1 and T2 are two inputs used to preset one of four different conversion ratios (1/1, 2/3, 1/2 and 1/3) to implement different step-down conversions.

The conversion block contains a signal router and three capacitors connected with different types of switches shown in Figure 13 (B). The signal router is used to generate the control signals for the conversion block. All control signals from G1 to G11 are generated by the signal router. After one of the four conversion ratios is preset by T1 and T2, the signal router generates those control signals based on the values of S1 and S2. The signal router also needs a stable Vdd.

Different combinations of open and closed positions for the switches result in the four different capacitor connection topologies shown in Figure 14, in which M represents the conversion ratio (1/1, 2/3, 1/2 and 1/3). Switching does not

change the total energy stored in the capacitors but the total value of the capacitors is changed. Switching thus changes the voltage conversion ratio according to $E = \frac{1}{2}CV^2$.

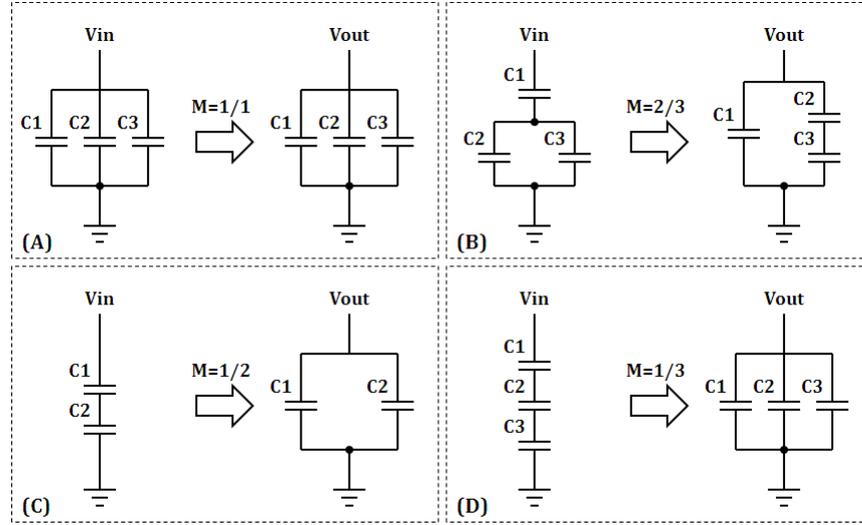


Figure 14. Capacitor connection topologies for the different conversion ratios (M represents the conversion ratio) [147].

During the power delivery process, if the capacitor connection topology $M=1/1$ shown in Figure 14 (A) is used by the SCC, it will achieve highest power delivery efficiency. And the capacitor connection topology $M=1/3$ shown in (D) will cause the SCC to have the lowest power delivery efficiency [148].

Figure 15 presents the control signal waveforms of the asynchronous controller incorporating the dual threshold comparator. V_A and V_B are two signals generated by the comparator and are sent to the inputs of the controller. Threshold V_{Aref} is set to $V_{ref} + 0.05 V$, and threshold V_{Bref} is set to $V_{ref} - 0.05 V$.

In Figure 15 (A) when the SCC circuit is in energy accumulation and V_{out} is below V_{Bref} , the controller keeps (S_0, S_1, S_2) at $(1, 0, 0)$ to maintain the direct switch on to charge C_0 and the capacitors in the two conversion blocks as well. When V_{out} has already reached V_{Aref} and the required output voltage level is achieved, both V_A and V_B are set to “1” by the comparator. Meanwhile, the controller switches the direct switches off by setting (S_0, S_1, S_2) to $(0, 0, 0)$. Due to system latency, an overshoot is inevitable after switching off the direct switch. Because of the pull-down effect from the load, V_{out} falls below V_{Aref} shortly. Then

the controller sets $S1$ to “1” immediately. Therefore the conversion block controlled by $S1$ performs capacitor switchings according the preset conversion ratio and provides power supply to load.

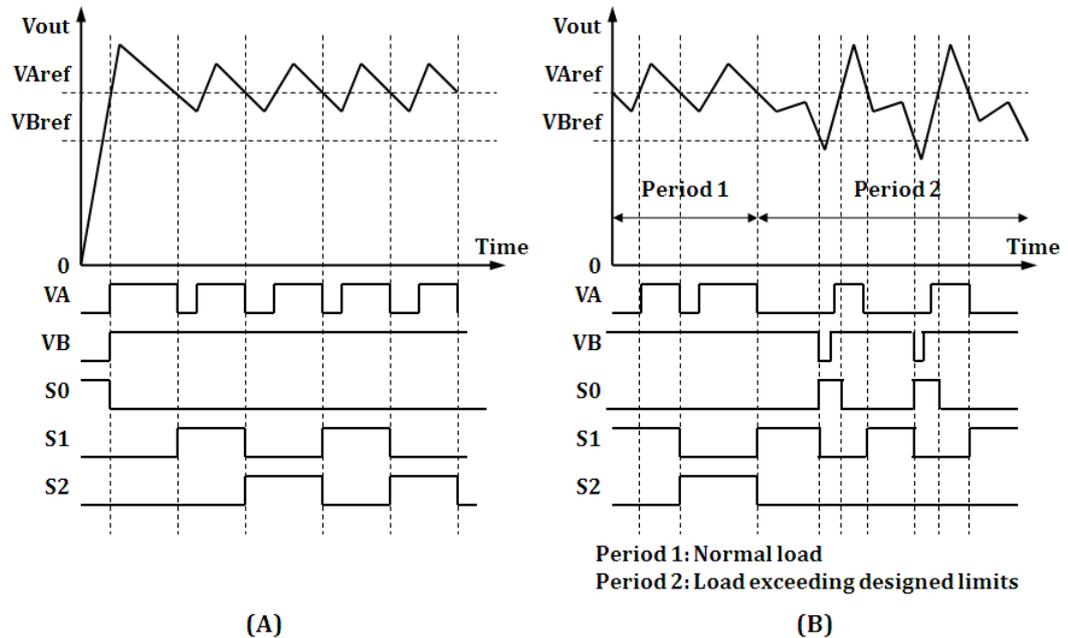


Figure 15. Timing diagram when SCC works under: (A) normal load and (B) load exceeding design limit [147].

If the load is not too heavy, once the conversion block starts to power the load, V_{out} should rise beyond V_{Aref} again. Then, V_{out} has to fall down and across V_{Aref} after the energy stored in the conversion block is expended enough. Now the controller sets $(S0, S1, S2)$ to $(0, 0, 1)$, switching the load to the other fully charged conversion block controlled by $S2$ and the conversion block controlled by $S1$ is connected to the source to be charged for the next round. Then, these two conversion blocks begin to power the load alternately and $S0$ is always kept to “0”.

However, if the load is too heavy and exceeds the designed limit, the controller will take different reaction to try maintaining the V_{out} at a required voltage level as long as the power supply is sufficient, shown in Figure 15 (B). In period 1, when the load is not heavy, the conversion blocks can power the load alternately. But in period 2, the load is very heavy. The fully charged conversion block still cannot raise V_{out} beyond V_{Aref} and V_{out} falls down below V_{Bref} . In this case, the controller sets $(S0, S1, S2)$ to $(1, 0, 0)$ to let the load to be powered directly by the

source and at the same time the source also charges the two conversion blocks. In this case, the SCC tries its best to keep V_{out} above V_{Bref} .

3.3 On-Chip Voltage Sensing

In *Analogue Mixed Signal (AMS)* SoC designs, analogue and digital components are always employed. In the designs, there may be more than one V_{dd} domain existing on the chip. Additionally, modern SoC designs always calls DVFS techniques to gain advantages [149]. Furthermore, for wireless sensor network and biomedical applications, EH techniques are becoming more and more popular. In such system, unpredictable energy source may have large impact on the stability of V_{dd} levels [150]. Therefore V_{dd} levels in each domain on the chip may not be considered as static parameters any more. These parameters may need be sensed and adjusted to achieve optimization in terms of energy consumption [151] [152], power delivery efficiency [153] [154], die temperature [155] [156], and system performance (e.g. mobile devices and wireless sensor networks [157] [158]).

3.3.1 Traditional ADC and comparator

In [159], a traditional high speed ADC is introduced and the design employs resistor based voltage reference, and traditional comparators, shown in **Figure 16** (A). In this work, the fundamental trade-off between speed-power-accuracy and the impact of technology scaling on this trade-off is examined. It clearly shows that without extra modifications to the design or technology, power consumption will become a problem for future high-speed ADCs. Especially for very deep submicron technologies power will go up in order to achieve the same specifications as nowadays. This can limit the integration of digital and analogue electronics.

For traditional ADCs, they are based on a chain of comparators, such as the high precision process-invariant voltage comparator introduced in [160] shown in **Figure 16** (B). These comparators need voltage references that are normally generated by using resistor or transistor ladders [161] [162]. Additionally, these comparators are usually based on current mirror and OTA [163]. Therefore generating various voltage references for comparators and intrinsic structure of comparators may cause a large amount of energy consumption.

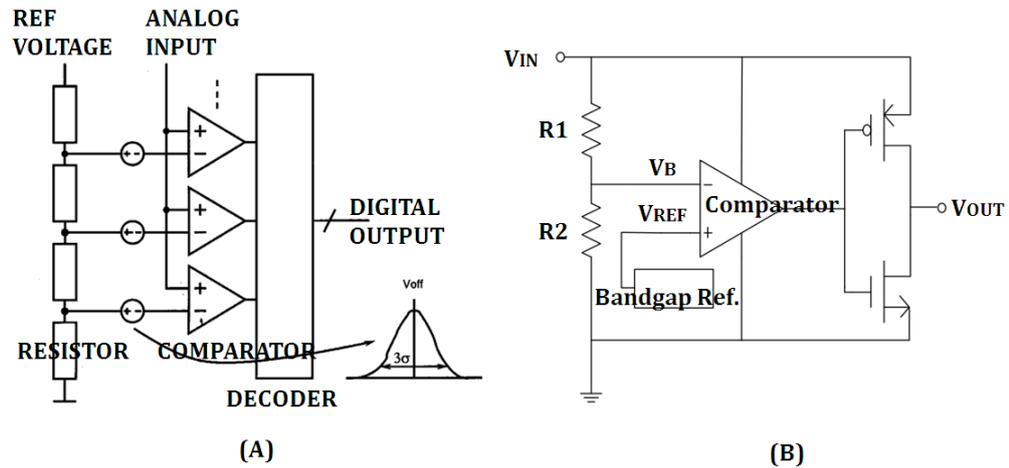


Figure 16. Comparators used for voltage sensing: (A) high speed CMOS ADC [159] and (B) voltage sensor architecture [160].

Unfortunately, these characteristics of traditional ADCs may make energy consumption of systems even worse especially for EH systems where harvested power is very limited and unstable. Besides, traditional ADCs trend to achieve very high voltage conversion accuracy and have to do trade-off with conversion time. However, in EH systems, very high voltage conversion accuracy might not be necessary as high accuracy normally means large energy consumption and long conversion time [164] [165].

3.3.2 Power-on-Reset Circuit

In [166], systematic comparative investigations about **Power-on-Reset (POR)** circuits are presented and concluded. Besides, threshold voltage sensing circuits: **Voltage Level (VL)** and **Charge Capacitor (CC)** are employed as voltage sensors working for **Radio Frequency Identification (RFID)** systems.

The VL circuit is shown in Figure 17 (A). The ladder (M1–M10) biases the transistor M12. When V_{IN} achieves the upper threshold voltage (V_{up}), M12 conducts and the Enable Signal is set to HIGH. The circuit is implemented entirely with MOS devices.

The CC circuit is shown in Figure 17 (B). The capacitor C delays the activation of the Enable Signal. The output stage, formed by M6–M12, sets to HIGH the Enable Signal when the transistor M7 is switched on. M7 conducts only when capacitor C is charged enough. Because C is charged via transistors M1–M4, the dimensions of

these transistors determine the charging time and V_{up} rise time. When the voltage in V_{IN} decreases, C is discharged through M_5 . In this way, the minimum required time between two consecutive Enable signals is reduced.

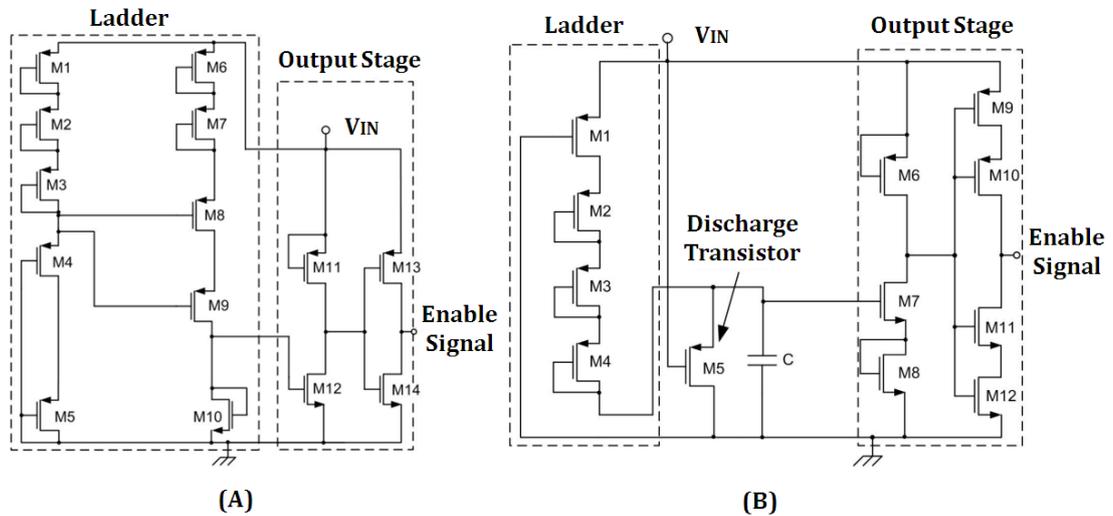


Figure 17. Adjustable voltage sensor: (A) Voltage Levels and (B) Charge Capacitor [166].

Compared with normal ADCs, threshold based voltage sensing circuits introduced above may be more economic in energy consumption and faster in A/D conversion. The threshold voltage sensing circuit employs its intrinsic threshold to sense a fixed voltage level and generate an Enable signal. Threshold voltage of the circuit can be preset by adjusting width and length of transistors or size of capacitors inside the circuit.

Traditionally, threshold voltage sensing techniques are prevalently employed in POR applications in single voltage sensing for circuit initialization or system recovering but seldom being employed in multiple voltage sensing purposes. On the other hand, the threshold voltage sensing techniques mentioned above may only be good at sensing rising voltage level. When a voltage level is raised above a threshold of the POR circuit, the POR or Enable signal will be generated immediately. But when the voltage level is decreased below the threshold, the signal will be pulled down to GND very slowly.

The VL circuit in, due to use resistor or transistor ladders, might have a slow response in voltage sensing. The CC circuit in, due to use a small on-chip capacitor, might have “memory effect” existing during each voltage sensing period, as the charge accumulated in the capacitor may not be removed immediately before

starting next voltage sensing. In this case, these POR circuits may not be good candidates for sensing voltage in falling process.

3.3.3 Reference-Free Voltage Sensing

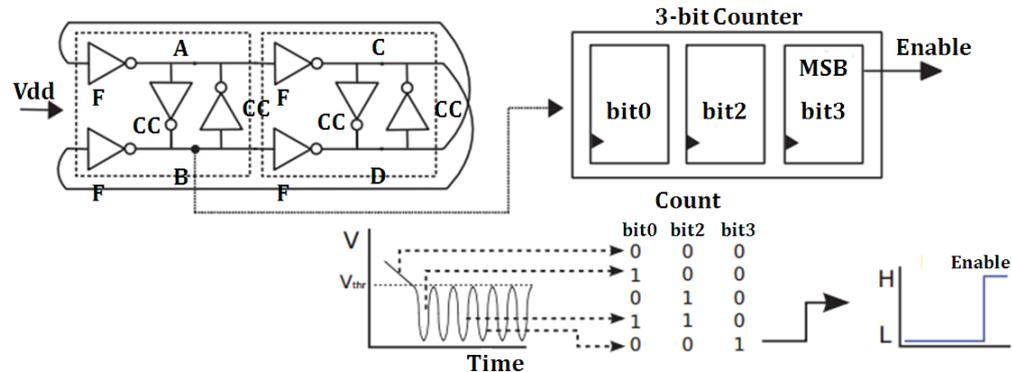


Figure 18. Configuration for the detection of the onset of the oscillation [167].

In [167], a voltage sensing method based on the dependence of the operating mode of a circuit on the supply voltage is proposed. The method is applied on an even stage ring oscillating and latching modes at certain V_{dd} levels, shown in **Figure 18**. When the V_{dd} of the ring oscillator drops below a certain level, the circuit starts oscillation. On the other hand, when the V_{dd} rises above the level, the oscillation will stop. A 3-bit counter is connected to an internal node of the ring oscillator and is preset to 000. The counter waits for the oscillating signal which acts as the clock for the counting. The **Most Significant Bit (MSB)** of the counter serves as the Enable signal that informs the rest of the circuit about the change in V_{dd} level.

In this work, only incorporating digital components without any resistors and capacitor greatly reduces circuit area and simplifies integration. On the other hand, adjusting size of transistors inside inverters can effectively tune switching threshold voltage. Therefore, an external voltage reference is not necessary. Unfortunately the ring oscillator based reference-free voltage sensor may only be used for falling voltage level sensing.

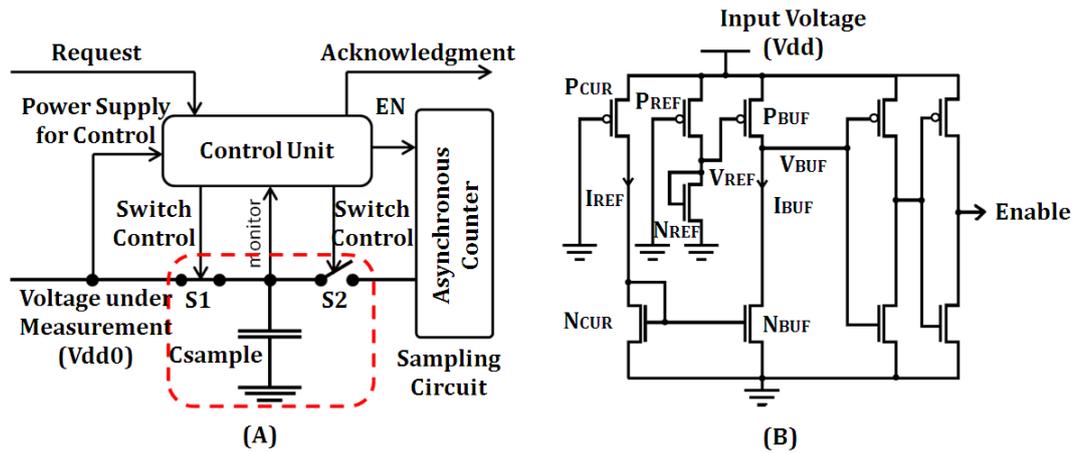


Figure 19. (A) General architecture of the reference-free voltage sensor [168] and (B) schematic of a dual-threshold POR circuit [169].

In [168], a general architecture of a reference-free voltage sensor is shown in Figure 19 (A). A small on-chip capacitor C_{sample} is used as an energy storage component. The capacitor charge and discharge operation is organized by an asynchronous control unit using S1 and S2. An asynchronous toggle counter is used as a ruler. When sensing round starts, S1 will be switched on and S2 switched off. Thus the capacitor will be charged by V_{dd0} and the counter is disconnected from the capacitor. After the completion of sensing, the capacitor is disconnected from V_{dd0} (S1 off) and will be connected to the counter (S2 on) to prepare A/D conversion.

A reference generator [169] (inside the control unit) having two thresholds also powered by the capacitor will enable the counter to start computation (A/D conversion) using the higher threshold. When the voltage level at the capacitor reaches the lower threshold of the reference generator, the computation performed by the counter will be stopped immediately.

The key feature of this method is that the counter is entirely powered by the energy of the charge obtained from the voltage it measures, and the speed at which it works reflects this voltage. Additionally, in the work, different sample capacitor values are investigated regarding the A/D conversion precision. For less energy consumption a smaller capacitor can be used at the cost of lower precision of the output code.

For the reference generator, a dual-threshold POR circuit is employed and its modified circuit schematic is presented in Figure 19 (B). In the design, transistors P_{REF} and N_{REF} form a voltage divider and give a reference V_{REF}. V_{REF} is feed to the gate of transistor P_{BUF}. N_{BUF} sources current from P_{BUF}. This current is copied from the P_{CUR} and N_{CUR} current source. Voltage V_{BUF} will be grounded while V_{REF} is below the threshold voltage of P_{BUF}. When V_{REF} is above the threshold voltage of P_{BUF}, V_{BUF} is copying the supply V_{dd}. P_{REF} and N_{REF} control the point at which the node V_{BUF} has activity. Two inverters are used to sharpen the transition of the V_{BUF} and generate an Enable signal.

Compared with traditional ADCs, the reference-free voltage sensor in [168] may save more energy as it does not need generating voltage references and it incorporate an asynchronous self-timed counter to instead of conventional comparators for A/D conversion. However, the reference-free voltage sensor may need longer time to achieve high A/D conversion precision, as higher precision requires using higher capacitor value for sampling and the counter needs longer period to complete computation (A/D conversion).

Chapter 4

Switched Capacitor DC/DC Converter Investigation

4.1 Introduction

“Next Generation Energy-Harvesting Electronics: A Holistic Approach” is an university and industry cooperative project (Newcastle University, Southampton University, Imperial College, Bristol University, DIODES, ARM, MENTOR GRAPHICS, and DIALOG SEMICONDUCTOR) sponsored by *Engineering and Physical Sciences Research Council (EPSRC)* [170].

Research of the project concentrates on developing ultra energy-efficient electronic systems for emerging applications including mobile digital health, and autonomous wireless monitoring in environmental and industrial settings. There are three main research themes: Micro-Generator Design (EH and *Micro-Electro-Mechanical Systems (MEMS)* processing methods), Computational Circuits (low-power embedded computing systems), and System Optimisation (*Electronic Design Automation (EDA)*).

The thesis author as one of the project participators mainly focuses on providing on-chip power delivery solutions between EH micro-generator and computational circuits for miniaturised low-power systems with smart task & power scheduling ability.

In order to understand problems existing in power delivery path between harvesters and loads in micro-scale systems and find opportunities to develop a new power delivery method to solve the problems, an elementary on-chip power delivery investigation was completed. An example of a typical SCC used for powering biomedical implantable electronic devices [147] was studied by hardware implementation. In order to investigate *Dynamic Voltage and*

Frequency Scaling (DVFS) techniques [171], the design of SCC circuit was also optimized to be able to generate six different output voltage levels using four conversion ratios to better meet voltage scaling requirements from the load.

In the Holistic Energy Harvesting project, the SCC hardware is also employed to meet a requirement of asynchronous chip verification and demonstration. Switched capacitor based variable V_{dd} powered asynchronous chip demonstration was successfully presented in the project advisory board meeting in Southampton University on 2nd of July, 2012 (shown in Appendix A, Figure 76 and Figure 77).

4.2 SCC Investigation Methodology

The DC/DC conversion unit investigation is based on an SCC found in [147] and introduced in Section 3.2.2. For the investigation, hardware implementation is necessary for studying and understanding power distribution inside the SCC during power delivery process.

The SCC is required to have ability to generate various output voltage levels for the load. It is also required to have a quick output voltage sensing speed and capacitor switching response to compensate input power variation (assuming harvested energy may be largely influenced by environment and it may be not stable) and to meet requirement of workload weight change (assuming workload weight may be changed due to different tasks).

On the other hand, in the Holistic Energy Harvesting project, an asynchronous self-timed *Static Random Access Memory (SRAM)* chip (Appendix A, Figure 78) is manufactured for an EH system and it is waiting for chip function verification and the advisory board meeting demonstration. In order to complete the chip verification and demonstration, the SCC hardware is employed as a PDU, which cooperates with a host *Personal Computer (PC)* used as a *User Guider Interface (UGI)*, to regulating controllable power for the SRAM chip.

4.2.1 SCC Based Asynchronous SRAM Chip Verification System

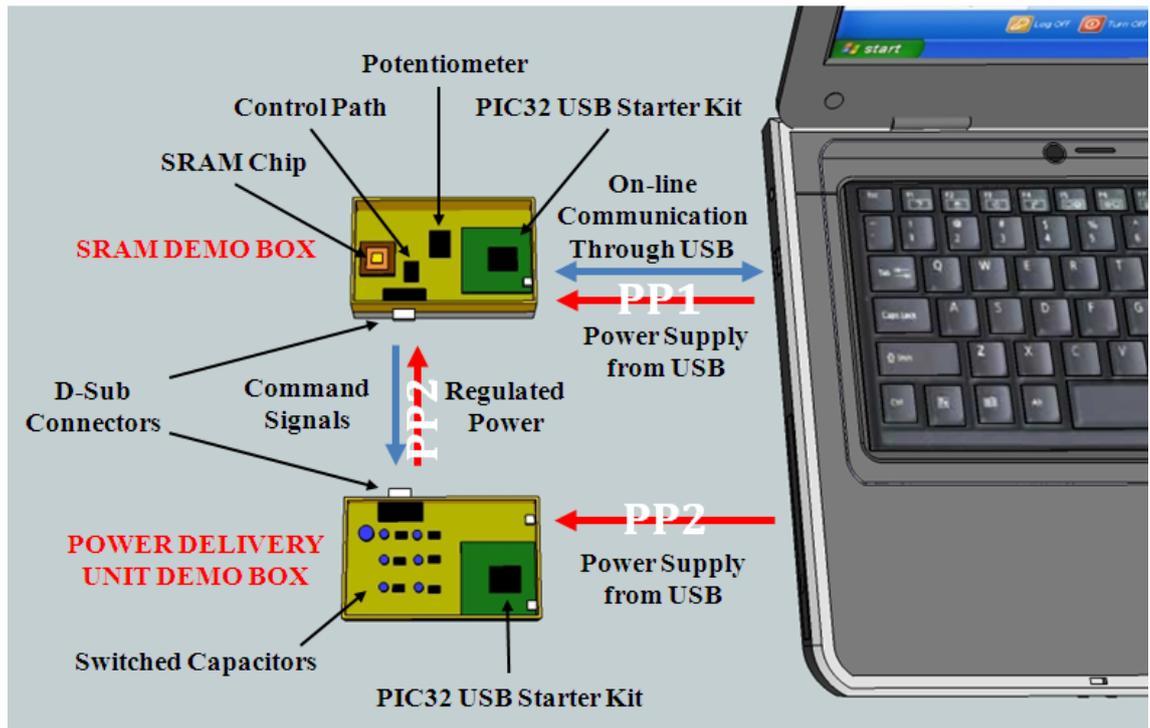


Figure 20. Portable, user-friendly SCC based PDU investigation system diagram.

The entire portable (small size and box protected) user-friendly (Microchip MPLAB interface) SCC based asynchronous SRAM chip verification system diagram is shown in Figure 20. Circuit boards inside the PDU demo box and SRAM demo box are manufactured based on **Printed Circuit Board (PCB)** technology. For the SCC based PDU board, it mainly contains a microcontroller (PIC32 USB Starter Kit) [172], analogue electronic switch chips, capacitors, and a power and signal female connector. For the asynchronous self-timed SRAM board, it mainly contains a microcontroller (the same as that of PDU board), a digital potentiometer with non-volatile memory (MCP4161) [173], a control path, a SRAM chip and a power and signal male connector.

The verification system is powered by a host PC using its USB ports, which provide 5 V (500 mA to 900 mA) power supply [174]. In the system, there are two **Power Paths (PP)** shown in Figure 20. The PP1 is from the host PC USB port to the SRAM board. On the board, the potentiometer is located in the PP before the load (SRAM chip). Through programming, the potentiometer can adjust output voltage level in 256 steps (internal resistance adjustment resolution) for the SRAM chip.

The PP1 is employed for the SRAM chip individual verification and demonstration. However, experiment data of the SRAM chip obtained by using the PP1 can be used as comparative study references for the investigation of the SCC that is located in PP2.

The PP2 is from the host PC USB port to the SRAM board via the PDU board. The input power from the USB port will be regulated by using the switched capacitor circuit controlled by the PDU microcontroller. The regulated power will be delivered to the SRAM chip from the PDU board via D-Sub Connectors that are employed for both power and signal connections.

4.2.2 Microcontroller Application

The microcontroller on the SRAM board is used to implement on-line communication with the host PC through a USB cable by using the MPLAB on-line debugging function [176], shown in Figure 20. Therefore, users can easily use the host PC to access the SRAM via the microcontroller on the SRAM board. Testing data can be written into the SRAM by using the host PC keyboard and the stored data can be read out and shown on the host PC screen.

On the other hand, the microcontroller on the SRAM board can be considered as a master, which can send command to the PDU microcontroller (used as a slave). Therefore, the user can also use the host PC to control PDU to generate various V_{dd} for the SRAM during writing and reading process.

4.2.3 Generating Six Various Output Voltage Levels

Since the SRAM chip is fabricated in UMC 90nm Technology, voltage level between 1 V and 1.2 V is considered its normal V_{dd} range [111]. However, the voltage level from the USB port of the host PC (5 V) is much higher than that needed by the SRAM chip. In this case, the PDU demo board is employed to regulate the input power from the USB port and deliver proper output power for the SRAM chip.

Table III. SCC generates six different output voltage levels for fine voltage regulation.

Input Power (V)	Conversion Ratio (M)	Output Voltage (V)
1.8 (from Regulator 1)	2/3	1.2

	1/2	0.9
	1/3	0.6
1.2 (from Regulator 2)	1/1	1.1
	2/3	0.8
	1/3	0.4

On the PDU board, the 5 V input power will be regulated by two voltage regulators for generating 1.8 V or 1.2 V power. Then the coarsely regulated power (1.8 V or 1.2 V) will be delivered to the SCC manufactured on the PDU board. Since the SCC has four conversion ratios (1/1, 2/3, 1/2 and 1/3), by exclusively enabling one of these two voltage regulators (for 1.8 V or 1.2 V), the SCC is able to generate six different output voltage levels (1.2 V, 1.1 V, 0.9 V, 0.8 V, 0.6 V and 0.4 V) to implement fine voltage regulation for the SRAM chip.

Table III shows the details of employing the SCC to implement fine voltage regulation drawing power from either Regulator 1 (1.8 V) or Regulator 2 (1.2 V).

4.2.4 D-Sub Connectors for Power and Signal Connection

In order to increase demo portability and convenience, the SRAM and PDU boards will be located in semi-transparent plastic boxes (called Fibox [175]) with signal and power connectors stretching out through the wall of the boxes. Two D-Sub connectors are used for sending command (requiring a fine regulated power) from the SRAM board to the PDU board, and delivering required power from the PDU board to the SRAM board. By using this kind of connection, the complexity of power and signal connection interface between two boards is significantly decreased. Figure 21 provides pin specification of the female D-sub connector located on the PDU board.

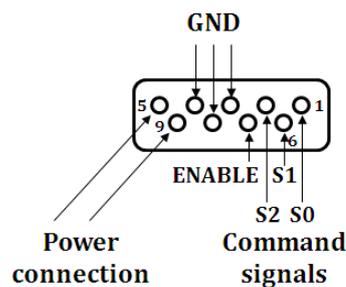


Figure 21. Pin specification of female D-sub connector on PDU board.

For requiring a fine regulated power from the PDU board, the SRAM microcontroller will first preset S0, S1 and S2 (PIN 1, 6 and 2) whose values are used to choose one of six output voltage levels, then toggles ENABLE (pin 7) once to trigger the PDU to deliver fine regulated power with the required voltage level via pin 5 and 9 to the SRAM board. Pin 3, 8 and 4 are used for GND connection.

4.3 Hardware Implementation

To achieve the SCC hardware implementation, several points need to be considered, such as 1) command synchronization between two microcontrollers located on SRAM board and PDU board respectively, 2) power and signal connection between PDU board and its microcontroller, 3) voltage regulating for powering electronic devices manufactured on the PDU board, 4) PDU circuit testability, 5) component locating and wire routing to fit the PDU board into the demo box, and 6) demo box processing and so on.

4.3.1 Power Delivery Unit Circuit Schematic

Figure 22 shows the circuit schematic of the PDU. A nine-pin D-Sub connector (Block 12) is employed to connect command and fine regulated power between the SRAM and PDU boards.

Block 1 and Block 2 are pull-up resistors and slide switches respectively. The slide switches are used to manually control the output voltage level of the PDU for circuit testing purposes. Block 13 contains four jumpers, which are used to choose either manual control using slide switches, or external control receiving the signal from SRAM board.

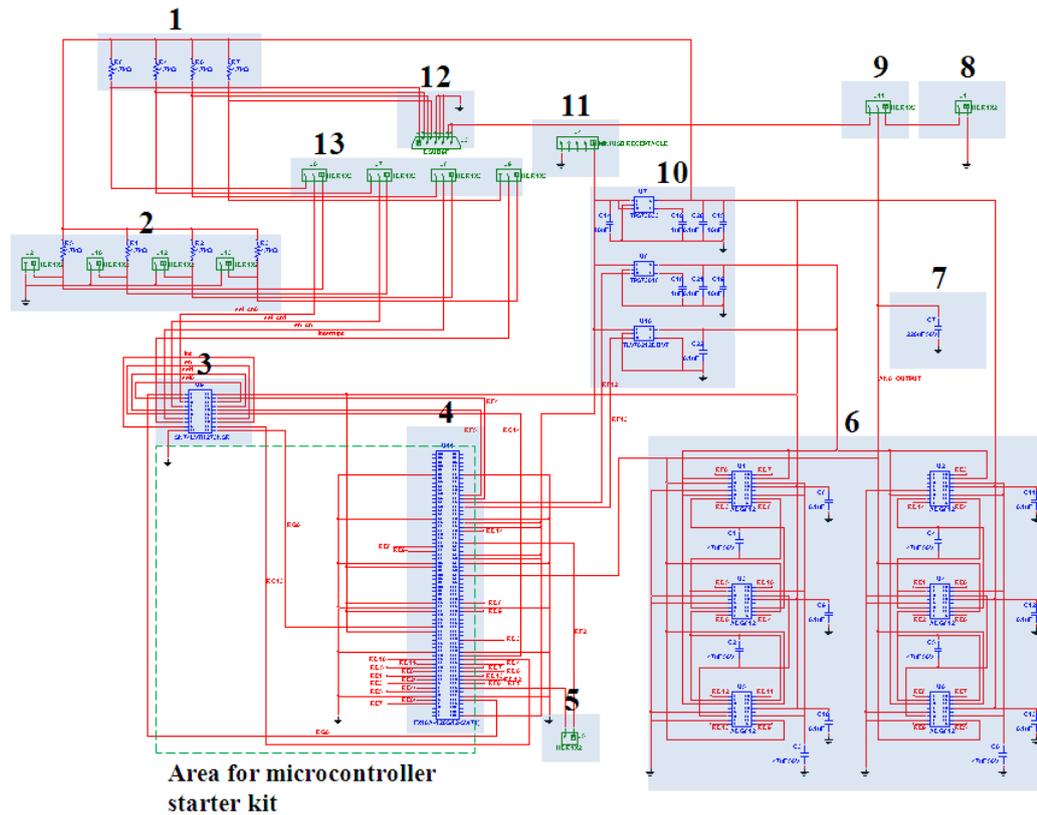


Figure 22. Power delivery unit circuit schematic.

Block 3 is an eight-channel *D-type flip flop (DFF)* chip (SN74LVTH273NSR). It is used as a synchronizer to prevent the PDU from unexpected operations caused by mismatched clocks generated from two microcontrollers of the SRAM board and PDU board respectively. The driving clock of the DFF is generated by the PDU microcontroller using SPI function [177]. The microcontroller is connected to the PDU board by using a kit connector (Block 4) for VDD, GND and switched capacitor circuit control signal connection. Block 5 is a PCB terminal for checking working status of the microcontroller ADC component.

Block 11 is a MINI USB TYPE-B receptacle used for drawing input power from a host PC USB port. Then the input power will be regulated to three voltage levels by using three voltage regulators (3.3 V, 1.8 V and 1.2 V shown in Block 10). 3.3 V power is for all the electronic devices on the PDU board and the microcontroller. 1.8 V and 1.2 V power are for the input of SCC.

Block 6 contains six electronic switch chips (ADG812) and six switched capacitors used for implementing power delivery. The control signals of the switches are sent from the microcontroller through a connector Block 4. Block 7 is

an output capacitor to filter output voltage ripples. Block 8 is a PCB terminal used as a testing output to check the PDU working status. Block 9 is a jumper used to choose the regulated power going to either Block 12 for the SRAM board or going to Block 8 for a RC testing circuit.

4.4 Microcontroller Programming

For implementing SCC control, a *Finite State Machine (FSM)* with six states is used [147]. An ADC component of the microcontroller located on the PDU board is employed for the PDU output voltage sensing. The fastest data conversion speed of the ADC component is approximately 1 MHz. *(C language program codes for the microcontroller of the PDU are copied into a CD attached to the thesis.)*

There are two sensing control problems needing to be solved in terms of 1) control of the PDU microcontroller sensing the four-bit command sent from the SRAM microcontroller, and 2) control of the ADC sensing the PDU output voltage level. To solve the problems, both polling and interrupt methods can be used. However, different sensing methods will cause different ADC sampling and PDU response performance, when 1) input power changes; 2) load weight changes, and 3) required output voltage level changes.

4.4.1 Polling Method for Both Command and ADC Sensing

Figure 23 shows a concise program flowchart for SCC control by using a polling method for both command and PDU output voltage level sensing. After configuring the microcontroller, the program flow jumps into a loop.

The microcontroller will sense the command for setting an output voltage level required by the SRAM board. Then it will wait for completion of the ADC conversion. After receiving *End of Conversion (EoC)* from the ADC, the converted data will be read out from an ADC buffer. Then according to the converted data, corresponding control signals will be generated for the switched capacitor circuit. The detailed program flowcharts for the SCC control using polling method for both command and ADC sensing are shown in Appendix B, **Figure 85** and **Figure 86**.

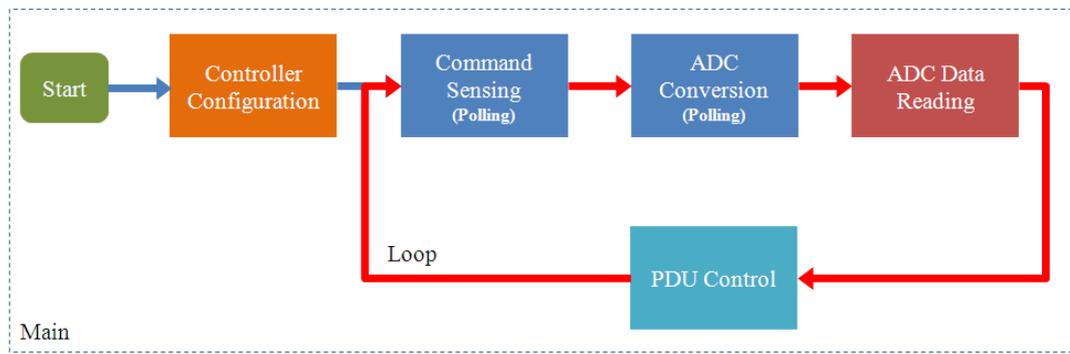


Figure 23. Concise program flowchart for SCC control (polling method for both command and ADC sensing).

4.4.2 Interrupt Method for Both Command and ADC Sensing

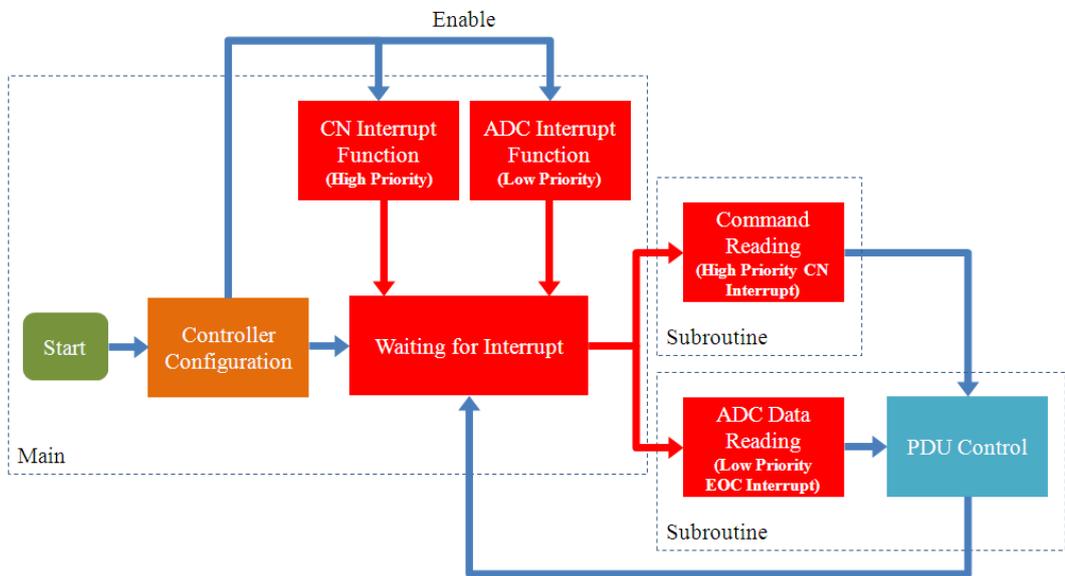


Figure 24. Concise program flowchart for SCC control (interrupt method for both command and ADC sensing).

Figure 24 presents a concise program flowchart for SCC control using interrupts for both command and PDU output voltage level sensing. After configuring the microcontroller, the *Charge Notice (CN)* and ADC interrupt functions will be enabled.

When one of the interrupts is fired, the program flow will jump into the corresponding interrupt subroutine. Then control signals will be generated. If these two interrupts come at the same time, the CN interrupt with higher priority will be processed first. After completing the higher priority interrupt, the lower priority interrupt will be processed. The detailed program flowcharts for the SCC

control are shown in Appendix B, **Figure 87**, **Figure 88**, **Figure 89**, and **Figure 90**.

4.4.3 *Interrupt Mode for Command Sensing and Polling Mode for ADC Sensing*

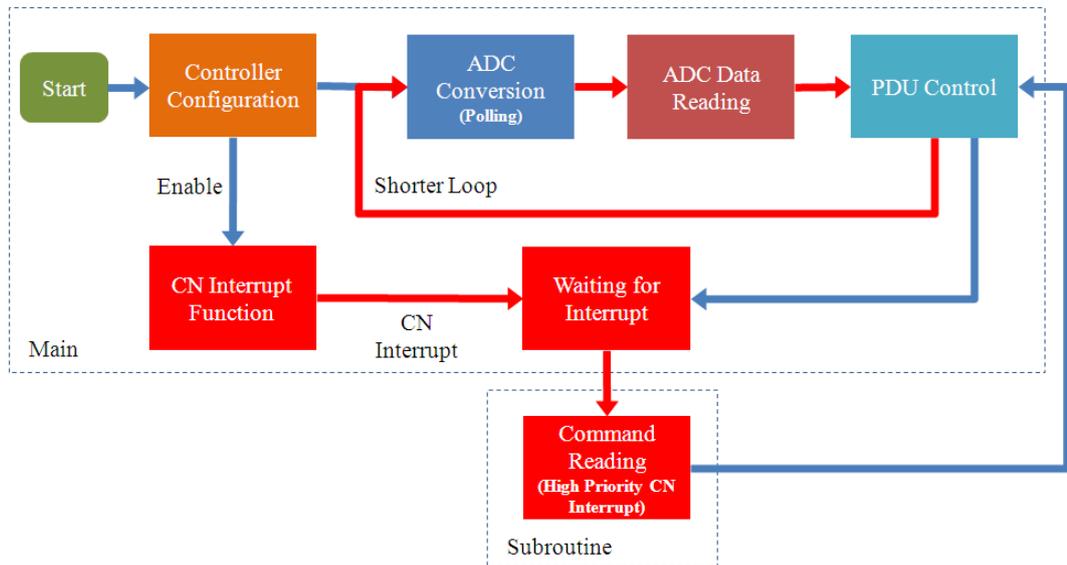


Figure 25. Concise program flowchart for SCC control (interrupt method for command sensing and polling method for ADC sensing).

Figure 25 describes a concise program flowchart for SCC control by using an interrupt method for command sensing and using a polling method for output voltage level sensing. After configuring the microcontroller, the CN interrupt function will be enabled.

At the same time, the program flow will jump into a loop, where the microcontroller will wait for completion of ADC conversion. When EoC is generated, the converted data will be read out. According to the data, corresponding control signals will be generated. This loop is shorter than the loop presented in **Figure 23**. During the power delivery process, if the CN interrupt is fired, the PDU control signal will be directly generated accordingly. The detailed program flowcharts for the SCC control are shown in Appendix B, **Figure 91**, **Figure 92**, and **Figure 93**.

4.4.4 *PDU Microcontroller Sampling Performance*

Table IV shows the PDU microcontroller sampling performance based on three different sampling methods. For using interrupt mode for both command sensing and ADC sensing, the system gets longest sampling time and only achieves 571

samples per ms. For using interrupt mode for command sensing and using polling mode for ADC sensing, the system gets shortest sampling time and can achieve 870 samples per ms. The sampling performance of the system using polling mode for both command sensing and output voltage sensing ranks in the middle.

Table IV. PDU microcontroller sampling performances based on three different methods

Sensing Method		Sampling Performance	
Command	Output Voltage Level	Sampling Time	No. of Samples
Polling	Polling	1.45 us	670/ms
Interrupt	Interrupt	1.75 us	571/ms
Interrupt	Polling	1.15 us	870/ms

From the sampling performance comparison, the method using interrupt mode for command sensing and using polling mode for ADC sensing helps the PDU to achieve fastest sampling performance. It also enables the PDU have fastest power delivery response. Since the SRAM microcontroller does not require changing the PDU output voltage level in a very high frequency, the command sent from the SRAM microcontroller is not changed frequently. Therefore, interrupt method used for the command sensing may be an appropriate way.

On the other hand, for the PDU output voltage sensing, high frequent sampling speed is very important for the PDU to maintain an accurate output voltage level and have a fast response to overcome input power and workload weight changes. Therefore, using polling method for ADC sensing and letting the PDU microcontroller to work in a shorter loop (see Figure 25 compared with Figure 23) may help the PDU to achieve best performance in terms of output voltage level sampling and PDU control response.

4.5 SCC Hardware Investigation and Asynchronous SRAM Chip Verification

For the SCC hardware investigation, an adjustable RC load and an asynchronous self-timed SRAM chip are used separately. For testing with the RC load, the maximum limit of the PDU in power delivery is investigated by continuously increasing RC load weight. For asynchronous SRAM chip verification, the SCC

hardware is not only used to simply generate several stable V_{dd} for the chip, it is also controlled to generate a variable V_{dd} varying in a large voltage range to verify the chip functions.

4.5.1 SCC Hardware Investigated with a RC Load

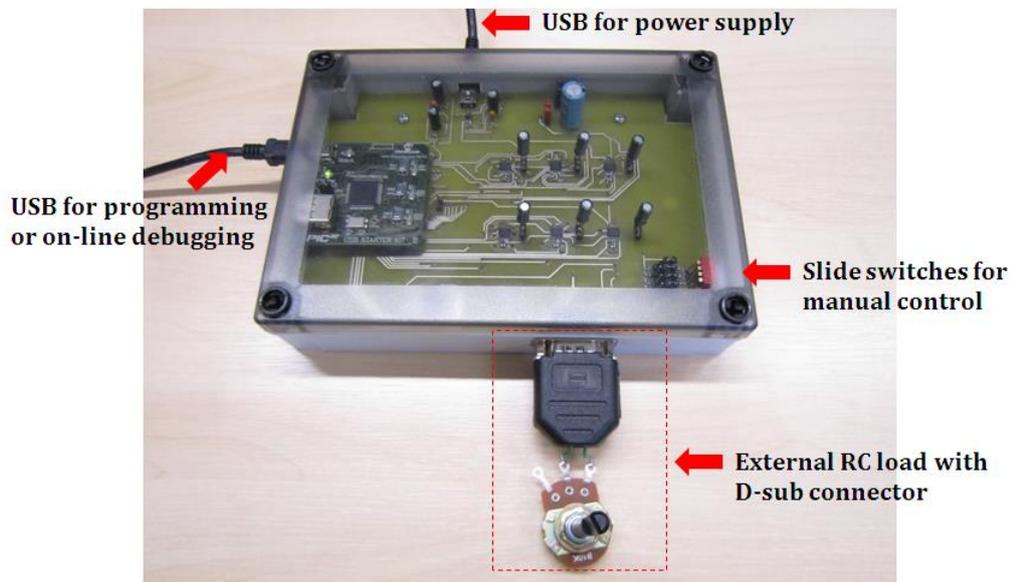


Figure 26. SCC hardware investigated with a RC load.

Figure 26 presents an experiment setting for the SCC hardware investigation using an external adjustable RC load with a D-sub connector. There are two USB receptacles located on the PDU board and the microcontroller starter kit board. One is used to connect power supply from a 5 V host PC USB port. The other is used for microcontroller programming and may be used for on-line debugging by using MPLAB on the host PC. Slide switches are used for PDU manual control to implement power delivery in variable voltage levels. An adjustable resistor and a fixed value capacitor (located inside of the black housing box) are used as an external RC load connected to the PDU demo box via the D-sub connector.

- **Capacitors Used for SCC**

In the investigation, six radial lead electrolytic capacitors (47 uf per each) are used as switched capacitors located in the SCC circuit (See Figure 22, Block 6). One radial lead electrolytic capacitor (220 uf) is used as an output capacitor to filter output voltage ripples (see Figure 22, Block 7). 22 uf radial lead electrolytic capacitors are used to buffer the SCC input power supplied from the host PC USB

port. Besides, 100 nf surface mounted capacitors are used to filter high frequent power noise for Vdd input of electronic devices located on PDU demo board.

4.5.2 Test 1: Deliver 1.2 V to an Adjustable RC Load

An investigation has been done to show SCC hardware performance by delivering 1.2 V power supply to an adjustable RC load. Results are shown in Figure 27. Vout is the voltage level at the output of the PDU. VA and VB are two control signals used to regulate the output voltage level of PDU. During the power delivery process, if the Vout is higher than VBref, VB will be pulled to High by the PDU microcontroller. Otherwise, it is still kept to Low. On the other hand, if the Vout rises further beyond VBref and higher than VAref, VA will be pulled to High (More detailed explanation of the SCC working principle is described in Section 3.2.2.).

In the power delivery process, the SCC tries to maintain Vout close to VAref. VBref can be considered as a deadline. If the Vout drops below the VBref, it means that the load weight exceeds the design limit. In this situation, the microcontroller has to connect the load directly to the input of the SCC to raise the output voltage level. The waveform of Cap Switching presents the capacitor switching frequency performed by the SCC.

In the experiment, the RC load with four different resistances (250 Ohm, 125 Ohm, 75 Ohm and 25 ohm) and fixed capacitance (22 uf) is tested. Diagram (A), (B), and (C) show the SCC working with a normal load (load weight is not beyond the SCC design limit (see Figure 15 (A))). Since the SCC working with a normal load, the Vout is always higher than VBref. Thus, VB is correspondingly pulled to High. On the other hand, since the SCC always tries to maintain Vout close to VAref, the control signal VA is always toggled to implement capacitor switching activities. From (A) to (C), due to decreasing the resistance of the RC load, the capacitor switching frequency has to be increased accordingly. Therefore, the VA toggle frequency is much higher in (C) than that in (A). Thus, the frequency of Cap Switching in (C) is much higher than that in (A).



Figure 27. 1.2 V regulated power delivered to an adjustable RC load.

Diagram (D) shows the SCC working with a load whose weight exceeds the design limit (see Figure 15 (B)). Since the resistance of the RC load is too small, it draws too much current from the SCC. Therefore, it is very hard to maintain V_{out} close to V_{Aref} and the output voltage level drops below V_{Bref} frequently. In this case, V_B has to be frequently toggled leading the output capacitor of SCC being charged frequently by the power supply (input of the SCC). If connecting the output capacitor to the power supply still cannot raise V_{out} close to V_{Aref} , it is considered that the SCC fails to power the RC load.

4.5.3 Test 2: Deliver Various V_{dd} to a Fixed RC Load

Table V shows SCC performance in delivering variable V_{dd} to a fixed RC load (R : 500 Ohm, C : 22 uf). Six voltage levels (1.2 V, 1.1 V, 0.9 V, 0.8 V, 0.6 V, and 0.4 V) are delivered by the SCC with different voltage conversion ratios (M). In the table, the Target V_{out} is an ideal value that the SCC tries to achieve. The Test V_{out} is an actual measured value. In the testing, V_{out} is very close to the High V_{th} (V_{Aref}).

The output current is measured by a multi-meter. To maintain a load working in a higher voltage level, the load draws more current from the SCC.

Table V. Delivery Various V_{dd} to a Fixed RC Load (R: 500 Ohm, C: 22 uf).

Conversion Ratio (M)	Target V _{out} (V)	Test V _{out} (V)	High V _{th} (V _{Aref}) (V)	Low V _{th} (V _{Bref}) (V)	Output Current (mA)
2/3	1.2	1.174	1.18	1.15	2.295
1/1	1.1	1.095	1.08	1.05	2.139
1/2	0.9	0.884	0.88	0.85	1.727
2/3	0.8	0.782	0.78	0.75	1.527
1/3	0.6	0.586	0.58	0.55	1.144
1/3	0.4	0.385	0.38	0.35	0.752

4.5.4 Test 3: Deliver a Variable V_{dd} to an Asynchronous Chip

Figure 28 shows the SCC based PDU powering the asynchronous self-timed SRAM chip. There are two USB cables used in the test. One is used to supply 5 V power for the PDU from the host PC. The other is used for on-line communication between the SRAM microcontroller and the host PC. The PDU regulates the input power and delivers it to the SRAM chip with six adjustable output voltage levels. The D-Sub connector connects the power supply and the command communication between the PDU demo box and SRAM demo box.

In the experiment, the SCC is not only used to generate stable V_{dd} with six various voltage levels, it is also employed to provide controllable and periodical variable V_{dd} for the asynchronous chip to investigate the voltage variation tolerance capability. During the power delivery process, the SCC sequentially decreases the output voltage level with six steps (1.2 V >> 1.1 V >> 0.9 V >> 0.8 V >> 0.6 V >> 0.4 V) and then sequentially increases the output voltage level also in six steps (0.4 V >> 0.6 V >> 0.8 V >> 0.9 V >> 1.1 V >> 1.2 V). The interval between two steps is set to 1 ms.

The voltage waveform of the PDU output is shown in Figure 29 (A). Although the interval of changing the PDU output voltage level is 1 ms, the large value output capacitor on the PDU board is able to filter the voltage gaps existing in every voltage level change. Therefore, the output voltage waveform of PDU is smooth rather than jagged.

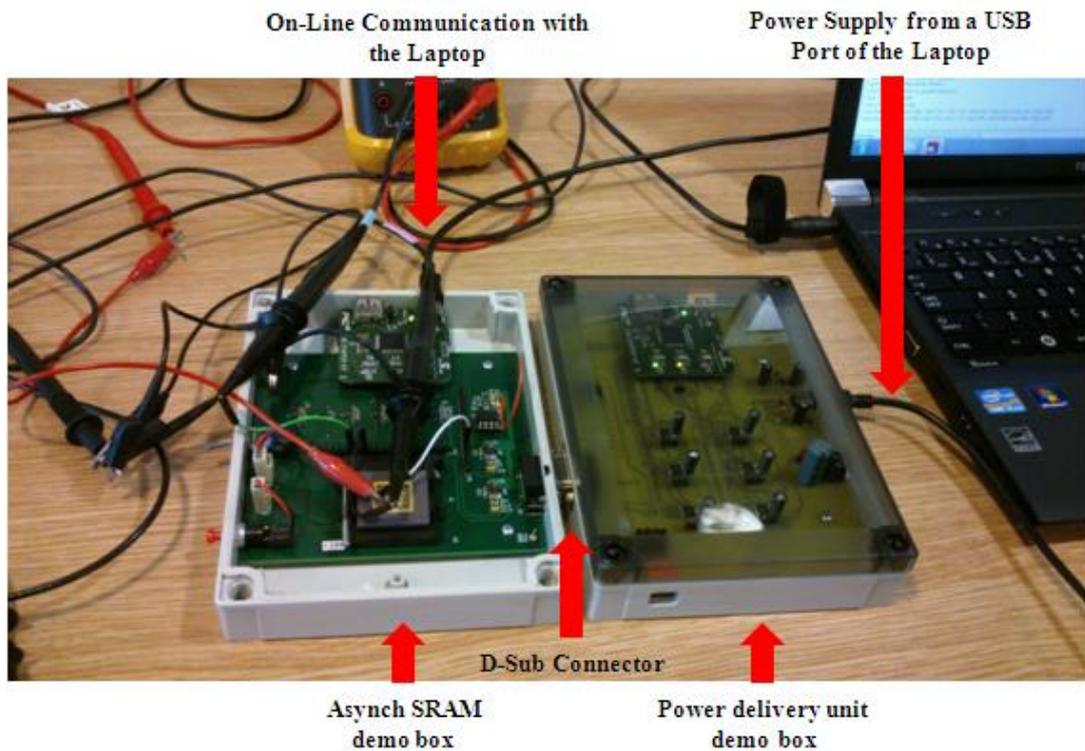


Figure 28. PDU demo box powering asynchronous self-timed SRAM demo box.

The waveform of writing acknowledgement signal of the asynchronous SRAM chip is shown in Figure 29 (B). When the V_{dd} of the SRAM chip drops below approximately 0.65 V, the signal transitions inside the chip are “frozen” due to the low V_{dd} supplied from the PDU. However, when the V_{dd} rises up above around 0.65 V, the chip is “awaked” and it starts to work again. Since the SRAM control circuit is implemented in asynchronous logic, when the V_{dd} of the SRAM chip is low, the speed of signal transitions fired inside the chip become slowly; when the V_{dd} is high, the signal transition speed becomes fast. Therefore, the transition speed of the writing acknowledgement signal is different with time.

From the investigation, asynchronous loads may have a good ability to work under variable V_{dd} , which varies in a large voltage range. Therefore, delivering a stable V_{dd} may not be necessary for powering asynchronous loads. However, so far there is not any on-chip efficient and sophisticated PDU design employed especially for generating controllable and variable power supply for asynchronous loads. Moreover, it is obviously inefficient to use SCC for achieving such a variable power supply, as SCC is originally designed to regulate stable V_{dd} . In this case, to

generate a variable power supply using the SCC, it has to charge voltage conversion ratios from time to time.

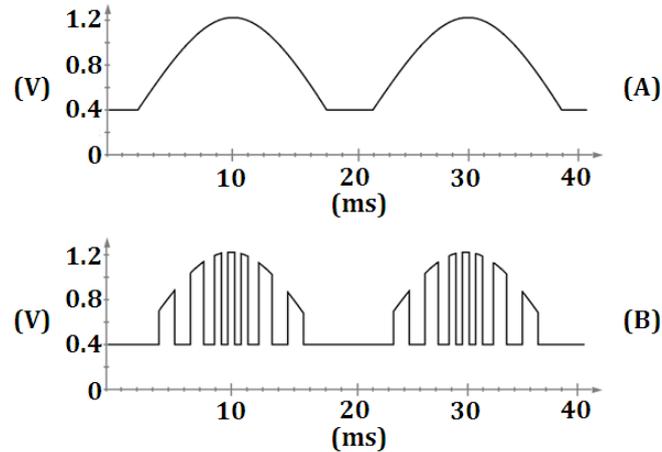


Figure 29. Waveform of PDU generating variable Vdd from 0.4 V to 1.2 V (A) and waveform of writing acknowledgement signal of asynchronous self-timed SRAM chip working with variable Vdd delivered from PDU board (B).

Additionally, for normal SCC designs, if the required output voltage level is lower than the input of the SCC, the voltage conversion (such as $2/3$, $1/2$ and $1/3$) is always performed in every capacitor switching. Almost all signals used to drive switches have to be renewed in each switching. This may cause very large power consumption in control. And it may also cause large power leakage, as it is very hard to guarantee that all control signals will be renewed simultaneously during voltage conversion. For example, the switches connected to GND may not be switched off in time and the input power may be lost by such leakage.

4.6 Summary and Conclusions

In this chapter, a typical on-chip SCC designed for powering biomedical implantable electronic devices (introduced in Section 3.2.2) is implemented by hardware for on-chip power delivery problem exploration. The hardware implementation is introduced in details. In order to meet DVS requirements from loads, the input of the SCC circuit is optimized to generate six fixed output voltage levels based on four conversion ratios. Additionally, to efficiently and fast control the PDU behaviour and sense the PDU output voltage level, three sampling

methods are developed, compared, and analyzed in term of the PDU sampling speed and power delivery response speed.

For the SCC research, three tests are performed in terms of 1) delivering power with a fixed voltage level to an adjustable RC load, 2) delivering power in six various voltage levels to a fixed-value RC load, and 3) delivering a variable power to an asynchronous self-timed SRAM chip. In Test 1, the SCC control method enable the SCC to have a good ability to maintain its output voltage level even powering a RC load even with very small resistance. In Test 2, the controller is able to deliver six various voltage levels in a high accuracy. In Test 3, the SCC has quick response to change output voltage level sequentially for generating a variable Vdd varying in a large range. The load, asynchronous self-timed SRAM chip, shows very good voltage variation tolerance ability working under the variable Vdd.

From the SCC investigation, regulating and delivering a stable Vdd may not be necessary for powering asynchronous loads, as the asynchronous SRAM chip may have a good capability to work under a variable Vdd. Additionally, using SCC for achieving such kind of power supply is obviously inefficient, as 1) SCC is originally designed for delivering stable power supply (usually aiming at powering synchronous loads); 2) SCC needs change voltage conversion ratios from time to time to generate a variable power supply; 3) it may be very hard to estimate amount of energy delivered to asynchronous loads because of varying voltage conversion ratios; 4) voltage conversion (such as $2/3$, $1/2$, and $1/3$) may cause large power lost because control signal cannot be renewed simultaneously during power delivery process; and 5) although SCC can generate variable power supply, it actually still regulate power in a very small range and causes large amount of capacitor switching unfortunately.

Chapter 5

A Novel Power Delivery Method

5.1 Introduction

Energy Harvesting (EH) is becoming a more popular method of generating energy from ambient heat, light, radio, or vibrations for computational systems, especially in sensor networks and mobile systems [178], with diverse energy conversion methods investigated [179]. An EH power delivery method is presented in Section 1.1 (Chapter 1), in which a MANAGY micro-system and a rechargeable battery is included. The MANAGY provides a direct power path from energy harvesters to internal loads bypassing a rechargeable battery when obtained energy is enough to supply the load. If the obtained energy is not enough, the battery is used as a supplement.

Energy-aware computations and energy-efficient systems have become popular topics of research, especially in EH systems where energy supply is nondeterministic. EH and the reality that computation is becoming more energy-bounded are some of the inspirations for the concept of energy-modulated computing (introduced in Section 1.1, Chapter 1). Energy-modulated computing treats both energy availability and data/task requirements as system design variables and design objectives can span the entire range between finding the optimal task scheduling to spend a given energy profile and finding the best energy supply scheduling to best fulfil a task requirement.

This has motivated various techniques in trying to smooth the power flow, including temporarily storing harvested energy in components such as rechargeable batteries and off-chip supercapacitors [23], which have a number of disadvantages [24]. On the other hand, directly delivering energy generated by harvesters to computational loads might be an alternative in some applications [25]. In this chapter, it focuses on the case where power from the EH device is

directly delivered to the load on-chip bypassing or in combination with off-chip storage, targeting extreme miniaturization for future applications.

The output voltage of EH devices typically depends on the designs of the devices and the conditions of the environment from which energy is harvested. It usually does not coincide with the correct V_{dd} level for the load electronics. DC/DC converters are normally needed to convert the voltage from EH devices to suitable V_{dd} levels for the load electronics. For extreme miniaturization, the DC/DC unit may be constructed onto the same chip as the computational load. For this purpose the best existing DC/DC solution is the **Switched Capacitor DC/DC Converter (SCC)** (introduced in Section 3.2.2, Chapter 3).

For synchronous computational loads, relatively stable power supplies are needed with minimum (5% to 10%) voltage variation allowed [26]. DC/DC converters may pass on the instability in the EH voltage when an off-chip intermediate storage is not used, potentially leading to the load needing to be switched off or into sleep mode. To increase power output stability, certain DC/DC converter designs can be dynamically switched among a number of different conversion rates at the expense of frequent mode switching. For example, variable power supply may cause frequent switching operations within SCCs [27].

Asynchronous computational loads in general can, on the other hand, tolerate wide voltage variations (introduced in Section 1.1, Chapter 1 and Section 4.5.4, Chapter 4). This makes them good candidates for use in EH systems with direct power delivery. And a provided proper V_{dd} range can be obtained. However, the overall performance of a combination of asynchronous loads and EH with DC/DC power delivery chain remains poorly studied. Additionally, since typical DC/DC converter designs target synchronous loads, whether they are suitable for asynchronous loads is unknown. There may also exist other solutions to voltage conversion between EH devices and asynchronous loads.

This chapter concentrates on methods which deliver power directly from EH devices to computational loads. A new power delivery method, based on an on-chip **Capacitor Bank Block (CBB)**, is proposed. It is aimed at providing a degree of programmability in the power delivery control so that power can be intelligently

delivered under different EH source and load conditions for performance or efficiency goals. This method is comparatively investigated with conventional SCC investigated in Chapter 4. The comprehensive analysis across the two different types of power delivery and synchronous and asynchronous loads represents the first attempt to systematically study the issue of on-chip power delivery from EH devices to computational loads.

5.2 Proposed Capacitor Bank Block (CBB)

Chapter 4 has introduced the investigations of a conventional SCC in details. However, SCC may not be a universal and all-purpose power delivery choice for all applications. Especially, there are still challenges existing in EH systems. Therefore, an on-chip CBB method is proposed and the author tries to solve some of these challenges using this method.

5.2.1 *Challenges of Using SCC in Energy Harvesting Systems*

Conventional DVS or DVFS systems require a stable and relatively high input Vdd which is converted into a number of different, usually lower, stable output Vdds [180], [181], [182], and [183]. This calls for highly periodic and highly amplitude constrained operation of the standard SCC. The EH environment, on the other hand, tends to imply incoming voltage sources with a high degree of uncertainty and low to even no stability, and asynchronous loads can operate functionally correctly if given unstable voltage supplies by becoming faster and slower on the go without logical errors. Intuitively, an aperiodic and amplitude-flexible power delivery method would be better not only for EH systems specifically, but also for energy-proportional systems in general.

5.2.2 *CBB Concept and Proposed CBB Structure*

With asynchronous loads, it may not be necessary to maintain a stable Vdd. This section provides an overview of the proposed CBB which provides unstable Vdds. With efficient voltage sensors (e.g. [184] and [185]) and a simple switching controller, CBB can achieve an obvious flexibility in charging and discharging capacitors to provide power supply to asynchronous loads.

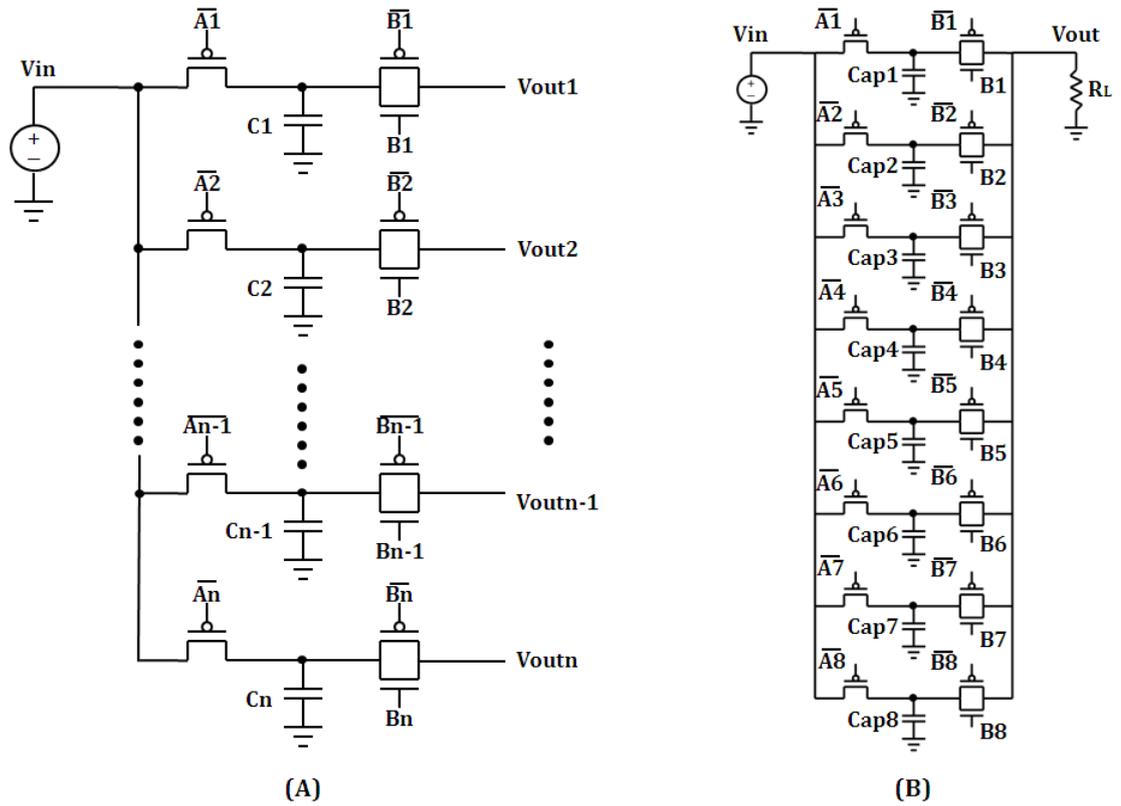


Figure 30. (A) CBB concept and (B) proposed CBB structure.

Figure 30 (A) presents the CBB concept, which consists of a number of capacitors and switches. P-type CMOS transistors are for input switches, and transmission gates are for output switches. There is at least one input resource used for charging the capacitors, and there is at least one output used for discharging the capacitors onto a computational load. For example, V_{out1} to V_{outn} can be used as individual outputs for load. This makes it possible to process more than one task in parallel, as long as there is enough energy. The values of the capacitors in a CBB do not need to be the same, and charging them to the same voltage may need different time. With a voltage sensor, the total amount of energy stored in a capacitor can be estimated as capacitance value is known. The energy passed to the load also can be estimated by checking the voltage discharging range. Therefore, the amount of energy stored in each capacitor can be very flexible and it depends on how much energy the load wants to draw within one discharge process. In this case, the whole power delivery process can be separated into very fine steps for implementing task and scheduling purposes. If such load characteristics as “energy per action” or “time per action” are provided, CBB is able

to provide an efficient platform for task and power management for asynchronous load in very flexible ways.

In order to compare with the conventional SCC easily and fairly, in this chapter only the simple CBB structure in Figure 30 (B) is studied. The proposed CBB employs eight capacitors all of the same value. This structure only has one input and one output. Therefore, only one task can be processed at any time. The charging and discharging processes are according to the first fully charged first discharging rule.

5.2.3 Finite State Machines (FSM) for CBB Control

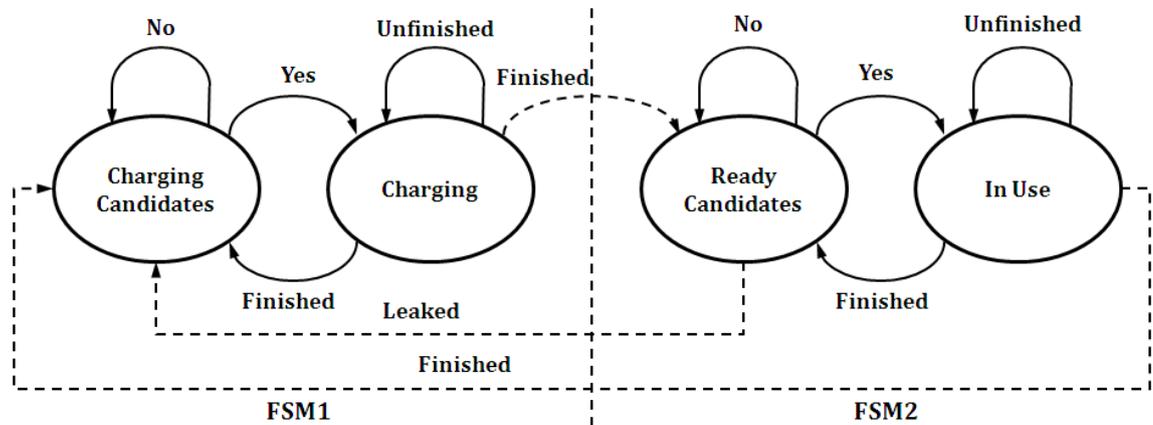


Figure 31. FSMs for CBB control (Here the solid arrows stand for data and control flow, and the dashed arrows for the data moving between machines).

The CBB control principle is described in Figure 31 using FSMs. FSM1 describes charging control and FSM2 discharging control. Each capacitor may belong to four states, charging candidate, charging, charged (ready candidate) and discharging (in use). If there are candidates and input energy available, CBB charges available capacitors one by one. The voltage level at the capacitor can be monitored by voltage sensors to decide when a charging capacitor becomes ready. A capacitor supplying its stored energy to the load is in use (discharging). When its energy is spent, it becomes a charging candidate. The CBB starts discharging the ready capacitors one by one when ready candidates and load tasks exist. Ready candidates may become charging candidates once they lose enough energy through leakage.

5.2.4 CBB Behaviours with Different Loads

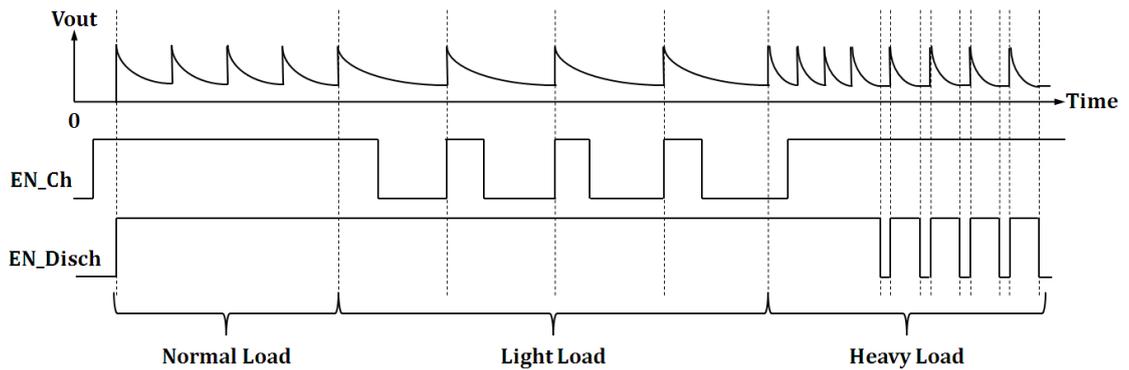


Figure 32. Charge and discharge behaviours of CBB powering with normal-weight load, light-weight load, and heavy-weight load.

Figure 32 shows the CBB behaviour working with different loads based on the same power supply. With appropriate loads, the charging and discharging processes may run in parallel without stop. With a light load, charging may need to be stopped periodically when all capacitors are charged to the required voltage, throwing away any surplus energy from the source. With heavy loads, CBB has to occasionally stop discharging and wait for a capacitor reaching the required voltage. Such load stoppages may entail stop/restart overheads for the load. The CBB method provides the buffering for quick charging and discharging control to reduce these undesirable situations.

Figure 33 provides an overview of CBB charging and discharging control behaviour working with voltage sensors. In (A), A0, A1 and A2 are charging codes used to select one of eight capacitors. The output signal of a voltage sensor Vsen0 is triggered to “1” when capacitors are charged to the required voltage. When Vsen0 is set to “1”, charging process is moved to charge next capacitor which is a charging candidate. Since the voltage at the charging candidate is low, Vsen0 is set to “0” again. In (B), B0, B1 and B2 are discharging codes used to select one of eight capacitors. When the voltage at a capacitor is discharged to the required level, the output signal of voltage sensor Vsen1 is set to “1”. And the discharging process is moved to the next ready candidate. Since the voltage at the ready candidate is high, Vsen1 is set to “0” again.

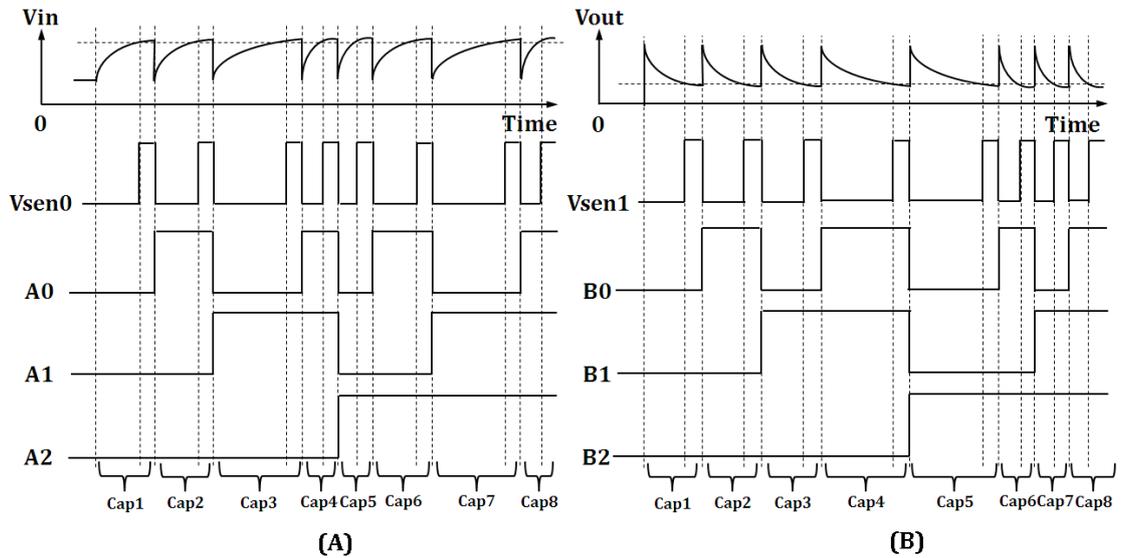


Figure 33. (A) CBB charging control and (B) discharging control cooperating with voltage sensors.

5.3 Comparison Study System Design

In order to compare the performances of SCC and CBB powering loads with various weight in EH systems, a comparison study system is designed and introduced below. In the system, piezoelectric EH circuit model is used to demonstrate that the system directly harvests energy from environment. Then the harvested energy profile data, generated by the model, will be regulated by SCC and CBB separately, and delivered to loads.

5.3.1 Piezoelectric Energy Harvesting Circuit Model

A simple piezoelectric EH circuit model is employed as a variable power supply for the comparative investigation. The EH circuit model has been introduced in Section 2.2.1, Chapter 2 (see **Figure 4**). The model is constructed in Matlab Simulink environment. The voltage and current profile data are recorded by using voltage and current sensor components of Simscape Packet. The profile data will be used for power delivery performance comparison later.

Current-technology piezoelectric MEMS energy transducers can achieve wide working frequency ranges from a few tenth of kHz to several tenth of MHz (introduced in Section 2.2.1, Chapter 2). Therefore, 1 MHz working frequency assumption is in line with these technologies.

Years ago, a low-power wireless sensor system used approximately 700 μW of power. This has more recently fallen below 100 μW and some applications are even targeted at a few microwatts or less [186]. Therefore, the variable DC with peak values 10 μA , 100 μA , and 1 mA are chosen in this chapter to represent sparse, moderate, and abundant supplies respectively. For the simulation in Matlab, the variable DC supply data with three different peak values of 10 μA , 100 μA , and 1 mA are recorded in the database. The frequency is 1 MHz and the period of each variable DC EH pulse is 1 μs .

5.3.2 System for Comparative Studies

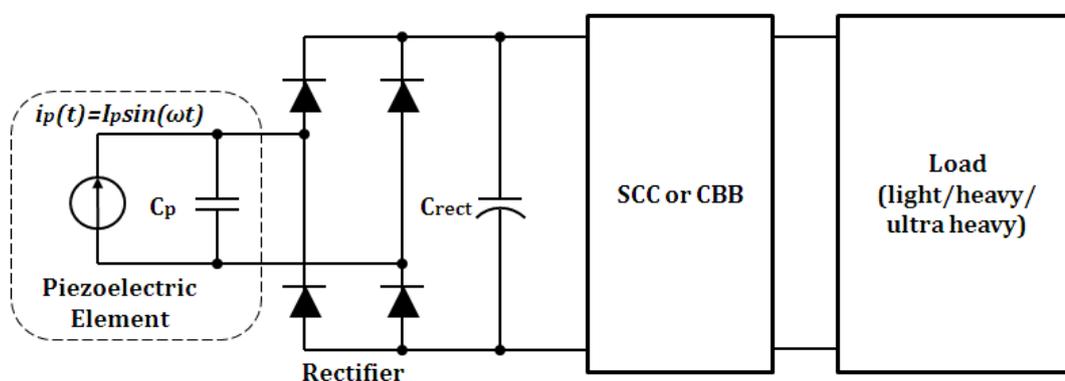


Figure 34. System architecture for comparative studies.

The entire system shown in **Figure 34** consists of a piezoelectric EH circuit as the power supply, a power delivery block, and a load. Two types of power delivery blocks, one based on SCC and the other on CBB, will be studied. Loads, in the forms of 16-bit self-timed counters from [34], with three different power consumption magnitudes, light, heavy and ultra-heavy, are investigated. Such a counter has a good linear proportional relationship between its computational effort and its numerical output. One counter is assumed as light load, three counters in parallel as heavy load and nine counters in parallel as ultra-heavy load.

Figure 35 shows the structure of the different power delivery blocks. These structures are implemented in UMC 90nm CMOS technology in Cadence tools. The model of the piezoelectric EH circuit (**Figure 4(A)**, Chapter 2) is converted directly to Cadence environment from Matlab results implemented by employing *Independent Piece-Wise Linear current Source Based on File (Ipwlf)*. The output

of I_{pwl} is used as the EH power profile in **Figure 35**. In the analysis, the nominal V_{dd} of the PDU is set to 1 V according to the UMC 90nm CMOS technology library specifications. MIM capacitors [138] are used in this comparison.

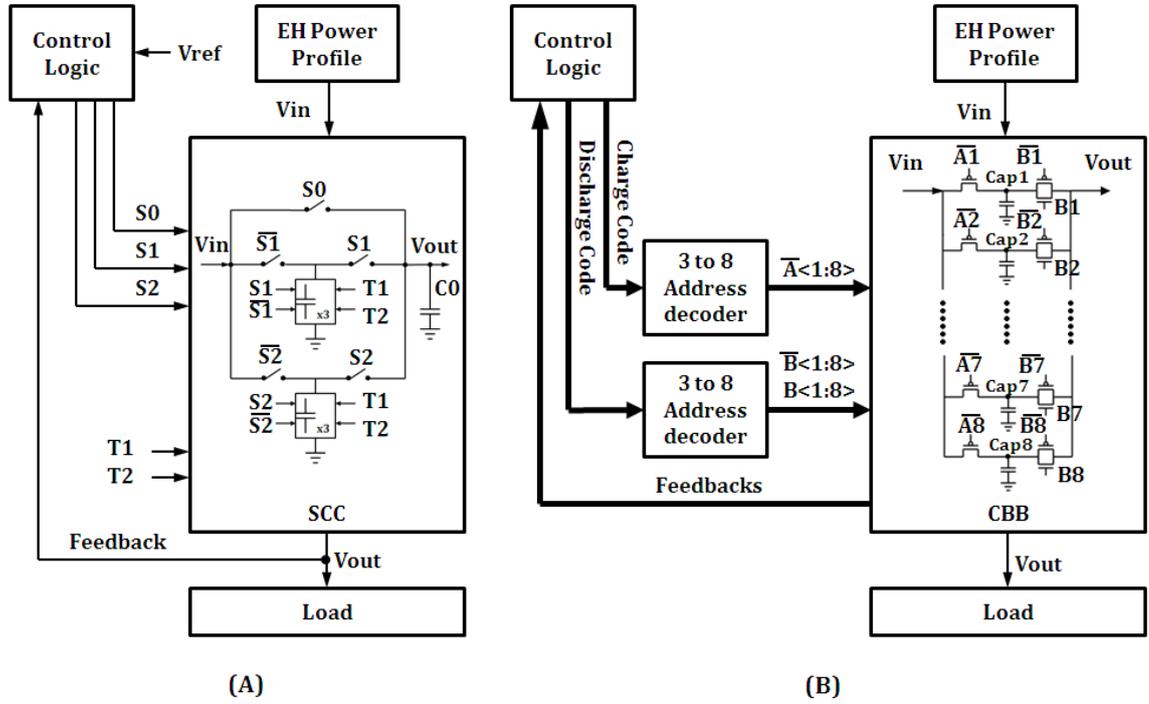


Figure 35. Testing system with SCC (A) and CBB (B) respectively.

In these studies, in **Figure 35 (A)** the SCC is assumed always to provide 1 V V_{dd} to load. Thus V_{Aref} is preset to 1 V, and T_1 and T_2 are preset to choose the conversion ratio 1/1. By changing the transistor size of the current mirror circuit inside the dual threshold comparator, the threshold voltage V_{Aref} and V_{Bref} can be accurately adjusted (introduced in Section 3.2.2, Chapter 3). Therefore, the output voltage ripple is approximately 0.1 V and the average voltage at the output capacitor C_0 is almost maintained at 1 V. The V_{dd} at load is slightly lower than 1V. The feedback from the voltage at C_0 to the control logic block is used by the comparator to compare with V_{ref} .

In **Figure 35 (B)**, the CBB power delivery block, control inputs in data form and two 3-to-8 line address decoders with address latches are used as a simple switching controller. The feedbacks are capacitor voltages. The control inputs consist of 8-bit control signals for charging enable (1 bit), discharging enable (1 bit), and charging and discharging addresses (6 bits), which determine the FSM transitions (introduced in Section 5.2.3 and Section 5.2.4).

The total capacitor value of CBB and SCC is the same, 80 pF, for similar on-chip size costs. For SCC, inside of these two conversion blocks, each capacitor has the same value, 11 pF. The value of the output capacitor C_0 is set to 14 pF. For CBB, eight capacitors have the same value 10 pF. Both SCC and CBB maintain the V_{dd} at load by connecting and disconnecting capacitors. The amount of such capacitor switchings is related to the energy overhead of running these power delivery blocks and will be monitored in the analysis.

In previous work [187] the advantages offered by the additional flexibility and programmability of the CBB method are demonstrated. The comparative studies concentrate on more in-depth comparative analysis of SCC and a relatively dumb CBB to demonstrate the validity of CBB's aperiodic and amplitude flexible approach.

5.4 Assumptions

Four assumptions are preset for the comparison study: 1) asynchronous load with SCC, 2) synchronous load with SCC, 3) Asynchronous load with CBB, and 4) synchronous load with CBB.

5.4.1 *Asynchronous Load with SCC*

Although digital systems can work under low voltage such as 0.3V for power saving [35], designs tend to work above 0.4V to maintain a safe margin [188] unless specifically targeting the sub-threshold region [189]. In this study, asynchronous circuits in UMC 90nm CMOS technology are investigated under V_{dd} from 1 V to 0.4 V. Although the self-timed counters used here work correctly over a much wider V_{dd} range, the author tries to represent a greater class of asynchronous loads by limiting the V_{dd} range and switching the load off when V_{dd} goes above 1 V or below 0.4 V.

5.4.2 *Synchronous Load with SCC*

For comparison fairness, the same self-timed counters are used as load in the synchronous load studies. Synchronous systems are usually assumed to be able to tolerate 10% of voltage variation. Therefore, in the studying synchronous loads,

once the load V_{dd} goes above 1 V or below 0.9 V, the controller of the system switches the power supply off the load. The SCC output is required to be charged up to 1 V before starting to deliver power to load.

5.4.3 Asynchronous Load with CBB

In the CBB, each capacitor is required to be charged to 1 V then discharged onto load down to 0.4 V. Discharging from 1 V to 0.4 V, the capacitor distributes 84% of its total stored energy to the load (see Equation (1)). The CBB control is according to first fully charged first discharging rule in addition to **Figure 31**.

$$E = \frac{1}{2}CV^2 \quad (1)$$

5.4.4 Synchronous Load with CBB

Since CBB is supposed to supply variable V_{dd} from 1 V to 0.4 V, it is unfair to let a synchronous circuit work always under the very slow clock according to the worst case 0.4 V to guarantee correctness or consider the potentially heavy clock frequency controller for DVFS. This system composition is therefore not studied.

5.5 Load Performance Results

For each system composition, three groups of experiments were performed with EH power supplies in three different strengths, corresponding to peak values of 10 μ A, 100 μ A and 1 mA from the EH source. For the moderate power supply (peak value 100 μ A), light and heavy loads are used to study the performances of SCC and CBB in normal working conditions. For the abundant power supply (peak value 1 mA), ultra-heavy load is used to investigate load influences in extreme situations (load exceeds the SCC design limit). For the sparse power supply (peak value 10 μ A), a soft task (implementing a required amount of computation within an acceptable time) in a light load helps illustrate the power delivery flexibility of SCC and CBB.

The resulting output waveforms of SCC and CBB are recorded as V_{dd} to the load. Other waveforms are also recorded. For instance, in the SCC, the switching signals S_0 , S_1 and S_2 control the direct switch and conversion blocks. The number of

switchings in these signals is recorded for comparative studies. In the CBB, the voltage waveforms of Cap1 to Cap8 show the charging and discharging process and voltage status on each capacitor, therefore the number of capacitor switchings is directly reflected in the times of charging and discharging actions. Q0 to Q15 are the outputs of a single 16-bit counter. The numbers counted by the counter are recorded as the amount of load computation. Energy consumption and energy delivery efficiency are derived from the studies using Cadence Virtuoso Spectre Circuit Simulator and Analysis Calculator in the ADE(G)XL Environment.

Since, in each group of experiments, the energy supplied by the EH is the same over the same time period, energy delivery efficiency as seen from the load can be derived from the amount of switching activity in load in a given time period. The self-timed counter as load has the characteristic that it counts when it has sufficient power and each count can be treated as the basic quantity of computation in these experiments. The ultimate metric here is thus how many counts can be generated given some amount of energy from the EH power supply.

5.5.1 Computation Performances with Moderate Power Supply

In this group, the EH supply peak current value is set to 100 uA and the supply is only available within 3 us and then disappears, shown as “DC Input” in **Figure 36**, **Figure 38** and **Figure 39**. One counter is used as light load and three counters in parallel are used as heavy load.

• Power Delivery Unit Behaviours and Load Computation Performances

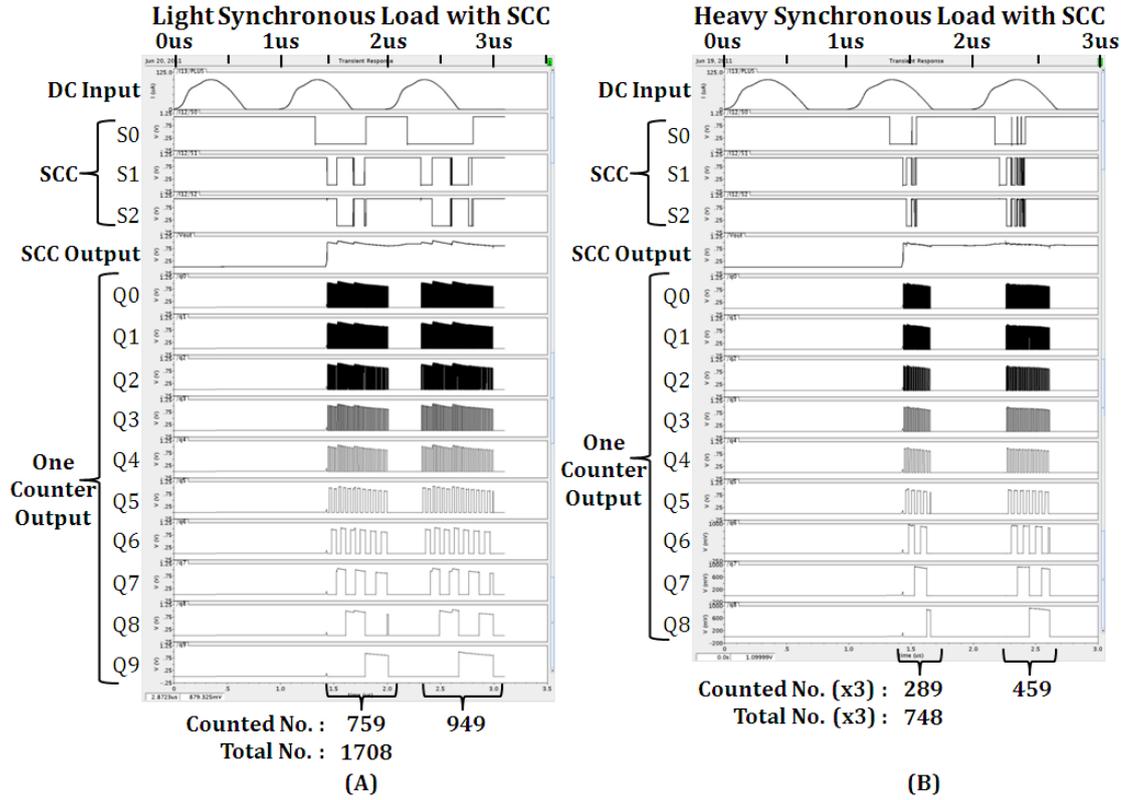


Figure 36. Computation performances of SCC powering light (A) and heavy (B) synchronous loads.

Figure 36 shows the computation performance of SCC powering light (A) and heavy (B) synchronous loads. SCC starts power delivery for light and heavy synchronous loads at the same time when the voltage at C0 rises beyond 1 V. And SCC has to switch the load off when the voltage at C0 falls below 0.9 V. Since heavy load draws more current than light load, it shortens the power delivery time significantly. Both light load and heavy load have to be switched off and re-computed when a non-power gap comes. Light load gets 1708 total computation with one power delivery stop. For heavy load, each counter achieves 748 computations in total and also has one power delivery stop. Any associated overheads with restarting here are not calculated.

The close up of SCC behaviour for powering heavy synchronous load from 2.16 us to 2.43 us is shown in Figure 37 (A). Before period 1, load is switched off. Then during period 1, conversion blocks start to power load alternatively. However, since the current pull-down ability from load is stronger than charging current from power source, the switching frequency begins to increase gradually. In period

3, although the EH power is approximately in the peak value, heavy load still cannot be supported and the switching frequency reaches highest within a very short period. During periods 2 and 3, the direct switch has to be switched on (set S0 to “1”) three times to directly connect the source to output capacitor C0. The energy provided by switching two conversion blocks cannot raise Vout above VBref at the end of period 3. Direct switch has to be connected again. At this time the voltage at C0 falls below VBref (around 0.95 V) but does not reach 0.9 V. Since the source is directly charging the output capacitor C0, load can continue working for a short period. When the voltage at C0 falls below 0.9 due to not enough energy coming from the source, load is switched off. In period 1, the number of capacitor switchings is 4. In period 2, it is 28. In period 3, it is 20.

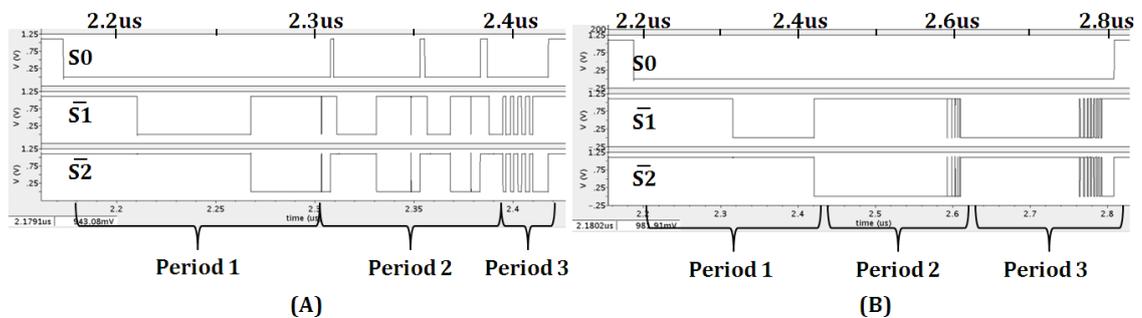


Figure 37. Behaviours of SCC with heavy synchronous load from 2.16 us to 2.43 us (A) and with light synchronous load from 2.16 us to 2.83 us (B).

In **Figure 37 (B)**, the close up of SCC behaviour powering light synchronous load from 2.16 us to 2.83 us is shown. When the power supply begins to decrease, the switching times start to increase gradually like (A) in periods 2 and 3. The power delivery stops after 2.8 us. The capacitor switching number in period 1 is 4; in period 2 is 22 and in period 3 is 32. The SCC switching times in period 2 and period 3 for light load are more than that for heavy load in the same periods. For powering heavy load, load is connected directly to source three times (set S0 to “1”). For powering light load, since the energy from switching conversion blocks is enough to raise Vout above VBref, S0 does not need to be set to “1”.

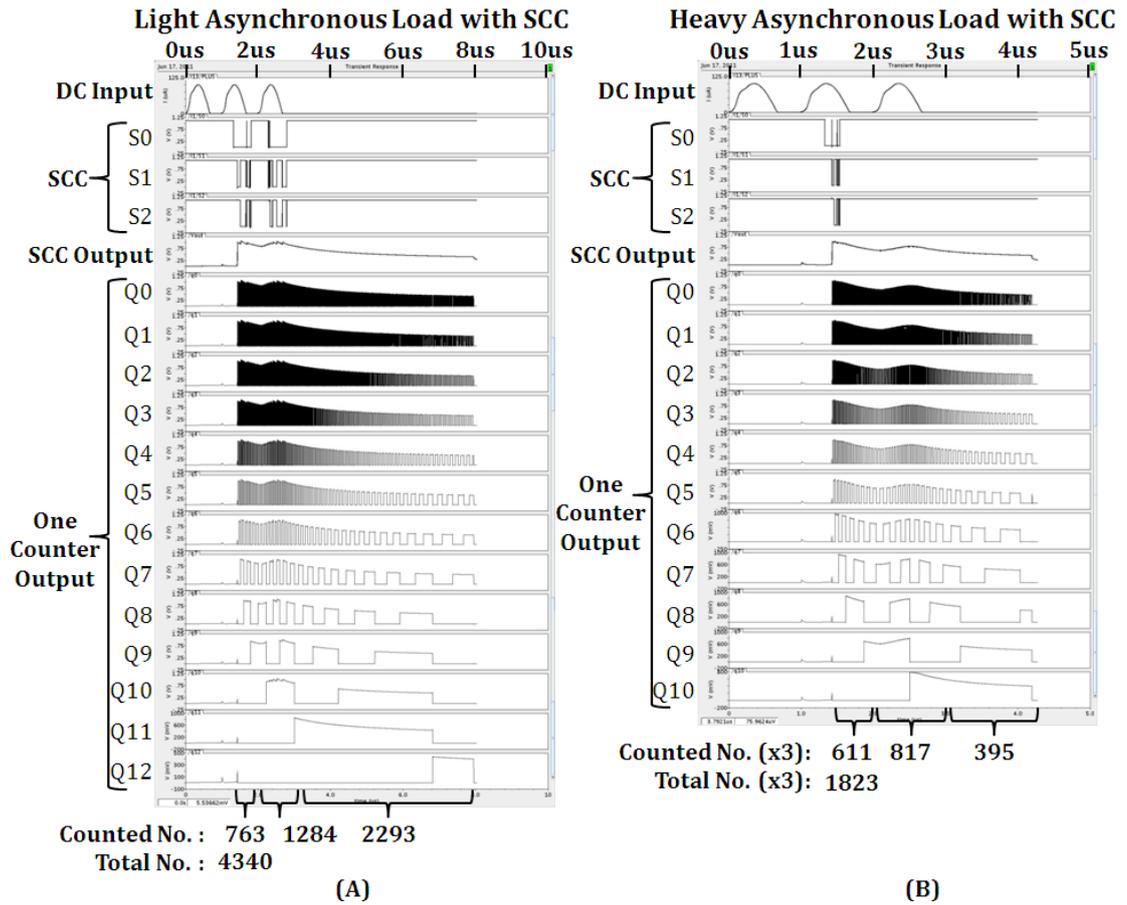


Figure 38. Computation performances of SCC powering light (A) and heavy (B) asynchronous loads.

The compositions of light and heavy asynchronous load powered by SCC are shown in **Figure 38**. The SCC starts power delivery when C0 is charged to 1 V. It will switch between conversion blocks as long as the voltage at C0 is above 0.95 V. When the input voltage falls below this threshold, normal SCC operation stops. In these experiments, the SCC is additionally allowed to give its stored energy to the load as if it is a dumb capacitor. The extra counts generated demonstrate how much energy the standard SCC would withhold from the load when power from the EH stops. When SCC stops switching between conversion blocks, direct switch connects C0 to the source. At the same time, the conversion blocks are connected to the source to be charged. If a non-power gap comes, the output capacitor and conversion blocks will be connected to the load.

In **Figure 38 (A)** light load works without stop until 7.930 us and 4340 total counts are achieved. Among these counts, the first 760 came from normal SCC switching mode, then followed by 427 counts when the SCC is used as a dumb

capacitor (These would have been withheld from the load in a standard SCC implementation and the load would stop during this period). Then 844 counts are delivered by the SCC in normal mode followed by a further 2309 counts with the SCC as a dumb capacitor. With the SCC operating in the standard mode, there would have been only 427 counts followed by a gap then 844 further counts delivered. It's quite clear that the majority of the energy would have been withheld.

In **Figure 38 (B)** with the heavy load, the SCC powering heavy load only switches conversion blocks during the second EH supply pulse. When the third pulse comes, the voltage at C0 cannot rise to 1V to trigger SCC. The total computation achieved by each counter is 281 during normal SCC operation and a further 1542 counts are delivered with the SCC serving as a dumb capacitor.

Figure 39 shows the light and heavy asynchronous loads powered by CBB. Eight capacitors with the same value are charged and discharged one by one. The period of discharging a capacitor from 1 V to 0.4 V with heavy load (227 ns) is significantly shorter than that of discharging a capacitor with light load (665 ns) with the same discharging range. Thus, shorter discharge period for each capacitor enable the CBB with heavy load to store all the energy coming from the source within 3 us and CBB stops power delivery at 4.105us, shown in Figure 39 (B).

However, with the light load, the average charging time for each capacitor is shorter than the average discharging time and CBB has to stop charging three times in the entire process when all available capacitors are full discharged to 1 V. In Figure 39 (A), after Cap1 is charged to 1 V at 1.440 us, the charging operation has to wait until Cap2 is discharged to 0.4 V. After that, only Cap2 and Cap3 are charged to 1 V from the second and third DC pulses even though one single such pulse was able to charge more than 5 capacitors. The light load gets 3908 total counts and stops computation at 7.730 us. In the heavy load, each counter gets 1983 total counts. This demonstrates the importance of load or task scheduling to improve energy efficiency.

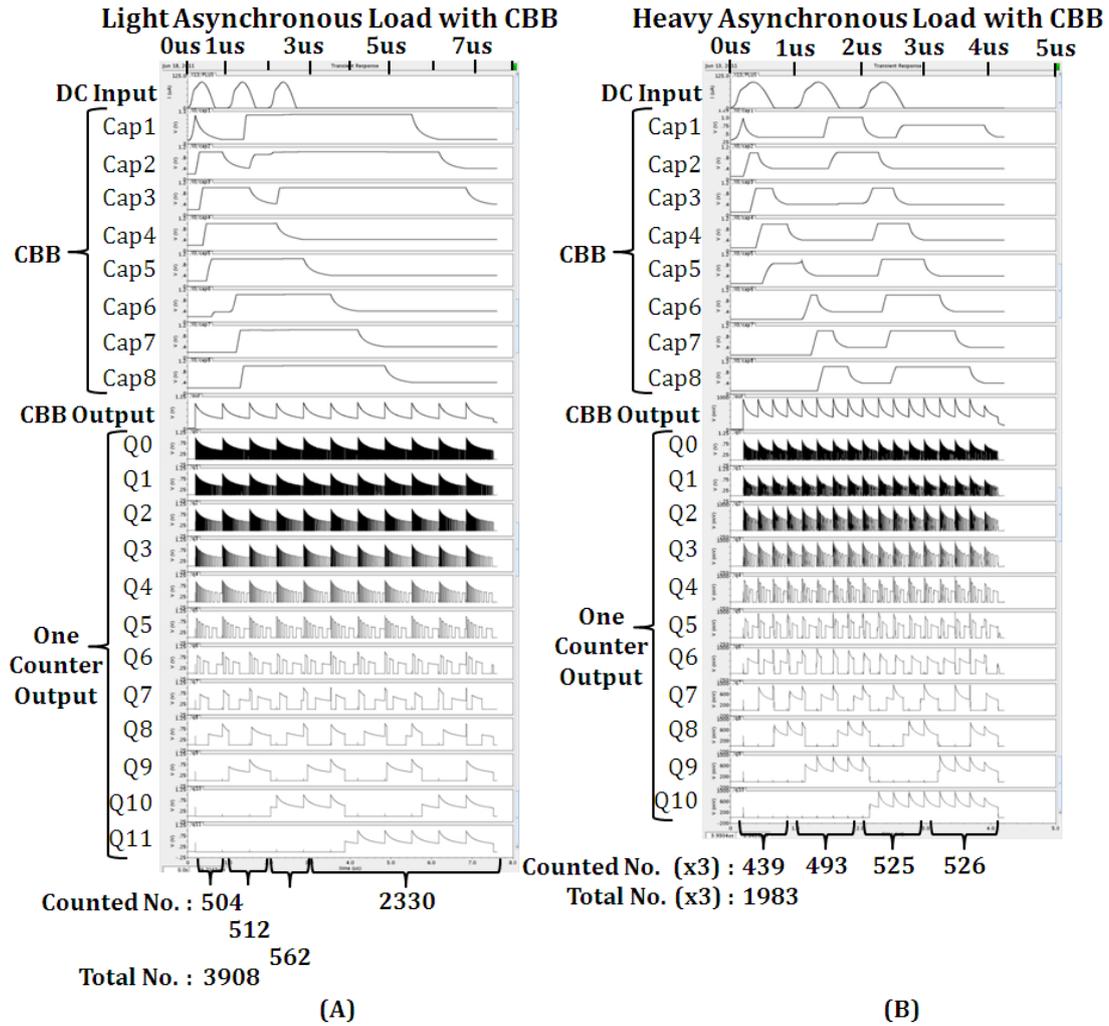


Figure 39. Computation performances of CBB powering light (A) and heavy (B) asynchronous loads.

- **Energy Delivery Efficiency and Energy Consumed for Switchings**

For quickly starting the load, CBB has an obvious advantage and the load begins computation when Cap1 (10pf) is fully charged to 1 V. It only takes 196 ns in the case of the moderate EH power supply. Loads powered by SCC can only start computation when all capacitors (80pf) are fully charged to 1 V. It takes 1.434 us in this case. In latency therefore the CBB performs better. Asynchronous loads can better extend their computation using the residual energy on capacitors, potentially “living across” non-power periods.

In Table VI, the energy delivery efficiency of SCC and CBB powering different load is shown. For heavy load, the total computation is the total counts from three counters. Asynchronous load powered by CBB achieves the highest computation

(5949). Since the average discharging time is comparable to the average charging time, CBB does not stop charging when power is available. Asynchronous load powered by SCC ranks in the second (5469) if the entire stored energy is drained into the load after normal SCC operation ends. The average working voltage of asynchronous load powered by CBB (0.548 V) is lower than that of asynchronous load powered by SCC (0.611 V) accounting for the additional counts as energy per count is lower at the lower voltage. It is worth noting that if the stored energy is allowed to be drained onto the load after supply voltage dips below 0.95 V the SCC scheme delivers more energy to the load than the CBB even though they have the same total amount of capacitance. Asynchronous load with SCC has the highest efficiency in energy delivered but not the computation done because much of the energy was delivered at higher voltages. Synchronous load with SCC gets the smallest computation (2244). Although SCC delivers higher average Vdd to load (0.959 V), synchronous load has to be switched off periodically and only works within short periods.

Table VI. Energy delivery efficiency of SCC and CBB with different load.

PDU Type	SCC				CBB	
	Synchronous		Asynchronous		Asynchronous	
Load Type	Light	Heavy	Light	Heavy	Light	Heavy
Load Weight	Light	Heavy	Light	Heavy	Light	Heavy
Average Load Vdd (V)	0.970	0.959	0.652	0.611	0.561	0.548
Total Computation	1708	2244	4340	5469	3908	5949
Load (pJ)	42.80	51.99	71.68	73.05	47.38	67.18
Harvested Energy (pJ)	123.10	123.10	123.10	123.10	123.10	123.10
Energy Delivery Efficiency (%)	34.8%	42.2%	58.2%	59.3%	38.5%	54.6%

With light load, asynchronous load powered by SCC reaches highest computation (4340) and asynchronous load powered by CBB ranks second, mainly because the light load makes the CBB stop charging even when power is available. Compared with asynchronous loads powered by SCC and CBB, synchronous load with SCC still gets the smallest computation (1708). The advantage in energy delivery of asynchronous load with SCC (58.2%) is larger over the same load powered by CBB (38.5%) and synchronous load powered by SCC (34.8%).

Under this EH profile, a heavy load powered by SCC and CBB achieves more total computation than a light load with SCC and CBB. The heavy load pulls down the average Vdd. Therefore, working at lower Vdd and tasks (represented by counters) processed in parallel result in more total computation using the same amount of energy.

Table VII lists energy consumed for switching processes, switching times and energy per switching inside the SCC and CBB PDUs. For the SCC, the switching components include one direct switch and two conversion blocks. For the CBB, the switching components include the capacitor bank and two 3-to-8 line address decoders. For the SCC, the switching events in signals S0, S1 and S2 are recorded. For the CBB, the charging and discharging switching events are recorded. The CBB powering asynchronous loads has a smaller number of switching events due to having a very large discharging range compared with SCC powering synchronous and asynchronous loads. Since CBB powering light load has to stop charging when all capacitors are fully charged, it gets the smallest switching number. For SCC power heavy asynchronous load, due to not enough energy to trigger SCC to switching conversion blocks, a smaller switching number is needed than other loads powered by SCC. Since SCC performs more switching to maintain high stable Vdd for load, it consumes more energy in internal switching compared with CBB. The table also shows that SCC consumes more energy per switching.

Table VII. Energy consumed for switchings.

PDU Type	SCC				CBB	
	Synchronous		Asynchronous		Asynchronous	
Load Type	Light	Heavy	Light	Heavy	Light	Heavy
Load Weight	Light	Heavy	Light	Heavy	Light	Heavy
Switchings (pJ)	26.68	23.85	29.4	11.52	7.26	10.54
Number of Switchings	58	53	60	24	22	34
Energy per Switching (pJ)	0.46	0.45	0.49	0.48	0.33	0.31

5.5.2 Computation Performances with Abundant Power Supply

In this group, the EH supply peak value is set to 1 mA and the supply is only available within 2 us and then disappears, shown as “DC Input” in Figure 40. Nine counters are used as ultra-heavy load.

- **Power Delivery Unit Behaviours and Load Computation Performances**

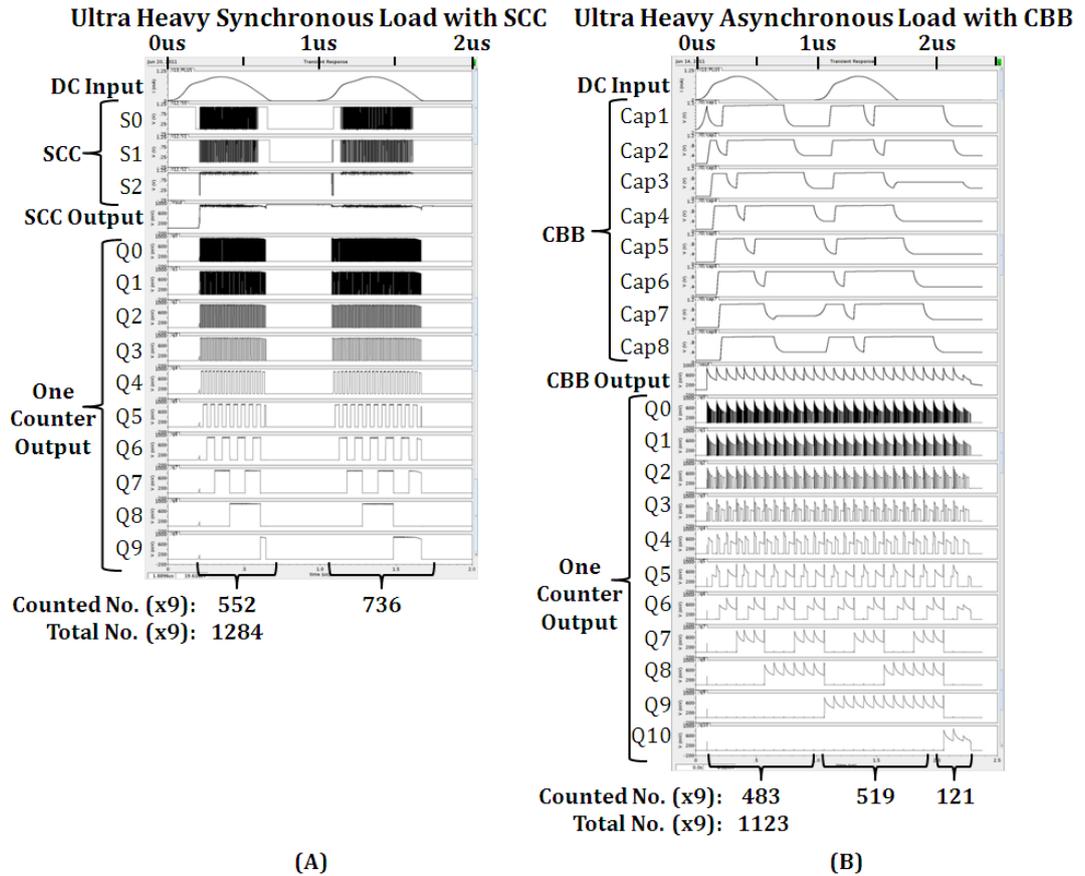


Figure 40. Computation performances of SCC powering ultra-heavy synchronous load (A) and CBB powering ultra-heavy asynchronous load (B).

Figure 40 shows the performance of SCC powering ultra-heavy synchronous load and CBB power ultra-heavy asynchronous load. In Figure 40 (A), the SCC powers can maintain a stable Vdd for load as long as sufficient power supply is available. When the power supply weakens, SCC has to switch load off due to Vdd at load falls down below 0.9 V. In Figure 40 (B), the discharging time is still significantly longer than the average charging time in the CBB because the supply is strong. After Cap8 is charged to 1 V at 0.229 us, CBB has to stop charging until the next capacitor (Cap1) is discharged to 0.4 V. After 0.229 us, energy from power supply has to be wasted during CBB stopping charging to wait for one of the capacitors to discharge to 0.4 V. For CBB powering ultra-heavy load, the power delivery process is extend beyond 2 us but not very far.

Figure 41 provides a close up of the behaviour of the SCC powering synchronous load from 0.160 us to 0.335 us. When load exceeds the SCC design limit, simply

switching two conversion blocks alternately to maintain a required stable V_{dd} for load becomes impossible. The output capacitor C₀ has to be connected by S₀ to power source to be charged up to 1 V. Then direct switch is turned off and the conversion block controlled by S₁ is switched to power load. However the conversion block fails to raise V_{out} to 1 V. The direct switch is set “on” again and the conversion block controlled by S₁ is switched to source to be charged. This powering sequence has to be repeated and switching frequency may be increased significantly.

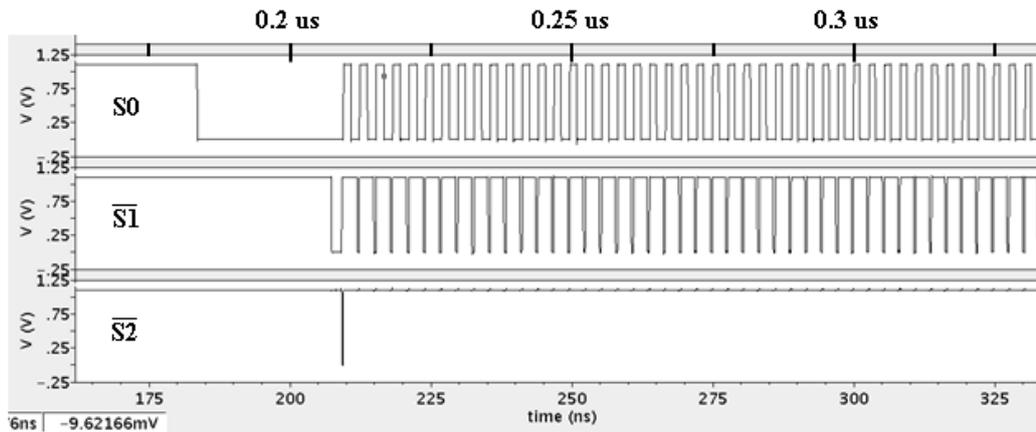


Figure 41. Behaviours of SCC powering ultra-heavy synchronous load from 0.160 us to 0.335 us.

- **Energy Delivery Efficiency and Energy Consumed for Switchings**

With the abundant power supply, CBB starts load computation at 93 ns, and SCC spends 208 ns to accumulate enough energy to start load. Table VIII provides a view regarding energy delivery efficiency of SCC powering ultra-heavy synchronous load and CBB powering ultra-heavy asynchronous load. For SCC, since the power supply is abundant, it enables load work at 0.944 V for 1.02 us. Thus the total computation contributed by synchronous load from 0 to 2 us is 11556, which is 14.3% more than that achieved by asynchronous load powered by CBB working at 0.548 V for around 2.1 us. However, comparing the energy consumed by load, asynchronous load with CBB only consumes 107.6 pJ, which is 57% less than that consumed by synchronous load with SCC. Since synchronous load with SCC gains more consumption, SCC achieves higher energy efficiency. For asynchronous load with CBB, since it works in an energy-saving way (at lower

voltage) and CBB has to stop charging 12 times, load consumes less energy and gets lower energy delivery efficiency.

Table VIII. Energy delivery efficiency of SCC and CBB with different load.

PDU Type	SCC	CBB
Load Type	Synchronous	Asynchronous
Load Weight	Ultra-heavy Load	Ultra-heavy Load
Average Load Vdd (V)	0.944	0.548
Total Computation	11556	10107
Load (pJ)	250.7	107.6
Harvested Energy (pJ)	803	803
Energy Delivery Efficiency (%)	31.2%	13.4%

Table IX. Energy consumed for switchings

PDU Type	SCC	CBB
Load Type	Synchronous	Asynchronous
Load Weight	Ultra-heavy Load	Ultra-heavy Load
Switchings (pJ)	212.10	15.95
Number of Switchings	606	55
Energy per Switching (pJ)	0.35	0.29

Table IX shows the energy consumed for switching, number of switchings and energy per switching within the different PDUs with different load. For SCC, it works under an extreme situation (load exceeds the design limit) with abundant power supply. Signal S0 and S1 alternately control the direct switch and one conversion block to power load in a very high frequency. Thus, SCC performs 606 times switching and consumes 212.10 pJ. SCC performs almost 11 times more internal switching than CBB, which only consumes 15.95 pJ on internal switching. The comparison shows an obvious difference between SCC and CBB in switching performance when the PDUs work with ultra-heavy load. And CBB consumes less energy for each switching than SCC.

5.5.3 Computation Performances with Sparse Power Supply

In this group, the EH supply peak value is set to 10 uA and the supply is available within 20 us and then disappears, shown as “DC Input” in Figure 42. One counter is used as light load. In order to show the power delivery flexibility of SCC and CBB, a soft task is assumed. The task requires a light load to perform 1000 computation within an acceptable time not beyond 20 us.

- **Power Delivery Unit Behaviors and Load Computation Performances**

For SCC, it has 80 pF total capacitor value and it has to wait until the voltage at C0 rises to 1 V. Therefore, synchronous load with SCC starts computation at 15.495 us, shown in Figure 42 (A). Then, due to the sparse power supply, synchronous load only work for a very short period. At the end of 20 us, although the total computation achieved by synchronous load is 1059, the load experiences two stops. The composition would not have been able to deal with a shorter deadline.

For CBB, the capacitor value and discharging range is known. Thus, by investigating the load characteristics, the computation from load powered by each capacitor discharging from 1 V to 0.4 V can be estimate. For example, one 16-bit self-timed counter can achieve approximately 350 counts powered by one 10 pF capacitor discharging from 1 V to 0.4 V. Therefore fully charging three capacitors can provide enough energy for asynchronous load to achieve 1000 computation without power delivery stops. In Figure 42 (B), three capacitors are fully charged to 1 V at 5.402 us. By discharging these three capacitors to 0.4 V one by one, asynchronous load achieve 1063 computation within 1.988 us. In other words, the composition is able to satisfy a much shorter deadline. Thus CBB powering asynchronous load shows an obviously flexibility for implementing task scheduling under a sparse power supply.

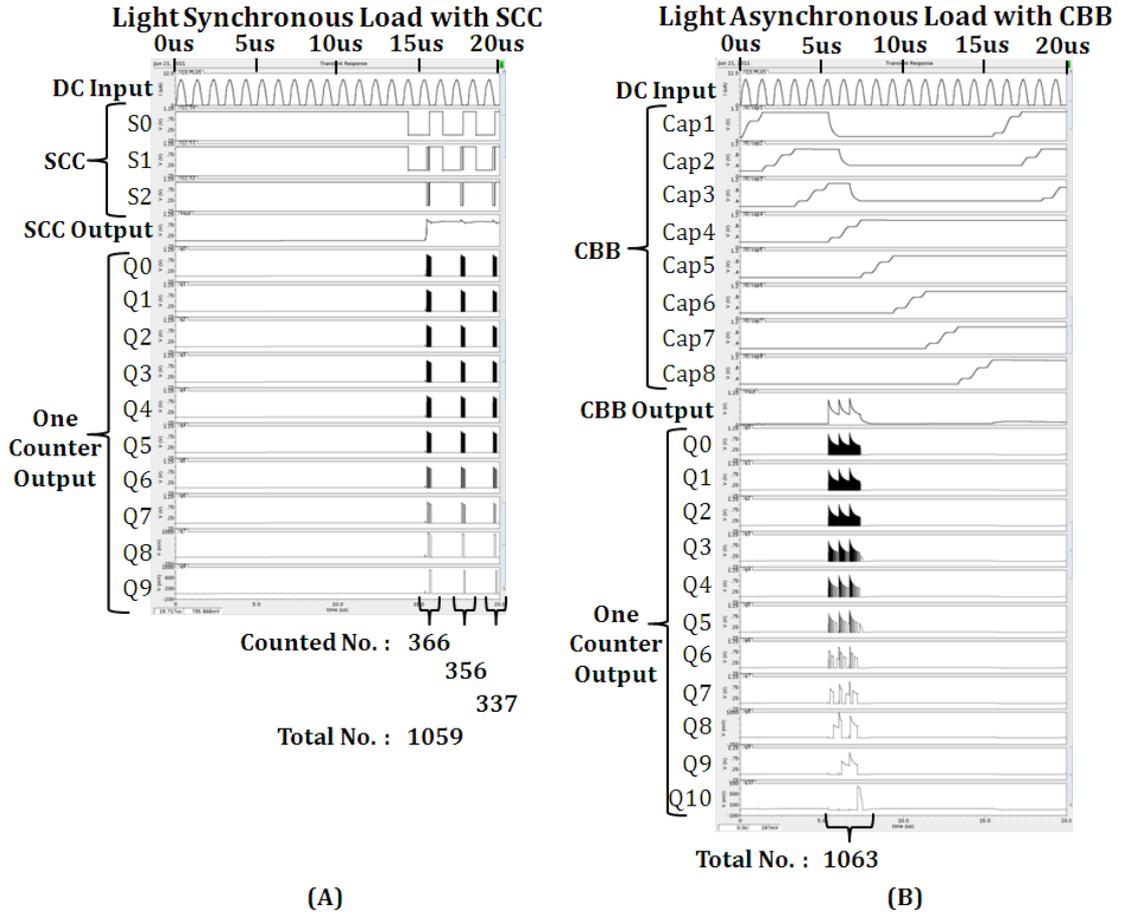


Figure 42. Computation performances of SCC powering light synchronous load (A) and CBB powering light asynchronous load (B).

- **Energy Delivery Efficiency and Energy Consumed for Switchings**

Table X. Energy delivery efficiency of SCC and CBB with different load.

PDU Type	SCC	CBB
Load Type	Synchronous	Asynchronous
Load Weight	Light Load	Light Load
Average Load Vdd (V)	0.968	0.554
Total Computation	1059	1063
Load (pJ)	24.73	12.95
Harvested Energy (pJ)	90.19	34.00
Energy Delivery Efficiency (%)	27.4%	38.1%

Table X lists the energy efficiency of SCC and CBB with different loads. Asynchronous load powered by CBB consumed 47.6% less energy to achieve 1063 computation than synchronous load powered by SCC to achieve 1059 computation. The “harvested energy” for SCC and CBB listed in the table is different. For fair

comparison, the harvested energy shown in the table is counted from 0 us to the time when task is finished or the deadline is reached. For SCC, the “harvested energy” is counted from 0 us to the deadline (20 us). For CBB, the “harvested energy” is counted from 0 us to the time when task is finished (7.362 us). Therefore, CBB powering asynchronous load has higher energy delivery efficiency than SCC powering synchronous load. Because CBB is able to choose capacitors to charge and discharge according to the load requirement, it can deliver energy to load continuously and economically. However, SCC only starts to work when the voltage at C0 is charged to 1 V, with a large latency penalty. The limited energy from source is distributed to raise the voltage to high across all capacitors. Because of this the SCC is in general less flexible in power delivery.

Table XI. Energy consumed for switchings.

PDU Type	SCC	CBB
Load Type	Synchronous	Asynchronous
Load Weight	Light Load	Light Load
Switchings (pJ)	12.9	2.1
Number of Switchings	30	6
Energy per Switching (pJ)	0.43	0.35

Table XI shows the energy consumed for switching. Although SCC only has three very short working periods, it still performs 30 times switching, as SCC tries to maintain a stable V_{dd} under limited power supply. CBB powering asynchronous load to finish the task only performs 6 times switching. Compared with CBB in terms of energy consumed for switching, SCC consumes approximately 12.9 pJ, which is six times of that consumed by CBB.

5.6 Summary and Conclusions

The results in the comparative investigation show that both the SCC and CBB systems as constructed and working under these specific conditions have quite low energy delivery efficiency compared with normal DC/DC converters working under ideal conditions. For instance, buck DC/DC converters with stable power supply can have approximately constant converter efficiencies between 75% and 95% [190].

However, EH systems tend to have highly time-variable power supply. PDUs based on techniques targeting a relatively stable power source cannot maintain high conversion efficiency under such radically variable power sources. This is confirmed by the data from the standard SCC and a relatively dumb CBB. The CBB is not designed for working with stable power inputs, but its aperiodic and amplitude-flexible approach makes it better suited for storing the energy from an unpredictable power source for use by an asynchronous load.

Asynchronous loads, which are becoming more common for energy conscious design because of their low-power and energy-adaptive characteristics, can in general work under a wide Vdd range. This wide working Vdd range remains unexploited by power delivery devices focused on maintaining stable and known Vdd values.

The CBB method represents the first attempt at developing appropriate power and energy delivery units suitable for loads which can tolerate and work well under highly variable Vdds and energy sources which cannot maintain constant outputs. The methodology is simple, based on charging and discharging capacitors in a group, and produces devices which can be implemented on chip, potentially advantageous for extreme miniaturization. It also provides enough flexibility for intelligent control aimed at maximizing performance, energy efficiency and other quantifiable goals.

A CBB with a voltage sensor can support precise charging and discharging cycles and sophisticated switching algorithms. Multiple capacitors of potentially different values can provide high flexibility and programmability for the CBB method which, if fully exploited, could further improve energy delivery efficiency. For instance, in some of the experiments, if it is found that energy from the source may be wasted, discharging can be limited to a higher voltage than 0.4 V. This is effectively demonstrated by our experiments where the SCC is almost operated as a CBB, maintaining high voltages across the capacitors and delivering high voltages to the load when power supply is plentiful, and draining down the capacitors to maintain computation when the supply stops.

The research results in this chapter have led us to the conjecture that both the SCC and CBB algorithms are members of a general class of methods which manage the energy delivery from power sources of various types to different types of loads by intelligently connecting and disconnecting multiple energy storage devices to and from the source and the load. For this general problem, a theory of SCC-CBB equivalences and a more intelligent control algorithm are waiting to be investigated and developed.

Chapter 6

Asynchronous Controller Design

6.1 Introduction

Previously, a *Capacitor Bank Block (CBB)* power delivery concept is introduced and compared with a conventional *Switched Capacitor DC/DC Converter (SCC)* working in an *Energy Harvesting (EH)* system. The research shows that CBB has advantages to regulate very limited and variable power directly from EH circuits for asynchronous loads without passing through traditional off-chip energy storage devices.

However, the CBB concept is still waiting for a sophisticated control method to form a feasible and practical on-chip *Power Delivery Unit (PDU)*. Additionally, the CBB is developed based on the concept of energy-modulated computing [22], in which the harvested energy will be partitioned into packets by employing the CBB according to tasks. Then each energy packet will be released to loads to finish one or a part of a task. In this case, theoretical relations between the power path and the task path need to be investigated. Moreover the CBB control is required to cooperate with asynchronous loads to implement a degree of task and power scheduling. The challenges still have not been solved by proper solutions yet.

On the other hand, since the CBB concept is especially for powering asynchronous loads, asynchronous method may also be employed to design a controller for the CBB PDU. In this case, the entire on-chip system (CBB PDU and loads) can get rid of global clocks and run in asynchronous way that has many advantages (introduced in Section 1.1, Chapter 1). However, the asynchronous controller for the CBB PDU is still waiting to be developed so far.

Although the research is not focused on the on-chip voltage sensing techniques, it is still relevant to the research. The voltage sensing for the CBB PDU working in EH systems is still looking for appropriate solutions. Since the power is very

limited from the harvesting circuits, incorporating traditional on-chip voltage sensing circuits may not have advantages due to large power consumption and requiring extra effort for generating voltage references.

In this chapter, the CBB PDU is optimized in order to work with an asynchronous controller cooperating with asynchronous loads to implement preliminary task and power scheduling. The CBB PDU optimization is also for working with threshold voltage sensing circuits that are optimized. An asynchronous control method is developed and corresponding **Signal Transition Graphs (STG)** are presented and discussed.

For the controller verification, a variable Vdd is applied on the CBB PDU to verify its power delivery performance. Vdd variation tolerance ability of the CBB PDU is crystallized and discussed. The power consumption of the entire CBB PDU is shown in term of working with different switching frequencies.

An option, using commercial long-life miniature alkaline batteries to independently power the CBB PDU in the EH systems, is investigated. The estimated operation life versus the CBB switching frequencies is presented as a reference for practical applications. Powering the CBB PDU using the independently power supply, the EH systems may be further simplified and miniaturised. Additionally, almost all harvested energy will be delivered to loads without sharing a part with controllers.

A case study has been done by discharging a standard energy packet to an asynchronous load using **Capacitor Banks (CB)** inside the CBB with different capacitance values and discharge ranges. Based on the case study, a preliminary task and power scheduling method is developed.

6.2 CBB PDU Optimization

In this section, the CBB PDU is optimized to develop a preliminary asynchronous controller that is able to cooperate with loads to implement a degree of task and power scheduling. The PDU optimization is also for the CBB PDU cooperating with voltage sensing circuits.

6.2.1 Structure Optimization

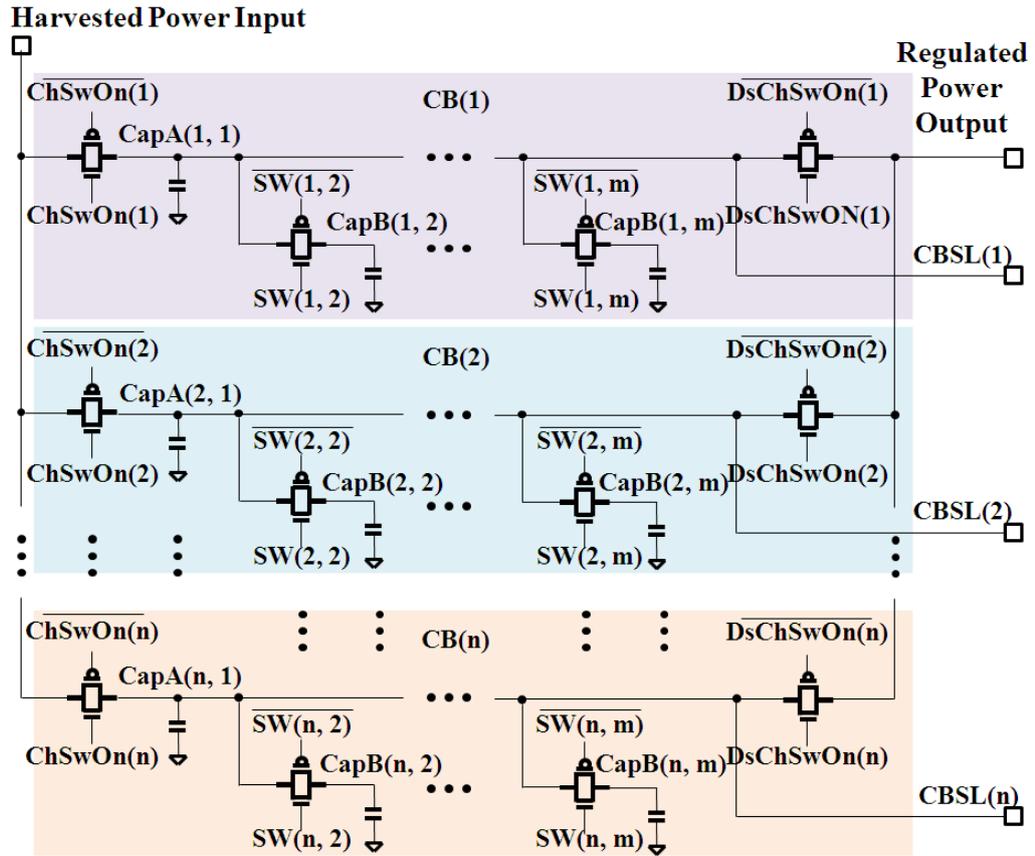


Figure 43. CBB structure optimization for capacitance value adjustment on each CB ($2 \leq n < \infty$ and $2 \leq m < \infty$, n and m are integers).

Figure 43 shows an optimized CBB structure. The structure only has one harvested power input and one power output. It has n CBs. In order to implement continuous power delivery, the CBB should have at least two CBs. For each CB, it has one **Capacitor Bank Sense Line (CBSL)** used to connect the CB to voltage sensing circuits. Signal $ChSwOn(n)$ and $DsChSwOn(n)$ are for CBB charge and discharge control respectively.

The $CB(n)$ is designed to have a basic capacitor $CapA(n,1)$ and it may have extra capacitors $CapB(n,m)$ connected in parallel to the $CapA(n,1)$. The $CapB(n,m)$ are switched by **Transmission Gates (TG)** and controlled by signal $SW(n,m)$. For each CB, the number of the $CapB(n,m)$ may be different. Therefore the value of m may be different in each CB. For the value of n and m , there is a trade-off in the power delivery flexibility and energy buffering ability versus chip area and fabrication costs. Thus, the more capacitors are fabricated, the larger on-chip area and higher cost will be.

- **Avoid Using Output Capacitors**

For traditional SCCs, large output capacitors are normally needed to filter output voltage ripples or non-power gaps caused by synchronized capacitor switching actions [191] [192]. Compared with SCCs, the proposed CBB structure may not need output capacitors. There are two reasons: 1) asynchronous loads have good capability in working with variable V_{dd} , and 2) due to incorporating an asynchronous handshake principle in the CBB switching control, the CBB is able to generate continuous output power without any non-power gaps. In this case, the CBB PDU design may be more economic in use of on-chip capacitors, as all on-chip capacitors are employed for energy buffering and delivery rather than being dumb capacitors for filtering.

6.2.2 Capacitance Value Adjustment

Figure 44 shows a control circuit for CB capacitance value adjustment. To adjust the CB value, a **D Flip-flop (DFF)** array $DFF(n,m)$ ($1 \leq n < \infty, 2 \leq m < \infty$) is used to open and close the TGs of the extra capacitors in each CB. Each DFF has two inputs. One is for signal **Capacitor Enable (CapEN)** sent from a task & power scheduler to control the TGs of the extra capacitors. Inside the task buffer, there will be the same number of CapEN blocks as that of CBs. Another one is for signal **Start Charge Process (StaChPro)** sent from a charge sequence control block to enable the DFF. StaChPro will be raised to High when the PDU starts to charge the corresponding CB and will be pulled down to Low at the end of the charge process. Therefore, the value of each CB only can be adjusted during its charge process. After charging the CB, the capacitance value is not allowed to be changed to guarantee the CB is able to deliver expected energy to loads.

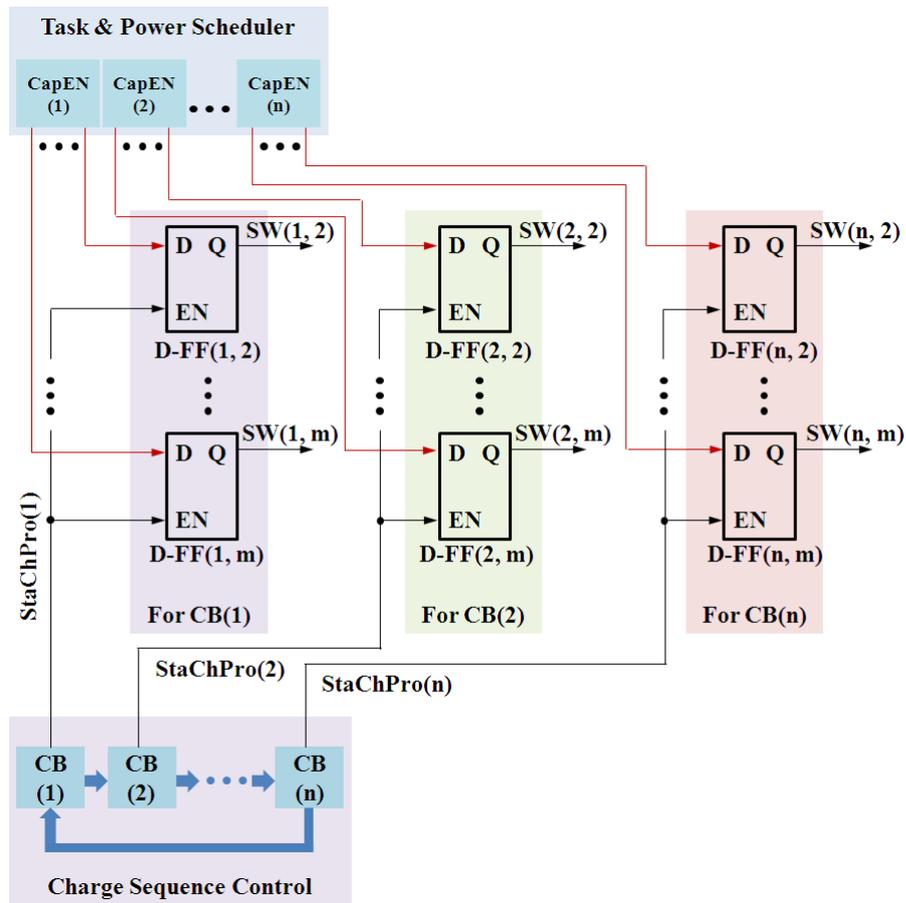


Figure 44. Task & power scheduler and charge sequence control block controlling connection and disconnection of extra capacitors inside CBs according ($2 \leq n < \infty$ and $2 \leq m < \infty$, n and m are integers).

In order to simplify the system, the extra capacitors $CapB(n,m)$ may be designed to have the same capacitance as the basic capacitor $CapA(n,1)$. Therefore, the capacitance value of a CB can be increased or decreased linearly.

6.2.3 Optimization for Voltage Sensing

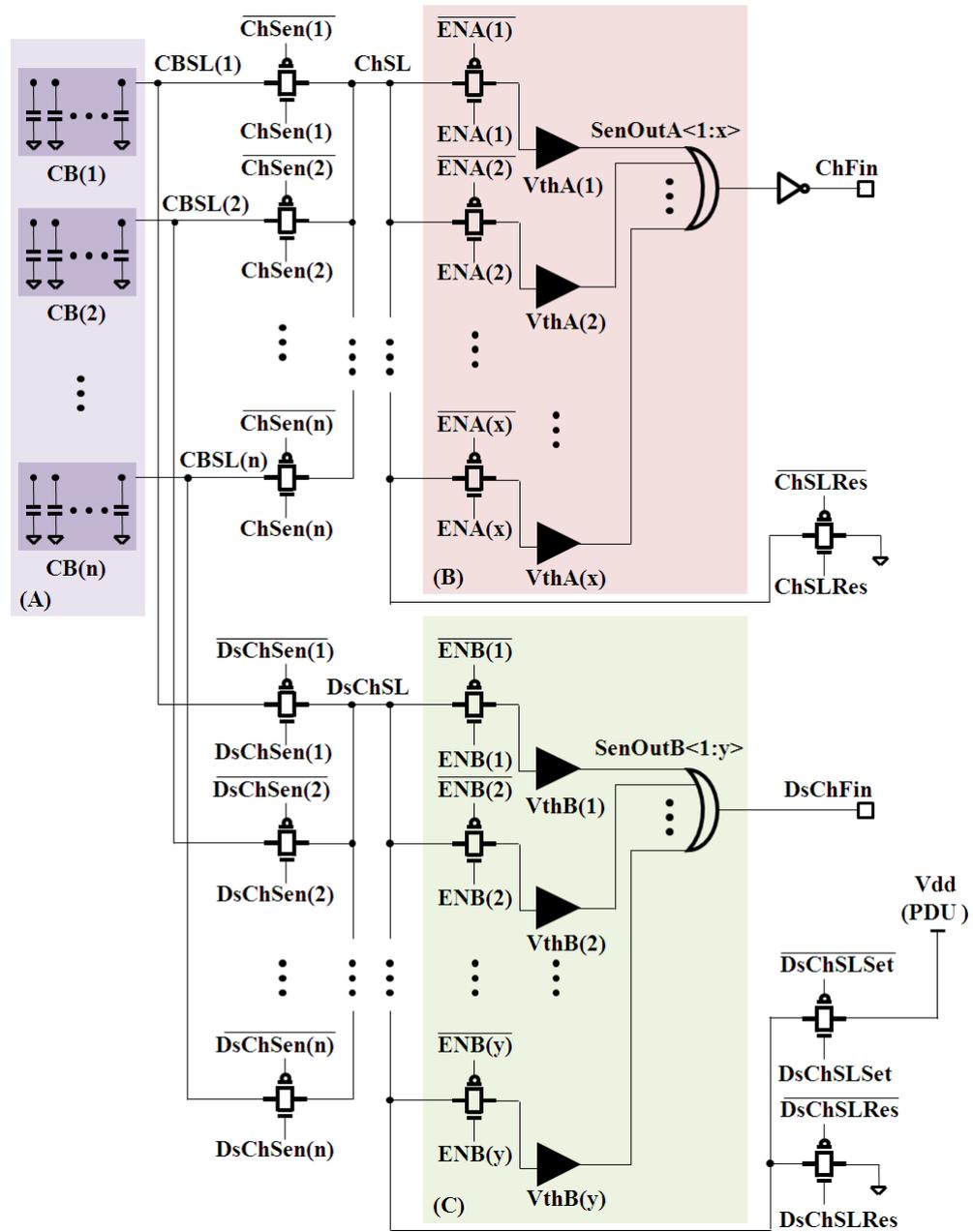


Figure 45. CBB structure optimization for voltage sensing. (A) CBB, (B) threshold sensing block for charge, and (C) threshold sensing block for discharge ($2 \leq n < \infty$, $1 \leq x < \infty$, and $1 \leq y < \infty$, n, m, x and y are integers).

Figure 45 shows the CBB structure optimization for voltage sensing. Each CB inside the CBB (A) has a CBSL connected to voltage sensing blocks for charge (B) and discharge (C). For (B) and (C), threshold sensing circuits that use intrinsic thresholds to sense fixed voltage levels are employed. The threshold voltage can be preset by adjusting width and length of transistors inside the circuits [193] [194] [195] [196]. In this case, the more thresholds can be sensed by the sensing blocks,

the more flexibility in power delivery the CBB PDU will have. However, it is also a trade-off between power delivery flexibility and circuit area.

In (B), threshold sensing circuits are used during charge process. The TGs inside (B) are controlled by signal ENA(x). When the threshold sensing circuit VthA(x) is selected by the task & power scheduler, the TG located between **Charge Sense Line (ChSL)** and VthA(x) will be switched on by the ENA(x). The outputs of these threshold voltage sensing circuits SenOutA(1:x) are connected to an OR gate with x inputs. After inverting the output of the OR gate, signal **Charge Finish (ChFin)** will be generated.

In (C), the same principle introduced above is employed. When the threshold sensing circuit VthB(y) is selected by the task & power scheduler, the TG located between **Discharge Sense Line (DsChSL)** and VthB(y) will be switched on by ENB(y). The output of these threshold sensing circuits SenOutB(1:y) are connected to an OR gate with y inputs. Then signal **Discharge Finish (DsChFin)** will be generated.

For voltage sensing in charge process, when a CB is selected to be charged, the task & power scheduler will set the corresponding signal **Charge Sense (ChSen)** to High to switch on the TG located between the CBSL of the CB and the ChSL. Therefore, the voltage level at the CB can be sensed by one of the threshold sensing circuits inside (B).

For the voltage sensing in discharge process, the same principle introduced above is employed. Signal **Discharge Sense (DsChSen)** is employed to control the TG located between the CBSL of the CB and the DsChSL. Thus, the voltage level at the CB can be sensed by one of the threshold sensing circuits inside (C).

Additionally, ChSL can be reset by signal ChSLRes. On the other hand, signal DsChSLSet and DsChSLRes are used to set DsChSL to High (CBB PDU Vdd) and reset it to Low respectively.

circuit is able to sense two different preset thresholds in V_{in} rising and falling processes respectively. Two inverters powered by the V_{dd} of the PDU controller are used to shift the voltage level of $porB$ for the controller.

In the threshold voltage sensing circuit study using UMC 90nm CMOS Technology in Cadence tool, the threshold sensing behaviour of the circuit is shown in **Figure 47**. In (A), V_{ref} is generated by the voltage divider. Two thresholds TH1 and TH2 can be sensed during V_{in} rising and falling periods.

However, in the V_{in} rising process, TH1 only can be sensed correctly when the V_{in} rises from “zero”. If the circuit is directly connected to a “non-zero” V_{in} , the output EN will be pulled up immediately to the same level of V_{in} regardless of whether V_{in} is higher than TH1, shown in **Figure 47** (B). After pulling EN to High, if V_{in} is still lower than TH1, EN will fall down to Low. As V_{in} continues rising and once the level is above TH1, EN will be pulled as high as V_{in} again.

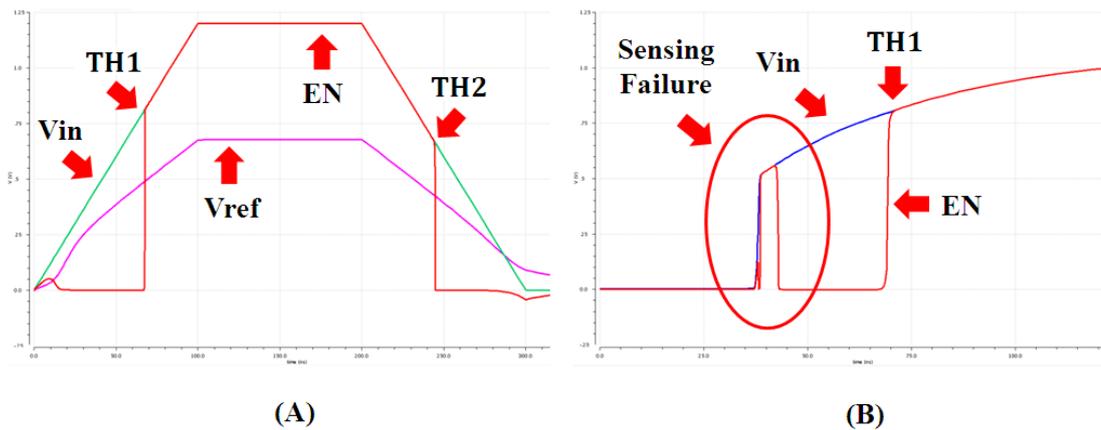


Figure 47. Threshold sensing behaviours: (A) able to sense two different thresholds in V_{in} rising and falling processes (TH1 can be sensed when the V_{in} rises from “zero”); (B) sensing failure happens when the circuit is directly switched to a “non-zero” V_{in} .

The sensing failure shown in (B) may not be solved easily by adjusting width and length of transistors inside the circuit. Since the width of p_{Cur} and p_{Buf} is preset much longer than their length [169]. When the POR circuit is directly connected to a “non-zero” V_{in} whose level is lower than the threshold of n_{Cur} and n_{Buf} , it is easy for charges going through p_{Buf} from the V_{in} , but it is hard for charges going through n_{Buf} to GND. Therefore, the charges accumulated between p_{Buf} and n_{Buf} enable the circuit to pull EN up to High. In this case, the circuit

shown in **Figure 46** may be only used to sense threshold during discharge process by the CBB PDU.

- **Threshold Sensing in Charge Process**

For threshold circuits sensing rising voltage levels, existing circuits introduced in Section 3.3.2, Chapter 3 may not meet the requirements of the CBB PDU, such as fast response speed, no “memory effect”, and correctly sensing a “non-zero” voltage source in its rising process. Therefore, an optimized threshold sensing circuit is developed and shown in **Figure 48**. In the design a voltage divider is employed to adjust sensing threshold. A buffer structure is borrowed from [166]. In order to effectively remove the “memory effect” from the circuit after each threshold sensing, V_{ref} and V_{buf} will be pulled down to Low by TGs employed for resetting. The TGs are controlled by signal $ChSLRes$.

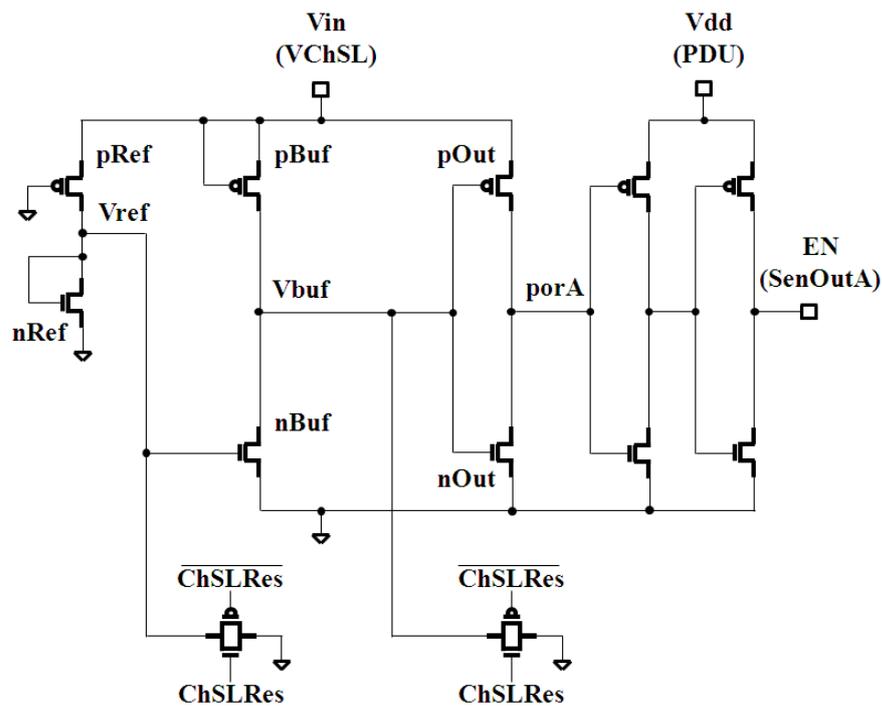


Figure 48. Threshold sensing circuit employed for sensing rising voltage level.

6.4 Asynchronous Controller Cooperating with Tasks

In the section, an asynchronous controller design is introduced. It is able to control the CBB to deliver adjustable and continuous power supply to loads and cooperate with loads to implement task and power scheduling. The asynchronous controller

is developed based on the basic method: sequentially charging and discharging the CBB. The controller may be improved by using more sophisticated methods.

A diagram of the CBB PDU is shown in this section and the function of control blocks inside the controller is discussed by using STG. EQN files of the control models (attached to Appendix C) are generated by using a Petriify asynchronous circuit synthesis tool [201]. According to equations listed on the EQN files, asynchronous circuits are generated by using complex gates [202].

6.4.1 General CBB PDU Structure

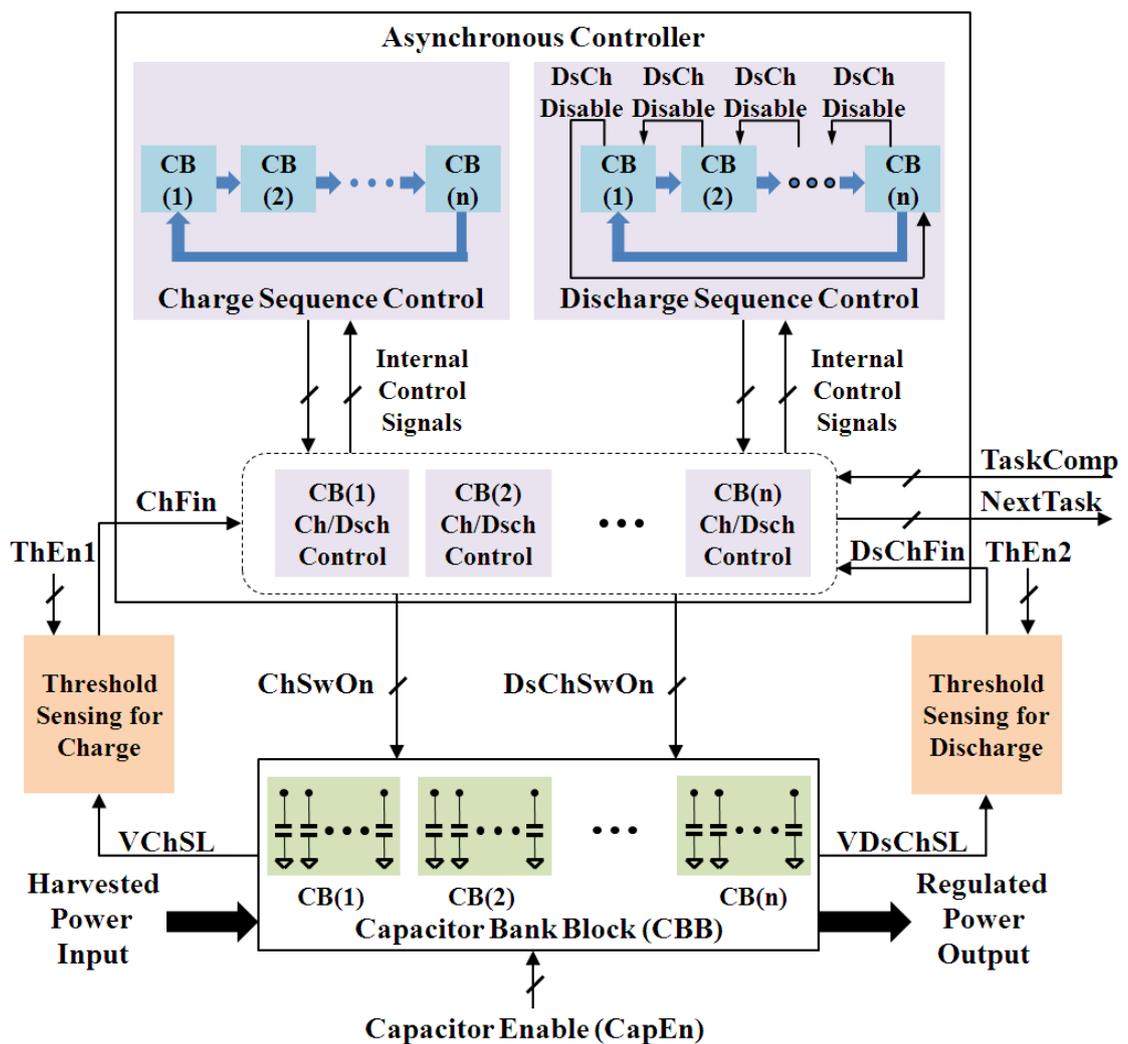


Figure 49. Proposed asynchronous controller working with tasks.

Figure 49 shows a diagram of the CBB PDU structure. For the proposed asynchronous controller, it mainly contains CB Ch/DsCh control blocks, one charge sequence control block, and one discharge sequence control block. The CBB is

controlled by the asynchronous controller. Each CB inside the CBB has its corresponding CB Ch/DsCh control block.

The CB Ch/DsCh control block is used to control charge and discharge of the CB by using signal ChSwOn and DsChSwOn. The CB Ch/DsCh control blocks also receive signal ChFin and DsChFin from two threshold voltage sensing blocks that are employed by the CBB PDU to sense voltage levels at the CBs in charge and discharge processes respectively.

- **Cooperating with Tasks**

The CBB PDU is able to cooperate with tasks. In the research, the tasks are assumed to contain two factors, computational amount and deadline. According to the factors, the task & power scheduler will employ 1) ThEn1 and ThEn2 to control CB charge and discharge range, 2) CapEn to adjust capacitance of CB for buffering demanded energy, and 3) TaskComp to inform the asynchronous controller the completion of the current task. On the other hand, the asynchronous controller will send signal NextTask to require a new task. Due to employing these control signals, coming task and harvested power can be scheduled according to the proposed method and the scheduled power delivery will be executed by the CBB PDU.

6.4.2 Asynchronous Control

For the CB charge and discharge control, a STG control model is shown in **Figure 50** (signal transitions with under line are inputs). In the model, there are two main control loops, one for charge control (A), and the other for discharge control (B).

For the charge control loop, it cannot start until SetDsChAv- is triggered by SetChAv- and DsChSwOn-. On the other hand, the discharge control loop cannot start until SetDsChAv+ is fired by ChSen- and NextPro-. Therefore, this method effectively enables the CBB PDU to avoid performing charge and discharge on a CB at the same time.

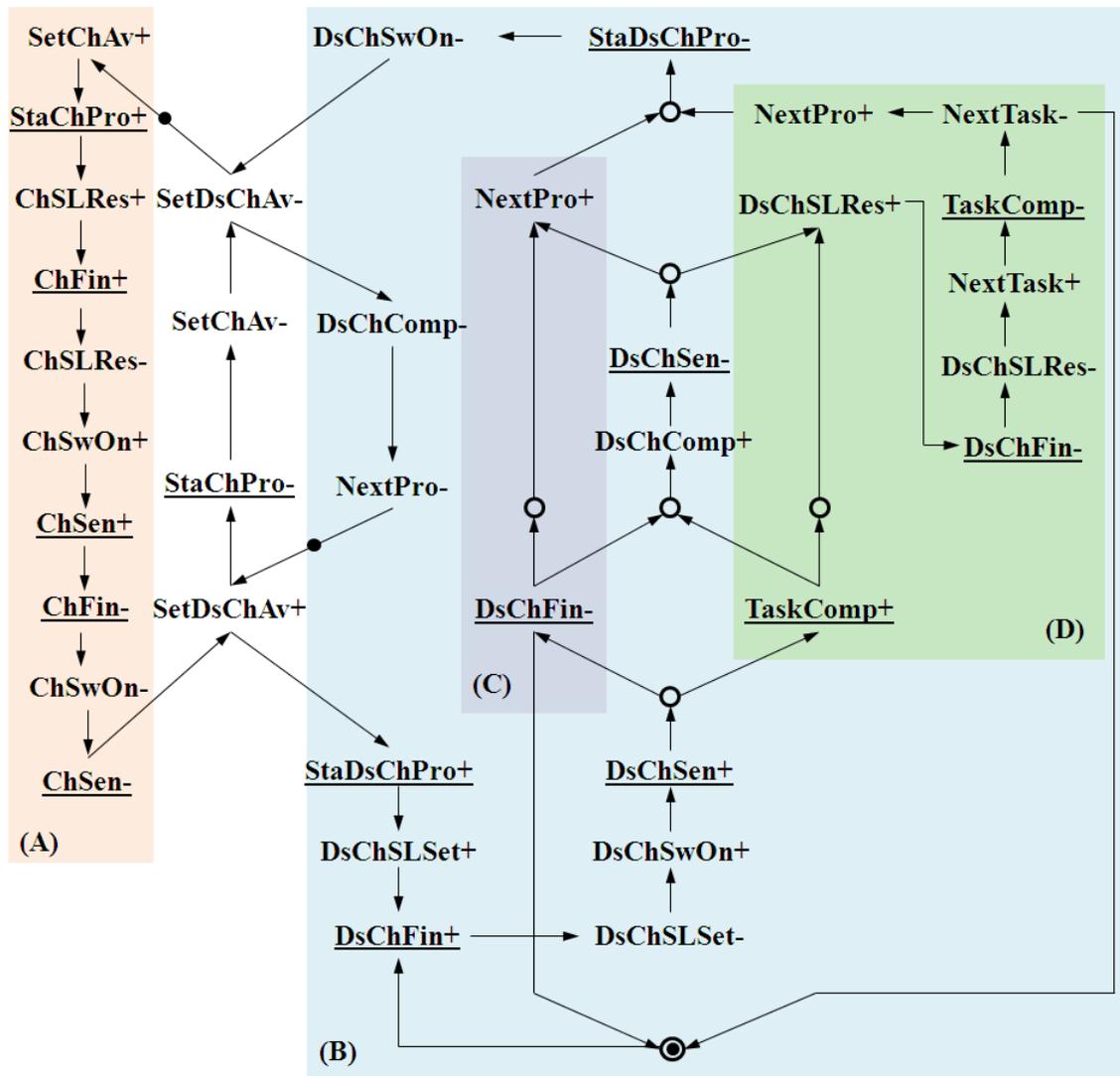


Figure 50. STG of CB Ch/DsCh control model (signal transitions with under line are inputs). (A) Charge loop. (B) Discharge loop. (C) Switching performed when low end of discharge range is reached. (D) Switching performed when present task is finished.

- **Charge Control**

In **Figure 50 (A)**, after the CBB PDU initialization, all CBs are labelled available for charge (**SetChAv+**). Then charge sequence control block chooses one of CBs inside the CBB to start charge process (**StaChPro+**) according to requirements of task and power scheduling.

Before enabling the charge switch of the CB, the **Charge Sense Line (ChSL)** will be reset to Low (**ChSLRes+**). Accordingly the output of the threshold voltage sensing block (for charge) will be pulled to High (**ChFin+**), as an inverter is used to invert the output (see **Figure 45**).

When ChSL reset is finished (**ChSLRes-**), the charge switch will be enabled (**ChSwOn+**). Then threshold sensing at the CB starts (**ChSen+**), connecting the **Capacitor Bank Sense Line (CBSL)** of the CB to the ChSL (see **Figure 45**). When the CB is charged to a target voltage level V_H (**ChFin-**), the charge switch will be disabled (**ChSwOn-**) and then the threshold sensing for charge process stops (**ChSen-**). The threshold sensing will only be enabled during the charge process to reduce the PDU energy consumption.

After completing the charge process, the CB will be labelled available for discharge (**SetDsChAv+**). Then **StaChPro-** and **SetChAv-** will be fired sequentially. And the charge loop shown in **Figure 50 (A)** may be repeated when the CB is discharged (**SetDsChAv-**).

In the CB charge loop, **ChSLRes+** is necessary. 1) When **ChSLRes** is set to high, the transition can be used to remove “memory effect” from the threshold sensing circuit for charge. 2) **ChSLRes+** can be used to help the CB Ch/DsCh control block avoid Stuck at “0” Fault for signal **ChFin** (output of the threshold sensing block for charge). When the target voltage level V_H (going to be achieved) is lower than the level at a discharged CB (going to be charged). In this case, **ChFin+** will never be fired. 3) **ChSLRes+** can prevent the sensing circuit from sensing failure caused by charges left on the ChSL after each threshold sensing.

CBs are charged sequentially and discretely (see STG of charge sequence control model in **Figure 51**). For example, only when the charge process performed on the

present CB(1) is completed ($\text{StaChPro-}(1)$), the next CB(2) is possible to be charged ($\text{StaChPro+}(2)$).

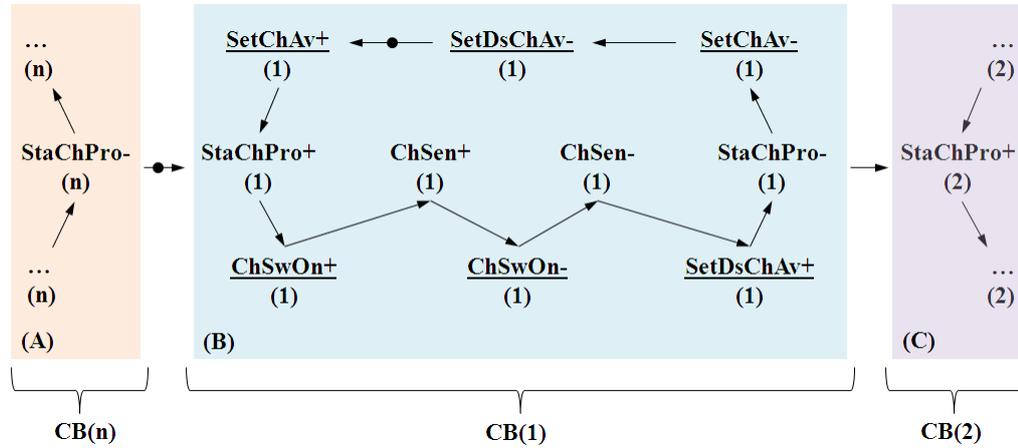


Figure 51. STG of charge sequence control model, (signal transitions with underline are inputs). In (A), (B) and (C), charge control loop for each CB is the same.

- **Discharge Control**

In Figure 50 (B), when one of CBs inside the CBB is available to be discharged (SetDsChAv+), once the discharge sequence control block decides to perform discharge on the CB (StaDsChPro+), the voltage level at the **Discharge Sense Line (DsChSL)** will be first set to High before the discharge process starts. The DsChSL will be set to High by connecting it to the PDU Vdd (DsChSLSet+). After the DsChSL is set to high (DsChFin+), signal DsChSLSet will be pulled down to Low.

In the CB discharge loop, transition DsChSLSet+ is necessary. The transition can effectively help the control block avoid Stuck at “0” Fault for signal DsChFin (output of the threshold sensing block for discharge) during the discharge process. When the charged CB is not used in time, the energy may leak off. In this case, the voltage level at the CB may be lower than the threshold of the selected sensing circuit for discharge. Thus, DsChFin+ will never be fired.

After DsChSL is set to high, the discharge switch of the CB will be enabled (DsChSwOn+) and energy stored in the CB will be released to loads. At the meantime, the TG located between the **Capacitor Bank Sense Line (CBSL)** and DsChSL will be switched on (DsChSen+). Thus, the being discharged CB is also connected to the input of the threshold sensing circuit (see Figure 45). During the threshold sensing process, two scenarios may cause the energy consumed by loads more than predicted: 1) task computation needs energy discharged from more

than one CB, and 2) load weight is increased during computation. In this situation, once voltage level at the CB reaches the low end of the discharge range (DsChFin-), the load will be switched to another charged CB (NextPro+) and the computation will be continued, shown in **Figure 50 (C)**.

On the other hand, since “conservative” energy consumption estimation strategy is applied for saving control and switching overhead of the controller, the energy delivered to the load will be slightly more than the demand based on the prediction. Therefore the task computation may be completed before the voltage level at the CB reaches the low end of the discharge range V_L . In this case, the asynchronous controller will be informed by the task & power scheduler (TaskComp+). Then the discharge sequence control block will be informed accordingly (DsChComp+), shown in **Figure 50 (D)**.

Since the voltage at the CB has not reached the V_L , transition DsChFin- will not be triggered. This will cause Stuck at “1” Fault for signal DsChFin when the next task computation starts. Therefore, after disconnecting the being discharged CB from the input of the threshold sensing circuit (DsChSen-), the DsChSL (still connecting the threshold sensing circuit) will be reset (DsChSLRes+) (see **Figure 45**), leading DsChFin- being triggered.

After completing the current task, the CB Ch/DsCh control block will require a new task (NextTask+) from the task & power scheduler and will inform the discharge sequence control block to prepare switching the loads to a charged CB to start a new task or maintain the computed data to wait for next task (NextPro+). DsChComp- and NextPro- will be fired sequentially and in parallel with charge loop to save transition time. The discharge loop shown in **Figure 50 (B)** may be repeated when the CB is charged (SetDsChAv+).

For discharge control, buffered energy in the CBB will be discharged from CBs sequentially and continuously. Incorporating asynchronous handshake logic in the control is able to avoid non-power gaps arising at the CBB output when the CB switching is performed. These gaps may cause the V_{dd} of loads dropping to GND and losing computed data.

The discharge sequence control model is employed to implement the asynchronous handshake logic for CB switching. Its STG is presented in Figure 52. The transitions shown in (E) are used to guarantee the CBB generating continuous output power without any non-power gaps.

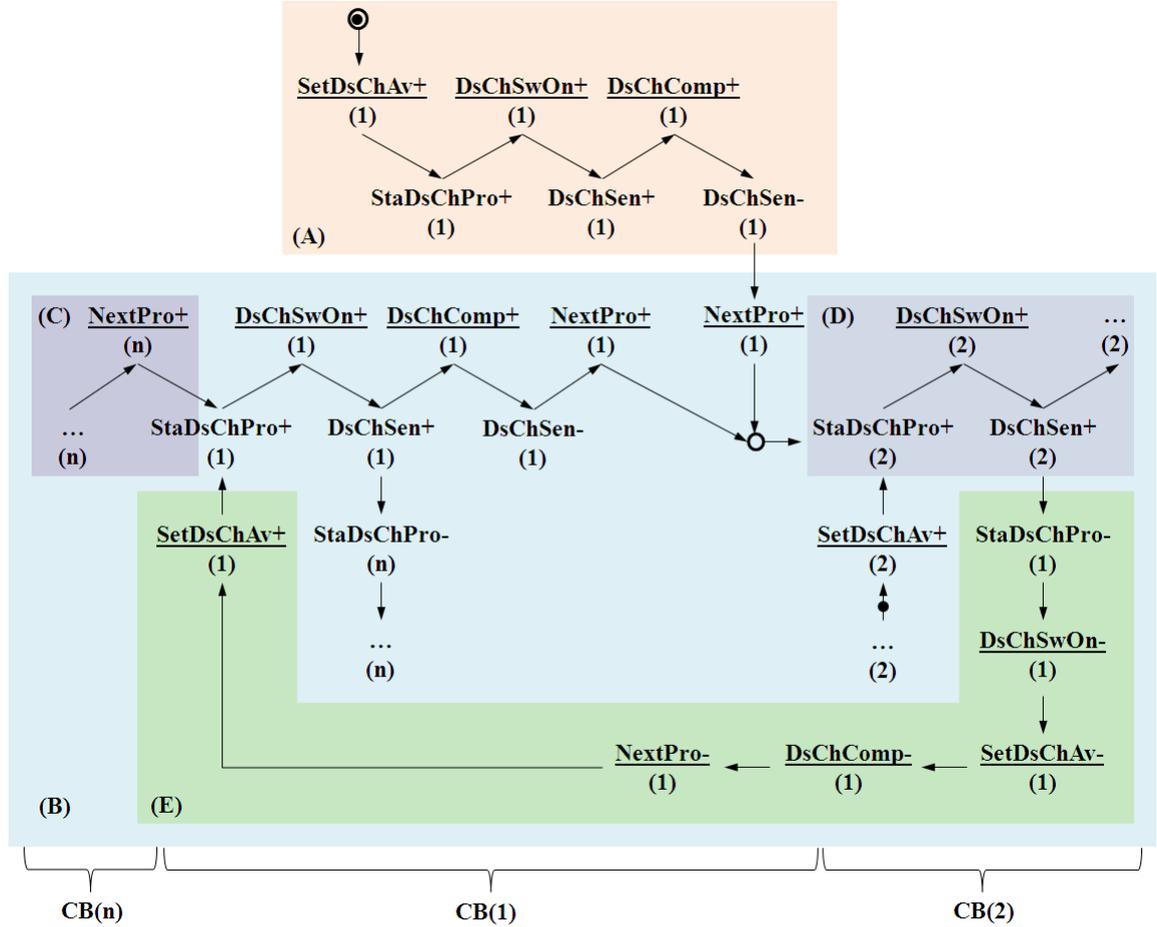


Figure 52. STG of Discharge Sequence Control model (Transitions with under line represent inputs). (A) Control discharge performed on the first CB after initialization. (B) Discharge control method. (C) and (D) Control for discharge performed on CB(n) and CB(2) respectively. (E) Guarantee continuous discharging power.

For example, only when the new charged CB(2) starts to discharge energy to loads (StaDsChPro+(2)), the discharge switch of the previous discharged CB(1) will be disabled (DsChSwOn-(1)). Then the previous discharged CB will be set as charge available (SetChAv+(1)) by firing transition SetDsChAv-(1).

6.5 CBB PDU Verification

In CBB PDU verification, the asynchronous control circuits are implemented by using Workcraft and Petrify. The PDU is built by employing UMC 90nm CMOS Technology library in Cadence. MIM capacitors from the same library are used for the CBB. The CBB has three CBs and each CB has 60 pf in total (one basic capacitor 20 pf and four extra capacitors 10 pf per each). Vdd of the PDU is set at 1 V. A stable voltage source 1.2 V is used as a power input for the CBB. A RC load is employed (1.5 KOhm, 1 pf).

6.5.1 Threshold Voltage Sensing

For verifying the asynchronous controller cooperating threshold sensing blocks, the PDU is set to regulate output power with discharge range from 1 V to 0.4 V.

- **In Charge Process**

Figure 53 shows control behaviours of the threshold sensing for charge. Two charge processes performed on CB(1) and CB (2) are shown. VChSL is the voltage level at the *Charge Sense Line (ChSL)*. ChFin is the output of the threshold sensing block. Vin is the voltage level at the input of the CBB.

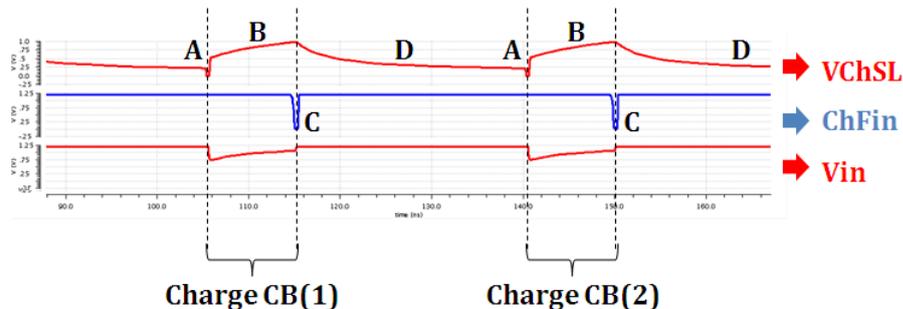


Figure 53. Threshold sensing for CB charge.

At the beginning of the charge process, the VChSL will be reset to Low to avoid Stuck at “0” Fault (introduced in Section 6.4.2 Charge Control), shown at Figure 53 A. After resetting, the ChSL will be connected to the CB(1) to start threshold sensing. The waveform of the CB(1) being charged by Vin is shown at B. When the VChSL rises higher than the threshold of the selected sensing circuit, the ChFin will be grounded, shown at C. Then the charge process ends and the ChSL is disconnected from CB(1). Since CB(2) and CB(3) are not available for charge (the former is in

use by loads, the latter has been charged), no threshold sensing for charge is performed. In this case, the ChSL is isolated from the CBB and the threshold sensing block. The charges at the ChSL left by previous threshold sensing will leak off slowly, shown at D.

- **In Discharge Process**

Figure 54 shows the control behaviours of threshold sensing for discharge. One discharge process performed on CB(1) is shown. V_{DsChSL} is the voltage level at the *Discharge Sense Line (DsChSL)*. $DsChFin$ is the output of the threshold sensing block. V_{out} is the voltage level at the output of the CBB.

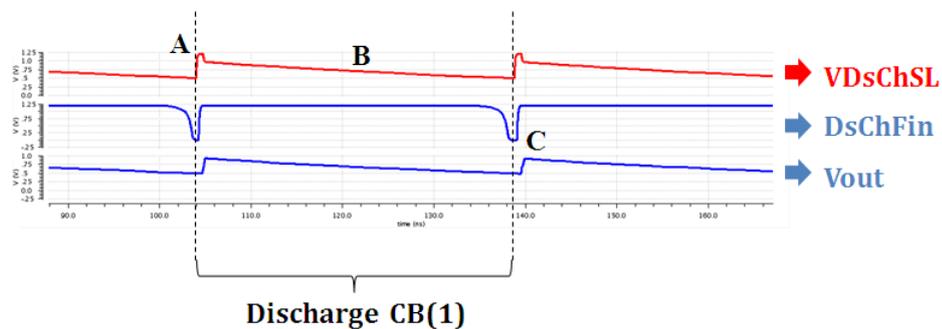


Figure 54. Threshold sensing for CB discharge.

To start discharge, the V_{DsChSL} will be set to High to avoid Stuck at “0” Fault (introduced in Section 6.4.2 Discharge Control), shown at Figure 54 A. Then the $DsChSL$ will be connected to the CB(1) to start threshold sensing. The waveform of the CB(1) being discharged is shown at B. When the V_{DsChSL} is lower than the threshold of the selected circuit, the $DsChFin$ will be grounded, shown at C. Then the threshold sensing process for discharging CB(1) ends.

6.5.2 Energy and Power Consumption of Threshold Sensing

V_{dd} of selected threshold voltage sensing circuits will be connected to the being sensed CB during voltage sensing processes for charge and discharge. The threshold voltage sensing for charge will start when the voltage level at the CB is raised to 0.4 V and end when the voltage level reaches 1 V. And the threshold sensing for discharge will be enabled when the CB is discharged and disabled when the voltage at the CB reaches 0.4 V.

- **Energy Consumption**

In the charge process from 0.4 V to 1 V, the power supply totally inputs 28.7 pJ energy to the CB (60 pF) and the sensing circuit for charge has drawn 0.33 pJ energy within 78 ns from the CB. After charge process, discharge is performed on the capacitor and threshold voltage sensing for discharge is enabled. The threshold sensing stops when 0.4 V is sensed. The sensing circuit for discharge has drawn 0.74 pJ within 66 ns from the CB. Therefore, the threshold sensing for charge and discharge in this case only consume 1.2% and 2.6% of the total energy coming from the power supply.

- **Power Consumption**

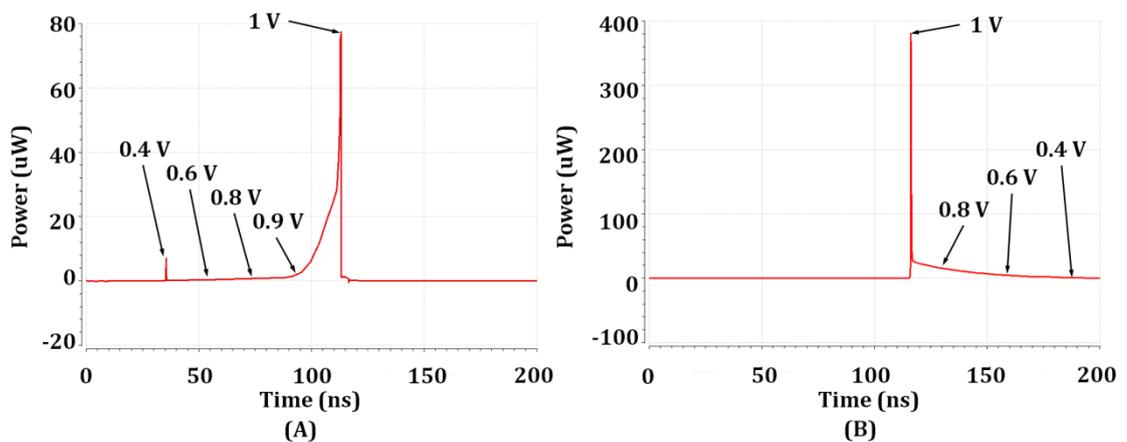


Figure 55. Power Consumption of threshold voltage sensing circuits for (A) charge (to 1 V) and (B) discharge (to 0.4 V) versus different voltage levels.

The power consumption of the threshold sensing circuits sensing 1 V for charge and 0.4 V for discharge is shown in **Figure 55**. For threshold sensing in the charge process, the sensing circuit has very low power when the voltage at CB rises from 0.4 V to 0.9 V. Then the power increases quickly. When the threshold 1 V is sensed, its instant power jumps to around 75 uW.

On the other hand, in the discharge process, when the sensing circuit for discharge is connected to the CB, its instant power jumps to around 370 uW, then it drops significantly to 40 uW. Until the threshold 0.4 V is sensed, the power of the circuit has been in very low.

Based on the investigation, the energy consumption of using threshold voltage sensing technique for the CBB PDU may be acceptable comparing the energy input from the power supply. However, since the research concentration is not focused

on voltage sensing techniques, there may be more low-power high-performance circuits available.

6.5.3 CBB PDU Working with Variable Vdd

In order to verify the performance of the asynchronous controller working with variable Vdd, the CBB PDU is supplied with a global Vdd varying in different ranges. The voltage waveforms of the output power supply regulated by the CBB PDU are recorded and analyzed.

- **Test 1: Global Vdd Variation Range Higher Than CBB Discharge Range**

Figure 56 shows the power delivery performance of the CBB PDU suffering Vdd variation and delivering power whose voltage range is lower than the Vdd variation range.

For (A), the PDU suffers light Vdd variation from 1.1 V to 1 V and the CBB works correctly and discharges power from 1 V to 0.4 V. Due to the intrinsic capacitance of the load, the high end of the discharge range is pulled down to 0.9 V. For (B), the PDU suffers medium Vdd variation from 1.1 V to 0.8 V. The performance of the CBB delivering power from 0.8 V to 0.4 V is still acceptable. For (C), the PDU suffers heavy Vdd variation from 1.1 V to 0.6 V. The signal transition speed inside the asynchronous controller varies largely caused by the serious and rapid Vdd variation. The charge and discharge switches cannot be controlled in time. Therefore working with heavy Vdd variation, it is hard for CBB PDU to regulate output power. However, in the whole process, the power delivered to the load is still continuous without stops.

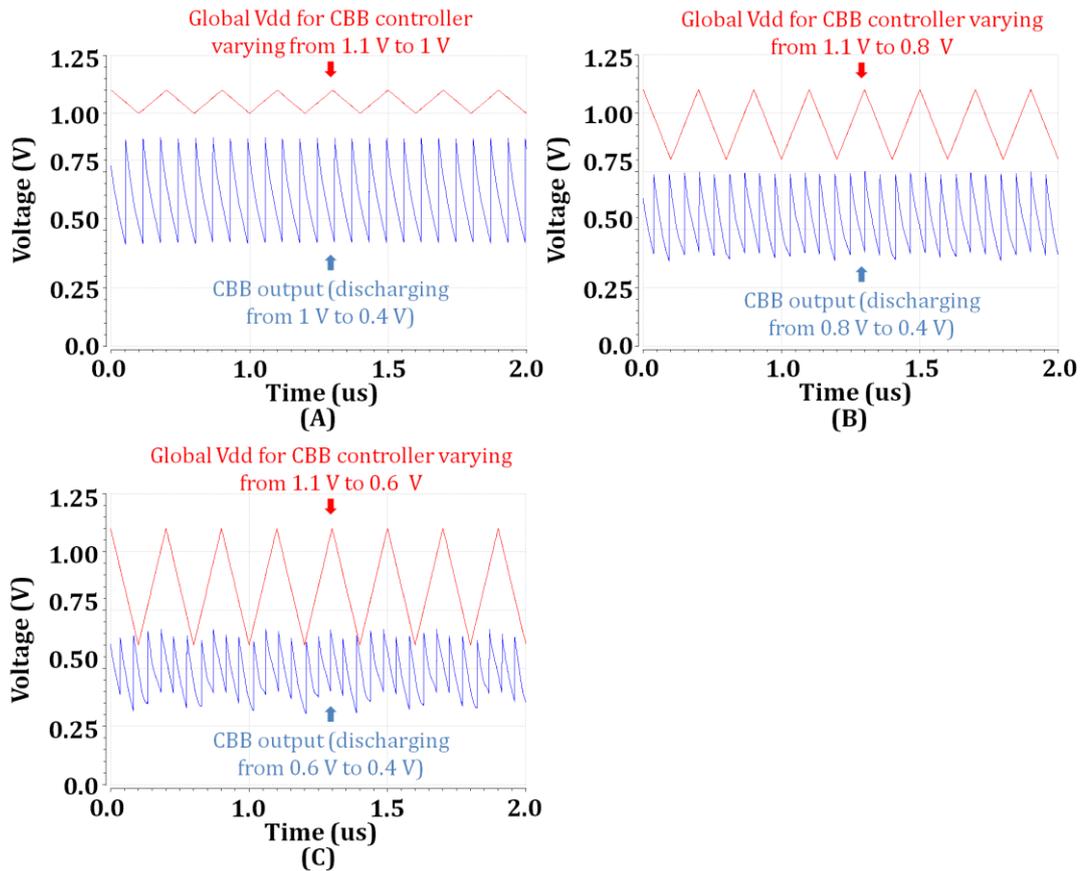


Figure 56. CBB PDU working with global Vdd (Vdd variation range higher than CBB discharge range).

- **Test 2: Global Vdd Variation Range Overlapping CBB Discharge Range**

Figure 57 shows the power delivery performance of the CBB PDU suffering Vdd variation and delivering power whose voltage range overlaps a part or the whole Vdd variation range.

In (A) there is a small overlapping between the Vdd variation range (from 1.1 V to 0.8 V) and regulated power range (from 1 V to 0.4 V). The CBB PDU still works correctly and is able to regulate power. In (B), there is a medium overlapping between the Vdd variation range (from 1.1 V to 0.6 V) and regulated power range (1.1 to 0.4 V). The CBB PDU shows weak power regulating ability. However, the power delivery is still continuous without stops. In (C) since the regulated power has the same variation range as that of Vdd, the CBB PDU fails to regulate output power due to various signal transitions inside of the asynchronous controller and not fully open or closed TGs inside of the CBB (working in low Vdd such as 0.4 V). How the signal transitions inside the controller, which works with low Vdd 0.4 V, are still correct. Although the CBB PDU is not good at working with Vdd that varies seriously and rapidly, it still shows a certain degree of Vdd variation tolerance.

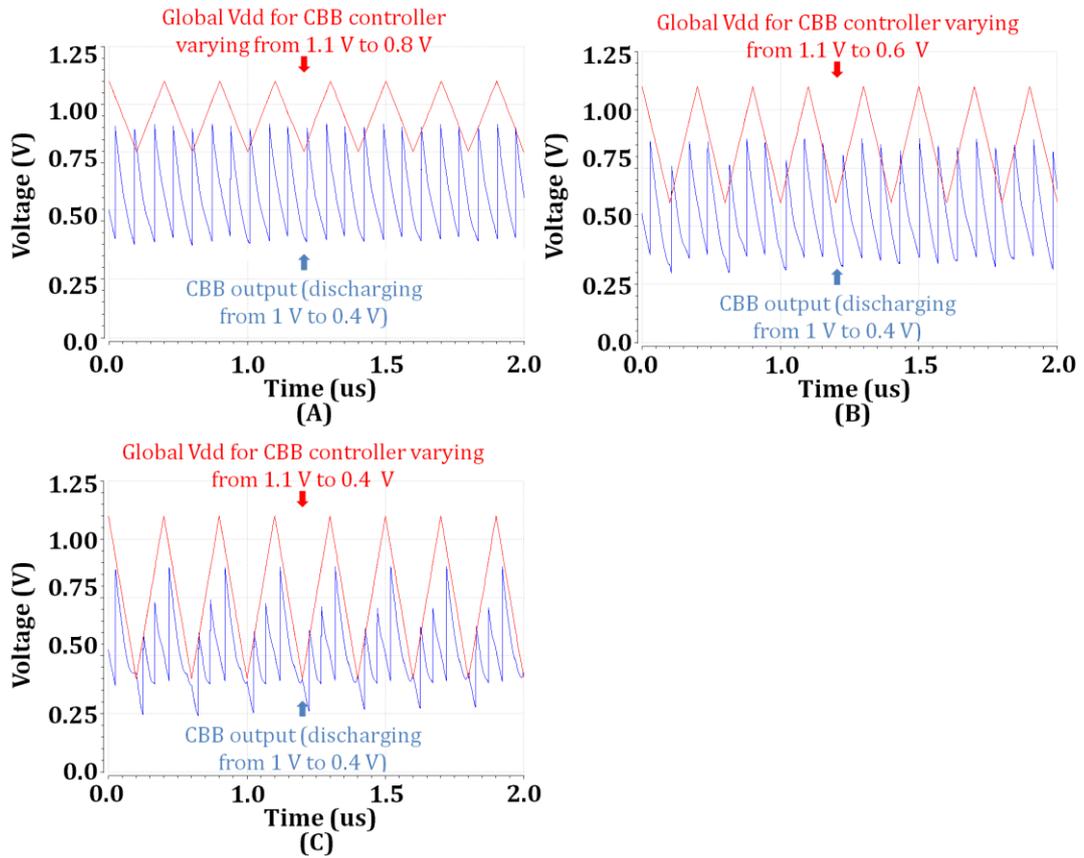


Figure 57. CBB PDU working with global Vdd (Vdd variation range overlapping CBB discharge range).

6.6 CBB PDU Powered by a Primary Battery for Energy Harvesting Systems

In this section, the power consumption of the CBB PDU working in different CBB switching frequencies is presented. The theoretically estimated operation life of the CBB PDU (independently powered by a primary battery) versus the CBB switching frequency is presented for a practical application reference.

6.6.1 Power Consumption of CBB PDU

- **Switching Frequency Range**

From recently published works, the switching frequency of on-chip SCC design is mainly in a range approximately from hundred KHz to 15 MHz [147] except [16] that is implemented with 45 nm CMOS Technology and employs 30 MHz switching frequency (details of the published SCC works are listed in Appendix D).

However, the CBB PDU may not need to achieve the switching speed as fast as SCCs to minimize voltage ripples at the output, as the CBB PDU is used to power asynchronous loads which have good voltage variation tolerance.

- **Power Consumption Vs Switching Frequency**

Figure 58 shows the CBB PDU average power consumption versus CBB switching frequency working with 1V Vdd. The average power consumption includes the power consumed by the asynchronous controller, voltage shifting for threshold voltage sensing signals, and TGs inside the CBB. Due to using asynchronous controller, the CBB switching frequency is totally adaptive to the load weight.

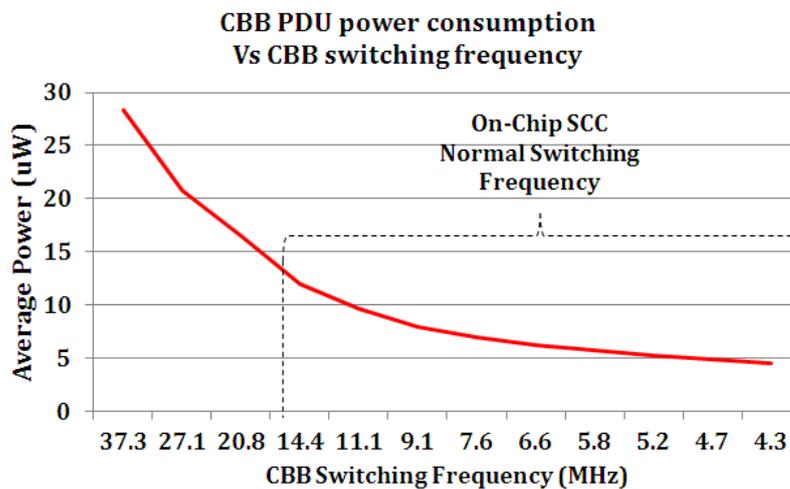


Figure 58. CBB PDU power consumption Vs CBB switching frequency working with 1 V Vdd.

In the simulation, the CBB PDU, discharge energy from 1 V to 0.4 V, is able to deliver output power from 77 uW (switching at 4 MHz) to 565 uW (37 MHz) to the asynchronous loads. If the PDU employs shorter discharge ranges starting from 1 V, the output power will be higher. As a longer discharge range from 1 V provides lower average output voltage than a shorter discharge range from 1 V.

6.6.2 CBB PDU Powered by a Primary Battery

As the design of the CBB PDU employs asynchronous control and threshold voltage sensing methods, the power consumption of the CBB PDU may be decreased efficiently. Therefore, the design may open an opportunity of using a miniature primary (non-rechargeable) battery to directly power the CBB PDU to achieve a long operation life.

- **Opportunities of Using Primary Batteries**

Since the harvested energy in harvesting systems is usually very limited, powering CBB PDU by a primary battery may guarantee the load obtaining maximum power and energy from harvesters. Although a very small part of harvested energy will be contributed for the threshold sensing, it may be considered negligible (introduced in Section 6.5.2).

Additionally, using a primary battery powering the asynchronous controller can avoid the use of a supercapacitor or rechargeable battery, and corresponding charge and discharge management circuits. This may further help the system to shrink the entire system size.

Compared with secondary (rechargeable) batteries, the primary batteries usually have higher capacity, lower self-discharge rate (alkaline 2-3 %per year, lithium 10% in five years), much longer shelf life (alkaline 7-10 years and lithium 10-15 years), and lower initial cost [91] [92]. The detailed review on batteries is presented in Section 2.3.1, Chapter 2.

- **Operation Life Estimation**

To theoretically estimate the operation life of the CBB PDU powered by a primary battery, miniature alkaline batteries from Energizer [207] are employed as examples, shown in **Table XII**. In this research, the alkaline batteries are assumed to suffer self-discharge 3% per year.

Figure 59 shows the operation life of the CBB PDU powered by the miniature alkaline batteries versus the CBB switching frequency. For E625, since it has lowest capacity, it can last almost two year if switching frequency of the CBB PDU is always kept at 15 MHz. Switching at this frequency, E96 can reach approximately seven years and E90 can support the PDU for more than seven years. For performing switching with the frequency lower than 5 MHz, the E625 is able to maintain the PDU operation for more than four years. However, for E96, performing switching with the frequency lower than 15 MHz may make the battery exceeds its design shelf life (7-10 years) with unspent energy stored inside the battery. This situation is the same to E90. In this case, lithium batteries with longer self-life (10-15 years) may be considered.

Table XII. Miniature alkaline batteries from Energizer.

Type	Voltage (V)	Capacity (mWh)	Weight (gram)	Volume (cm ³)
E625	1.5	210	3.3	1.2
E96	1.5	900	6.5	2.2
E90	1.5	1500	9	3.3

Battery capacity is measured in 21°C.

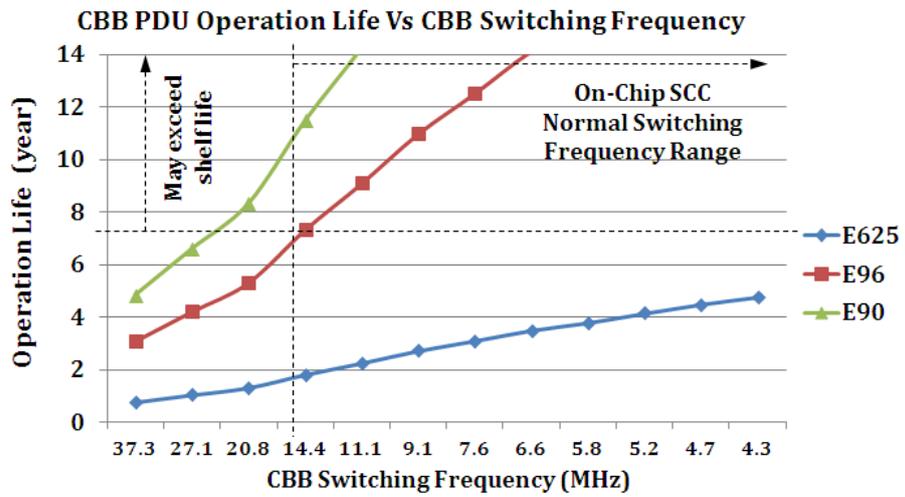


Figure 59. CBB PDU operation life Vs CBB switching frequency.

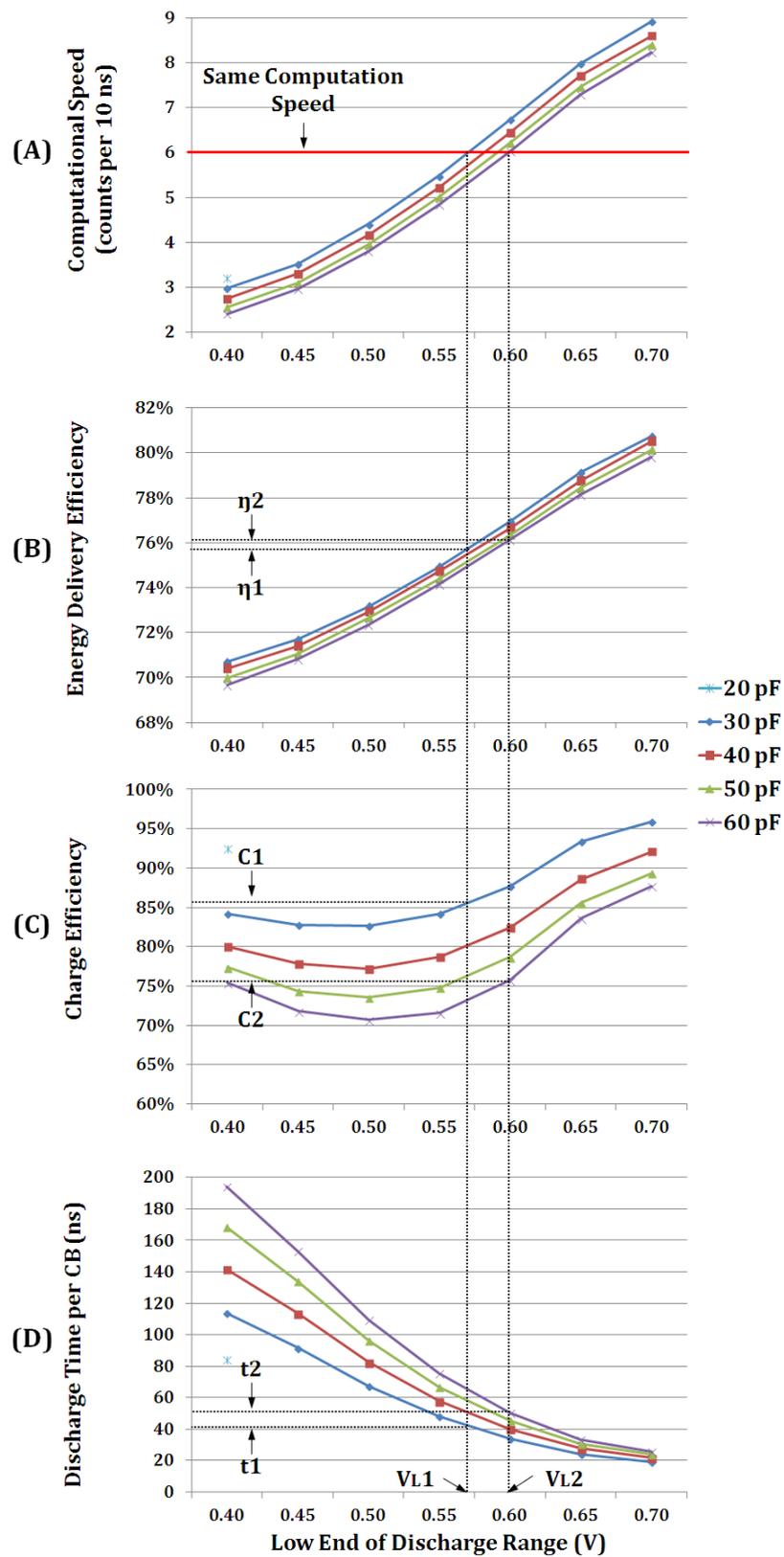


Figure 60. (A) Computational speed, (B) energy delivery efficiency, (C) Charge Efficiency, and (D) discharge time per CB versus discharge ranges releasing a standard energy packet.

6.7 Load Performance Investigation for Task and Power Scheduling Using CBB PDU

In asynchronous load performance investigation, harvested energy from harvesting circuit is temperately buffered inside the CBB. The buffered energy in each CB is considered as a packet that then will be released to asynchronous loads to finish a task or a part of a task.

- **Case Study of Load Performance Investigation**

For the load performance investigation, based on the optimized CBB PDU, the coming energy will be buffered by using CBs with different capacitance values (20 pf, 30 pf, 40 pf, 50 pf, and 60 pf). The energy discharged from the 20 pf CB with a discharge range 1 V to 0.4 V is considered as a standard energy packet in the investigation. The standard energy packet may be discharged in different ranges by these CBs to achieve different computational amount, computational time, energy delivery efficiency, and so on.

For analyzing impacts of discharging a standard energy packet in different discharge ranges to the loads, V_L the low end of the discharge range (0.4 V, 0.45 V, 0.5 V, 0.55 V, 0.6 V, 0.65 V, and 0.7 V) are preset for seven ranges. Since the energy of the standard packet is constant, according to the value of V_L and CB, V_H (the high end of the discharge range) can be calculated by using Equation (2). The calculation results of V_H based on different CB capacitance value and V_L are listed in Appendix E. For the loads, ten 16-bit asynchronous self-timed counters also implemented in Cadence with UMC 90nm CMOS Technology are used due to their good voltage variation tolerance and linear computational ability [34].

$$E_{st} = \frac{1}{2}CV_H^2 - \frac{1}{2}CV_L^2 \quad (2)$$

- **Performance Data Analysis**

Figure 60 shows the simulation results of computational speed, energy delivery efficiency, charge efficiency, and discharge time versus discharge ranges releasing the standard energy packet by CBs with different value. In (A), discharging the standard packet from a 30 pF CB from V_{H1} to V_{L1} (Combination 1) or from a 60 pF

CB from V_{H2} to V_{L2} (Combination 2) to the loads can achieve the same computational speed (6 counts per 10 ns). In (B), these two discharge combinations can make the CBB to achieve around 76% energy delivery efficiency (delivered energy versus input energy of the CB). η_1 of the Combination 1 is slight lower than η_2 of the Combination 2. However, in (C), there is a large difference in charge efficiency (energy of the standard packet versus input energy used to raise the voltage level from V_L to V_H on the CBs). The Combination 1 using smaller CB (30 pF) obtains higher charge efficiency C_1 in 85%. The Combination 2 only has 75%. In (D), Combination 1 has shorter discharge time t_1 releasing a standard packet (40 ns). And Combination 2 consumes 50 ns to complete discharging.

Combination 1 and 2 both can be employed to complete a task that requires a computational speed (6 counts per 10 ns). However, Combination 1 having higher charge efficiency thus uses less harvested energy to achieve a standard packet. This is more efficient in harvested energy use. On the other hand, Combination 2 having longer discharge time makes the CBB switching in lower frequency and the CBB PDU will consume less energy drawn from the power supply (long-life miniature battery). Thus, employing Combination 2 will enable the PDU to have longer operation life, but lower harvested energy use.

- **Task and Power Scheduling Method**

Based on the simulation data, a task and power scheduling method for CBB use is developed and shown in **Figure 61**. For completing a task that may contain computational amount and deadline, the average computational speed can be calculated. To simplify the problem, only these two factors are considered for tasks in this research. More factors can be employed for more advanced methods.

Based on the average computational speed, the optimization of power delivery scheduling will be performed through block (A), (B) and (C). In (A), combinations of CB capacitance value and discharge ranges used to achieve the required computational speed will be listed based on previous investigated data. Additionally, according to the discharge ranges, discharge time (t_1 to t_n), which decides the switching frequency of the CBB PDU, can be calculated. Then the voltage range from the present voltage level (V_0) at the CBs to the high end of the discharge range (V_H) will be calculated, shown in (B). In (C), to raise the voltage

level from V_0 to V_H , charge efficiency (C_1 to C_n) and charge time should be considered. Since V_0 may not be right equal to the low end of the discharge range (V_L), the charge efficiency may be different. In this case, the energy difference ($E\Delta$) that will be accumulated from V_0 to V_L will also be calculated.

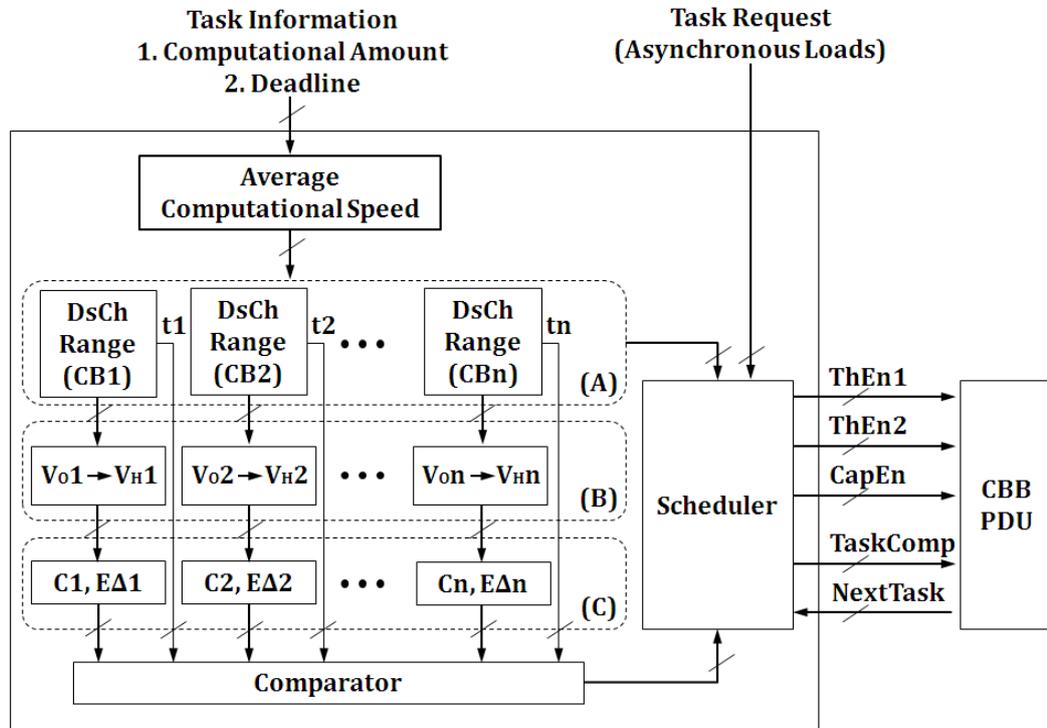


Figure 61. Task and power scheduler for CBB use.

Additionally, the PDU are required to have a certain degree of harvested energy prediction ability to estimate the charge time. There are lots of factors impacting charge time estimation. This goes beyond the research of the chapter and it will be considered as future work.

A comparator is used to choose a most appropriate combination from (C) for high efficient harvested energy use (considering charge efficiency C_1 to C_n) or long CBB PDU operation life (considering discharge time t_1 to t_n). According to the result from the comparator, a scheduler will apply corresponding control signals on the CBB PDU including $ThEn_1$ and $ThEn_2$ for threshold sensing in charge and discharge processes, $CapEn$ for CB value adjusting. Additionally, signal $TaskComp$ and $NextTask$ are employed for communicating the asynchronous controller (see Figure 49).

For the scheduling method introduced above, it is not only limited at implementing optimization in harvested energy use and CBB PDU operational life. Based on the scheduling model, optimization also can be performed on energy delivery efficiency or even combination of several factors. Therefore, more complicated scheduling method may be developed and the preliminary asynchronous controller and scheduler of the CBB PDU may also be improved or replaced accordingly.

6.8 Summary and Conclusions

In order to make the CBB concept introduced in Chapter 5 to be feasible for practical applications, an asynchronous controller is developed and has ability to work with tasks. Due to powering asynchronous loads, the entire EH system may get rid of clocks to obtain advantages in power consumption and operation speed. For the controller design, each block inside the asynchronous controller is introduced by using STG. The principle of the controller working for task and power scheduling is also introduced in details.

Optimization of the CBB structure has been done in order to cooperate with the asynchronous control and voltage sensing. The capacitance value adjustment enables the controller to implement finer and more flexible power delivery.

Working for EH systems, the voltage sensing circuits may need to be kept as simple, effective, and energy economic as possible. In this case, threshold voltage sensing technique is employed for the CBB voltage sensing. The threshold sensing circuits are optimized to better meet the requirements of working for the CBB PDU in terms of fast response speed, no “memory effect”, and correctness. The power consumption of the threshold sensing circuits for charge and discharge is presented. Compared with the energy stored inside the CBB, the energy contributed for threshold sensing may be negligible.

To verify the performance of the asynchronous controller, a variable global Vdd with different variation ranges is applied on the CBB PDU. The impacts of the variable global Vdd on the output power regulated by the CBB PDU are reported and discussed. It provides a reference for further CBB PDU applications.

Due to employ the asynchronous control method and the threshold voltage sensing technique, the power consumption of the entire CBB PDU is decreased effectively. Therefore, it may open an opportunity to use a primary (non-rechargeable) battery independently powering the PDU to achieve a long operation life. In this case, the almost entire harvested energy from the harvesting circuits can be used by loads. At the same time, it also may maximize the power of the loads for computations without giving a part to the CBB PDU.

To support the CBB concept, asynchronous load performance is investigated. Based on the investigated data (such as computational speed, energy delivery efficiency, CB charge efficiency, and discharge time), a preliminary task and power scheduling method is developed. This method is able to find an appropriate combination (CB value and discharge range) for the CBB PDU to implement power delivery that enables the loads to finish tasks. At the same time, high harvested energy use or long CBB PDU operation life can be achieved by incorporating the method. However, for the task and power scheduling method based on CBB concept, it still has a great potential to be improved. This initial attempt in this research area may be just considered as a tip of an iceberg.

Chapter 7

A Hybrid Power Delivery Method

7.1 Introduction

Energy Harvesting (EH) techniques can be considered as an alternative solution for many battery or power grid based applications [208] [209]. In addition, on-chip power delivery designs are more and more popular for reducing device size. One of the most popular techniques is *Switched Capacitor DC/DC Converter (SCC)*. However, most on-chip power delivery designs are aimed at regulating power from off-chip energy storage devices, such as supercapacitors or rechargeable batteries [210].

For further size reduction in EH systems, off-chip energy storage and charging circuits may be bypassed and SCC may directly regulate power from EH circuits to power loads. However power from harvesting circuits may be unstable, varying in a large range or even sporadic. Using SCC to directly regulate unstable power from EH circuits is very difficult.

In [211], an on-chip medical implantable SCC (investigated in Chapter 4) was investigated in an extremely simplified EH system. There a piezoelectric EH circuit was employed. When energy from the EH circuit was abundant and varied in a small range, SCC enabled loads to achieve high computing speed by maintaining high voltage level. It is ideal for tasks with short deadlines.

However, it performed inefficiently and had to stop power delivery to accumulate enough energy, when energy from EH circuit was sparse and varied in a large range. For this reason, an on-chip *Capacitor Bank Block (CBB)* was developed. It has capacitors with different values. With on-chip voltage sensors (introduced in Section 3.3, Chapter 3), charged and discharged energy can be estimated and controlled. Therefore it can temporarily buffer the harvested energy. CBB is designed to power asynchronous loads, which can work in a large VDD

range (introduced in 1.1, Chapter 1), and are predicted to become more common by [212]. Once the energy is accumulated to a required level, a corresponding task may be executed. CBB showed obviously better capability to cope with sparse energy with large variations with potential as a platform for developing an energy-modulated task and power scheduling method (introduced in 1.1, Chapter 1). In this case, CBB and SCC both have their advantages and disadvantages and are therefore suitable for working under different system operating conditions.

To deal with different tasks with variable harvested power, the system may have a range of operation conditions and thus call for both CBB and SCC type power delivery. It is possible to build a power delivery system which contains separate SCC and CBB parts which can be switched in and out at run time, effectively realizing a kind of dynamic reconfiguration of power delivery. This intuitively implies system size and energy overheads. The size overheads are especially important as on-chip capacitors for energy storage tending to be huge compared to logic. A hybrid structure **Hybrid Capacitor Bank Blocks (HCBB)** using the same set of capacitors to form both CBB and SCC configurations which can be reconfigured at run time is proposed in this chapter.

In the chapter, the study of task and power scheduling with SCC and CBB is introduced. Advantages and disadvantages of employing SCC and CBB to power asynchronous loads are discussed. Based on the discussions, a new power delivery method using a hybrid structure which can be configured as SCC and CBB is developed. The circuit schematic and the working principles are presented and introduced. Besides, in order to verify the HCBB concept and its power delivery performance, the HCBB PDU is implemented by hardware. The HCBB control principle is developed and implemented on **Field Programmable Gate Array (FPGA)**. The power delivery behaviours of the HCBB are shown in terms of CBB mode, SCC mode, and mode switching between CBB and SCC modes during power delivery process. The energy delivery efficiency of the HCBB powering a RC load with different weight is investigated in terms of CBB mode and SCC mode for the HCBB characterization. Additionally the HCBB hardware is employed for asynchronous chip testing. The results of the testing chip working in CBB mode and SCC mode are also shown.

7.2 Task and Power Scheduling with SCC and CBB

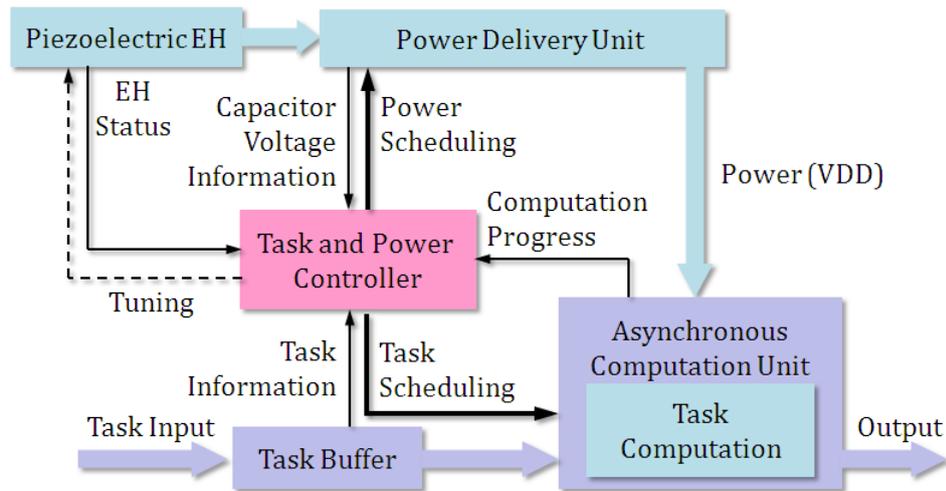


Figure 62. System structure of task and power scheduling method for asynchronous loads in energy harvesting systems.

Figure 62 shows a system directly powered by an EH circuit [211]. The system is designed to process tasks according to task priority and power scenario. Tasks with different priorities are assumed to arrive and be stored in a task buffer. According to task and power information, the controller produces power and task scheduling solutions to *Power Delivery Unit (PDU)* and a computation unit respectively. The computation unit implements priority-based task computation by selecting specific tasks from the task buffer according to the task scheduling results and energy limitation. Additionally, the computation unit is assumed to be able to activate multiple loads to implement multi-task computation in parallel.

In this study, SCC and CBB (with the same total capacitor value) are used as PDUs. 12-bit self-timed counters [34] are used as the load. Simulations are performed in Cadence toolkits with UMC 90nm CMOS technology library. Three task categories with high, medium and low priorities are used to model a system with simple task differentiation.

The SCC shows a good ability to deliver high power at a stable high Vdd when dealing with high priority tasks. However, when capacitors are empty it needs a long time to accumulate enough energy to raise output voltage to 1 V (the nominal Vdd for the technology) before the load can start.

In the CBB, charging a single capacitor to 1 V is much quicker. Therefore it enables the load to start computation quickly. However, by definition the CBB method results in more variable Vdd than SCC and requires a more complex control method to maintain some degree of Vdd stability at high Vdd, which usually means frequent switching with high control overheads. Thus CBB is not a good choice for high priority tasks. However, for processing medium and low priority tasks, which needs low Vdd for high efficiency and can tolerate Vdd variance, CBB performs better than SCC in terms of energy efficiency and load performance. When SCC has to perform step-down conversion to deliver a low Vdd, each switching performed by SCC requires switching almost all switches, leading to higher control overheads and lower energy delivery efficiency. If the PDU can work as a CBB when low and variable Vdd is fine and an SCC when high and stable Vdd is needed, the system may work better.

7.3 Hybrid Capacitor Bank Blocks (HCBB)

Figure 63 presents an HCBB structure. It has one power input and one power output. It contains two symmetrical blocks (the same switches and capacitors). Each block has four switched capacitors and 17 switches. In Block 1, the relationship of capacitance values of CA1, CA2, CB1 and CB2 is shown in Equation (3). IN0, IN1, IN2, IN3 are input switches and OUT is an output switch. In Block 2, the relationship of capacitance values of PCA1, PCA2, PCB1 and PCB2 is the same as that in Block 1.

$$2C_{CA1} = 2C_{CA2} = C_{CB1} = C_{CB2} \quad (3)$$

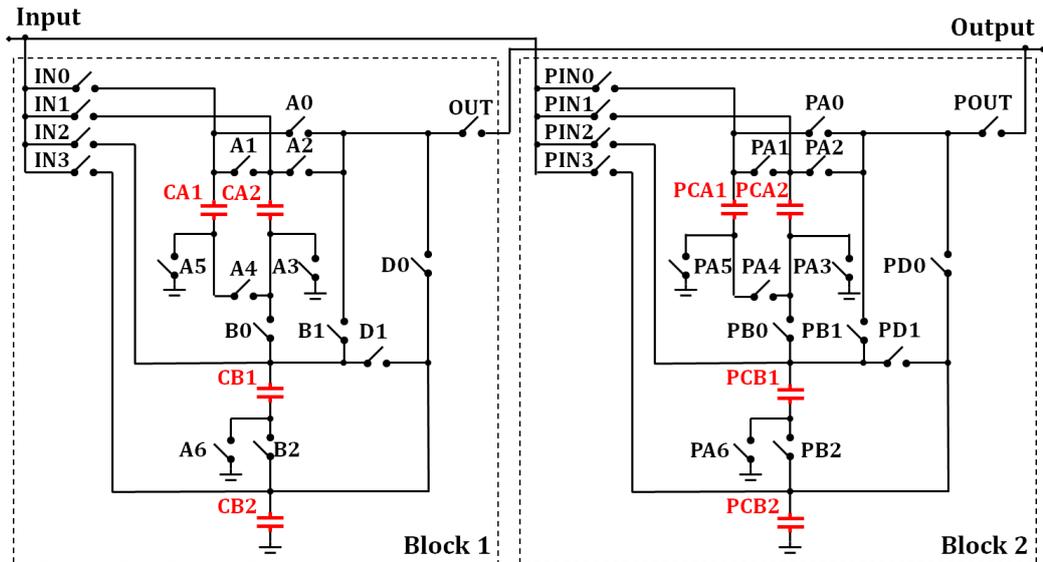


Figure 63. Hybrid capacitor bank blocks structure.

Figure 64 describes various connection topologies available for both Block 1 and Block 2 to implement CBB and SCC modes for power delivery. Since the structure of the Block 1 and the Block 2 are symmetrical, the connection topologies for both blocks are the same. Therefore only the topologies for Block 1 are shown.

When the topology in (A) is applied on both Block 1 and Block 2, HCBB is in CBB mode. In this case, all switched capacitors inside the HCBB structure are connected in parallel. The four smaller capacitors (CA1, CA2, PCA1 and PCA2) and four bigger capacitors (CB1, CB2, PCB1 and PCB2) can be charged or discharged individually.

The topologies shown in (B), (C), (D), (E), (F) and (G) are employed to implement SCC modes. Four step-down conversion ratios ($1/1$, $2/3$, $1/2$ and $1/3$) can be achieved by performing corresponding topologies on Block 1 and Block 2. Principles of implementing these four step-down conversion ratios can be found in [147]. From (B) to (E), the smaller capacitors (CA1 and CA2) are always connected in parallel to ensure that the total capacitance value of the pair (CA1 and CA2) is equal to that of each bigger capacitor (CB1 or CB2). For (F) and (G), only bigger capacitors CB1, CB2, PCB1 and PCB2 are used (also see Equation (3)).

When the topology (B) is used for both charge and discharge performed on the Block 1 and 2, the HCBB can implement $1/1$ conversion ratio in the SCC mode. For topology (B) applied on the Block 1, switches A0, A1, A4, B0, and B2 need to be enabled. IN0 and OUT are used to control input and output of the block. Other

switches inside the Block 1 are disabled.

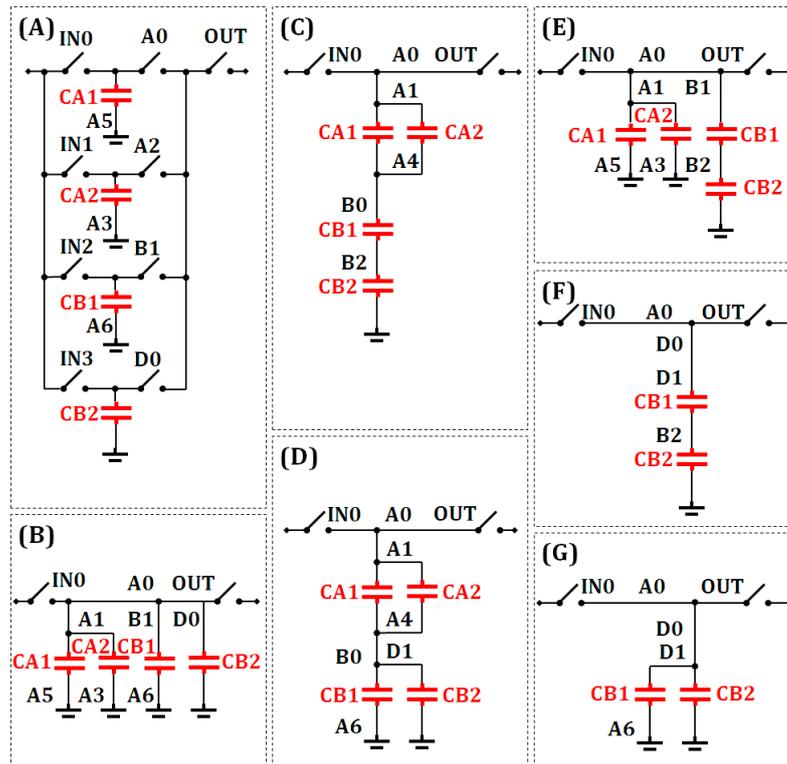


Figure 64. Different connection topologies for CBB and SCC modes (the topologies can be performed both on Block 1 and Block 2).

When the topology (C) is used for charge and topology (B) is used for discharge performed on the Block 1 and 2, the HCBP can implement $1/3$ conversion ratio. For topology (C) applied on the Block 1, switches A0, A1, A4, B0 and B2 need to be enabled.

When the topology (E) is used for charge and topology (D) is used for discharge, the HCBP can implement $2/3$ conversion ratio. For topology (E) applied on the Block 1, switches A0, A1, B1, A5, A3 and B2 need to be enabled. For topology (D) applied on the Block 1, switches A0, A1, A4, B0, D1 and A6 need to be enabled.

When the topology (F) is used for charge and topology (G) is used for discharge, the HCBP can implement $1/2$ conversion ratio. For topology (G) applied on the Block 1, switches A0, D0, D1 and A6 need to be enabled. For topology applied on the Block 1, switches A0, D0, D1 and B2 need to be enabled.

If the HCBP requires more choice in capacitor values, each capacitor used in the HCBP can be replaced by using more than one capacitor connected in parallel. And

the capacitor values are not necessary to be equal. As long as the total value of these capacitors for replacement is the same as that of the original capacitor. However, it can be considered as a trade-off in circuit leakage and control overhead versus power delivery flexibility.

7.4 Hardware Implementation

Figure 65 shows a system block diagram for verifying the HCBB concept and characterizing HCBB. Source supplies power to the HCBB PCB, which then delivers regulated power to the load. An FPGA development kit is used to control the PDU. Two ADCs are placed at the input and output of HCBB PCB respectively as voltage sensors.

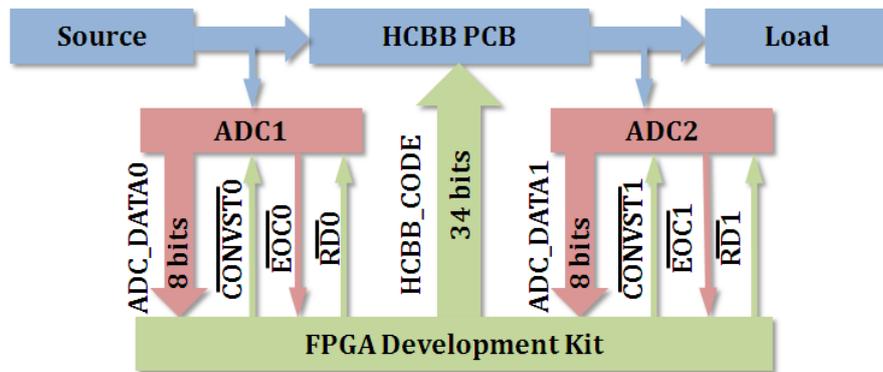


Figure 65. Whole implementation system.

For voltage sensing at input and output of the HCBB, the FPGA employs a polling method to control two ADCs to implement A/D conversion. Additionally, the ADCs are able to have different controllable sampling frequencies. By using $\overline{\text{CONVST0}}$ and $\overline{\text{CONVST1}}$, the FPGA controls the ADC sampling frequencies according to the speed of charge and discharge performed on capacitors inside the HCBB. Fast sampling frequency is required when HCBB needs very quick switching control in the scenario where loads are very heavy (maintaining an output voltage level or range) or input power is abundant (avoiding high input voltage damaging capacitors). When no task is computed in loads, discharge and ADC sampling at the output of the HCBB will be stopped. On the other hand, when all capacitors on HCBB are charged, charge and ADC sampling at the input of the HCBB will be stopped.

$\overline{\text{EOC0}}$ and $\overline{\text{EOC1}}$ are the conversion “done” signals. When A/D conversion is done,

EOC will be pulled down to GND. After finishing conversion, FPGA will use $\overline{RD0}$ and $\overline{RD1}$ to drive the output buffer of ADCs to send converted 8-bit data (ADC_DATA0 and ADC_DATA1) to the FPGA. Based on these values, the FPGA controls the behaviour of the HCBB in real time by using 34-bit control code (HCBB_CODE). A **Finite State Machine (FSM)** is implemented in the FPGA. The FSM contains two control units, one for SCC mode control and the other for CBB mode control.

The SCC FSM control unit is described in Section 3.2.2, Chapter 3. The main states are the initial accumulation of energy before power delivery, the maintaining of voltage during power delivery, the direct connection of load to source when charge on capacitors is low and returning to charging when voltage drops too far.

The concept of the CBB control is shown in Section 5.2.3, Chapter 5, in which CBB charges and discharges capacitors sequentially. The voltage level at a capacitor determines when charging and discharging should stop. Energy flows into the CBB through charging and to the load through discharging. The charging and discharging of particular capacitor sequences controls the energy flow.

7.4.1 HCBB Controller Implemented on FPGA

A functional block diagram of the HCBB controller implemented on FPGA is shown in **Figure 66**. The HCBB controller mainly contains four parts: 1) switch register block, 2) ADC blocks, 3) HCBB FSM blocks, and 4) HCBB control code block. *(Verilog HDL control codes developed for the FPGA are copied into a CD attached to the thesis.)*

- **Switch register block**

Eight slide switches on the FPGA development kit are used (see Appendix A, **Figure 81**). Switches 1 to 4 are employed as a 4-bit control signal (HCBB_MODE_SEL) to choose HCBB working modes such as SCC with different conversion ratios and CBB with different charge and discharge ranges. Switch 5 is designed to enable eight LEDs on the FPGA development kit (see Appendix A, **Figure 81**) to show converted data either ADC_DATA0 or ADC_DATA1 coming from two ADCs respectively. Switch 6 is employed to choose different ADC sampling frequency (FRQ_SEL). Switch 7 can enable or disable switches. The function of the Switch 7 is necessary

when the work mode of the HCBB (Switch 1 to 4) needs to be changed and manual control cannot control Switch 1 to 4 at the same time and avoid input signal jittering as well. After the switches 1 to 4 are reconfigured, the control signal (HCBB_MODE_SEL) will be renewed when the Switch 7 is set to “1”. Switch 8 is able to reset the controller by placing the switch to “0”.

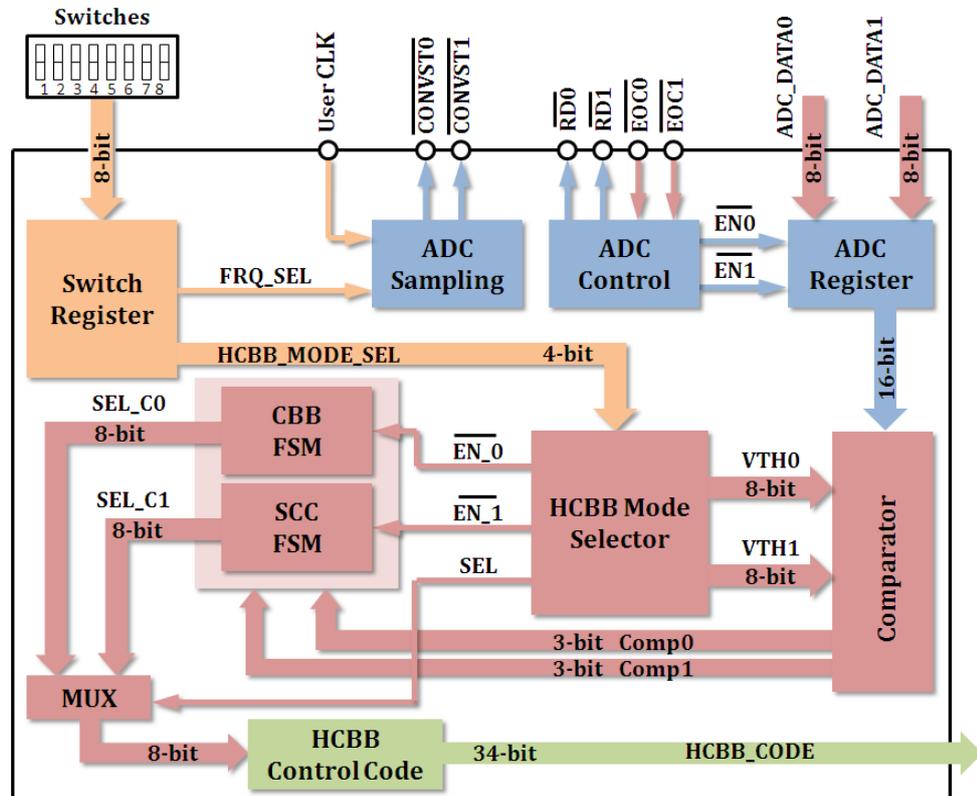


Figure 66. Functional block diagram of hybrid capacitor bank blocks controller.

- **ADC Blocks**

ADC blocks (ADC sampling, ADC control, and ADC register) are used for sampling voltage levels at input and output of the HCBB and reading converted data from the ADC buffers. By dividing the FPGA User CLK (100 MHz [213]) generated from the development kit, the ADC sampling block is able to generate sampling signals $\overline{\text{CONVST0}}$ and $\overline{\text{CONVST1}}$ with suitable frequency according to the rising and falling speed of the voltage at the input and output of the HCBB. ADC control block is used to control $\overline{\text{RD0}}$ and $\overline{\text{RD1}}$ to read converted data from ADC buffers. When the conversion processes are completed, $\overline{\text{EOC0}}$ and $\overline{\text{EOC1}}$ will be pulled down to GND immediately. Then $\overline{\text{RD0}}$ and $\overline{\text{RD1}}$ will be pulled down to GND to make the converted data ADC_DATA0 and ADC_DATA1 to be available at the output of the ADC buffers. After the completion of reading the converted data, the ADC control block will pull

$\overline{EN0}$ and $\overline{EN1}$ down to GND to store the converted data into the ADC register. And these two signals will be pulled up to High before the end of reading process ($\overline{RD0}$ and $\overline{RD1}$ are placed to High).

- **HCBB FSM Blocks**

HCBB mode selector is used to select one of the HCBB working modes (SCC and CBB) according to the signal (HCBB_MODE_SEL) from the switch register. The HCBB mode selector is designed to send two 8-bit threshold voltage data (VTH0 and VTH1) to a comparator to compare the data stored at the ADC register. The value of VTH0 and VTH1 depends on different conversion ratios (for the SCC mode) or charge and discharge voltage levels (for the CBB mode).

For SCC mode, both VTH0 and VTH1 are compared with ADC_DATA1 (the voltage level at the output of the HCBB). In this case VTH0 is used as a lower threshold V_{Aref} and VTH1 is used as a higher threshold V_{Bref} (these two thresholds are used to regulate the output range of the HCBB working in SCC mode, see Figure 15, Section 3.2.2, Chapter 3). For CBB mode, VTH0 is for the required charging voltage level and it is compared with ADC_DATA0 (the voltage level at the input of the HCBB). VTH1 is for the required discharging voltage level and it is compared with ADC_DATA1 (the voltage at the output of HCBB).

Two 3-bit compared results (Comp0 and Comp1) will be sent to both SCC and CBB FSM units as conditions. To start power delivery, one FSM will be enabled by the HCBB mode selector. And the other FSM is kept at idle state. And the selector will control a multiplexer to choose the 8-bit output data (SEL_C0 and SEL_C1) from the enabled FSM.

- **HCBB Control Code Block**

The output data passing through the multiplexer will be used in HCBB control code block to look up 34-bit HCBB_CODE for 34 switches inside the HCBB. The HCBB_CODE will be sent to the HCBB PDU through two output banks of the FPGA development kit (see Appendix A, Figure 81).

7.5 Testing and Verification

Figure 67 and Figure 68 shows the HCBB hardware verification system. It is also used as a variable power supply in our VLSI chip testing systems. On the PCB, nine electronic switch chips MAX4678 are used. For ADCs, two 8-bit 2 MHz AD7822BNZ chips are used. For FPGA, Vertex 5 xc5vlx110t is employed. Double layer ceramic capacitors of two values (2.2 uF and 4.7 uF) are used in the HCBB. The power supply is set at 1.1 V. A 0.5 K Ω resistor is placed between the power supply and the input of HCBB to limit the input current. The main purpose of this experimental set-up is to 1) provide fully controllable and variable VDD for our asynchronous chip testing system and 2) to verify the HCBB concept before laying out an on-chip version. More photos regarding the hardware verification system is shown in Appendix A, Figure 82, Figure 83 and Figure 84.

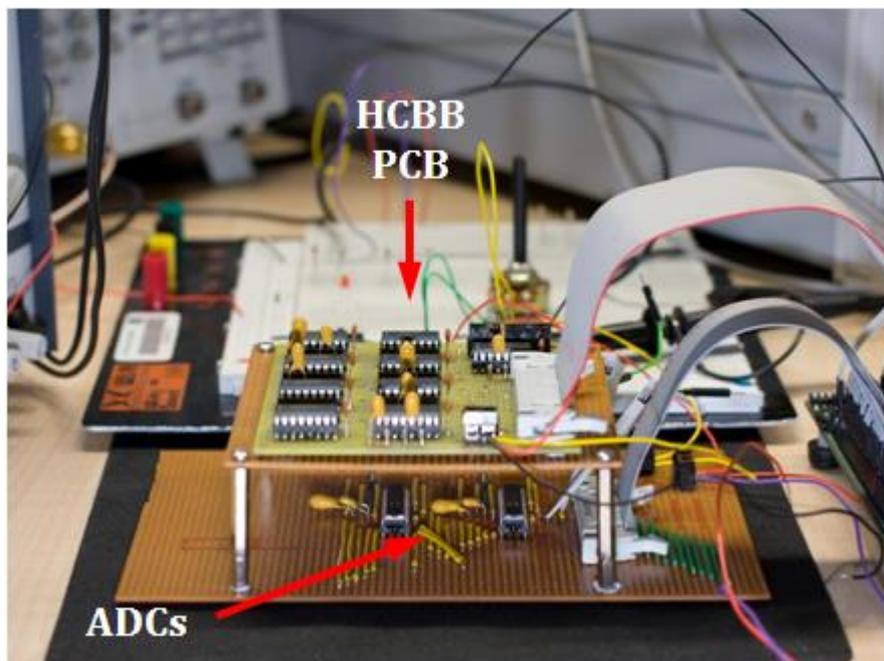


Figure 67. Hardware verification by PCB and FPGA (A).

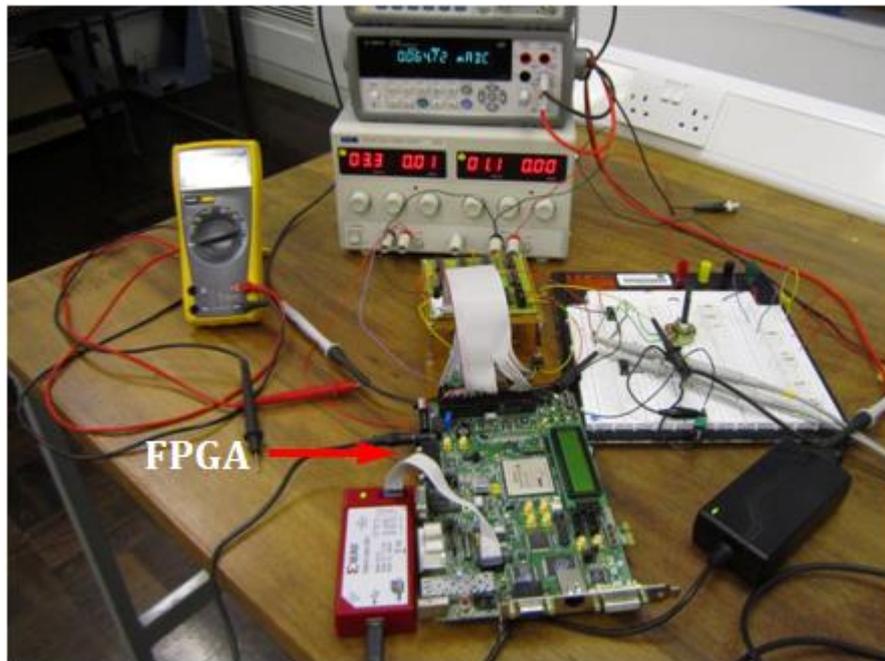


Figure 68. Hardware verification by PCB and FPGA (B).

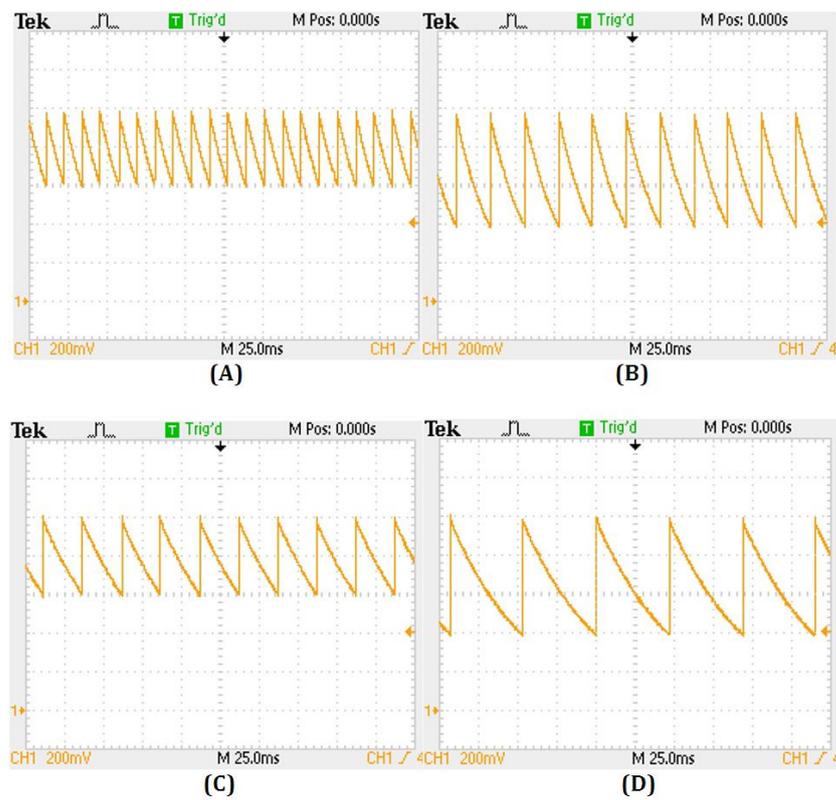


Figure 69. Voltage waveforms at output of HCBB working in CBB mode.

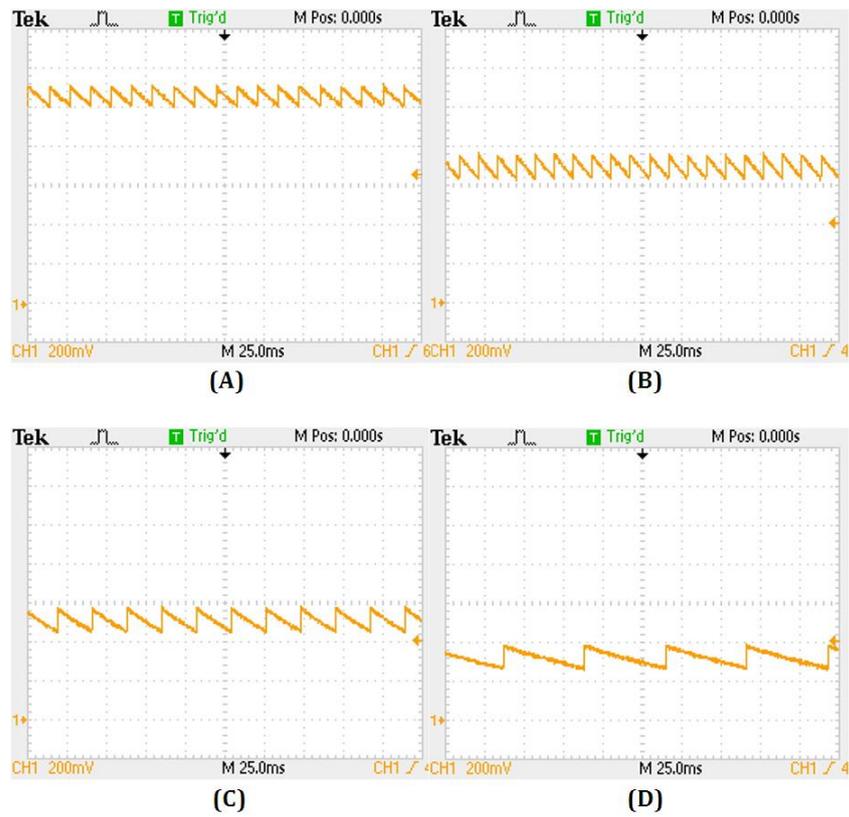


Figure 70. Voltage waveforms at output of HCBB working in SCC mode.

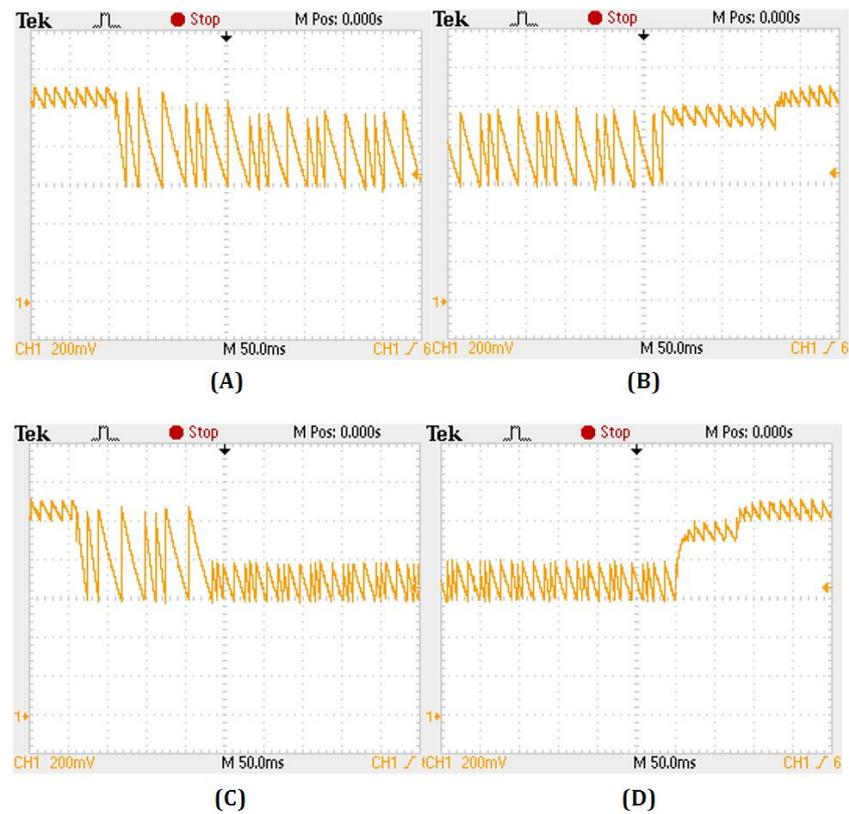


Figure 71. Mode switching between SCC and CBB modes.

For verifying HCBB functions, an RC load with fixed values (R: 10 K Ω , C: 0.1 μ F) is used. **Figure 69** shows HCBB working in CBB mode. In (A) and (B), capacitors with smaller value (2.2 μ F) are used to deliver power to the load. In (C) and (D), capacitors with bigger value (4.7 μ F) are used. Two discharge ranges are performed, 1-0.6 V for (A) and (C), 1-0.4 V for (B) and (D).

Figure 70 presents HCBB working in SCC mode with different step-down conversion ratios, (A) for 1.05 V (1/1), (B) for 0.7 V (2/3), (C) for 0.52 V (1/2) and (D) for 0.33 V (1/3). Since the load working under high VDD draws more energy than working under low VDD, HCBB performs more switching to maintain high voltage level shown in (A) and it needs less switching to keep low voltage level shown in (D). The voltage ripple range regulated by HCBB in SCC mode is less than 100 mV.

Figure 71 shows the voltage waveforms of HCBB output when mode switching is performed between SCC and CBB modes. For CBB mode, all capacitors are used for power delivery. The mode switching is performed from SCC mode (1.05 V (1/1)) to CBB mode (1-0.6 V) shown in (A) and to (0.8-0.6 V) shown in (C). Working in SCC mode to generate 1.05 V, each capacitor has accumulated enough energy to support the output in high voltage level. When it is switched to CBB mode, the redundant energy has to be discharged until the voltage level at each capacitor meet the requirement of the CBB mode. The mode switching is performed from CBB mode (1-0.6 V) to SCC mode (1.05 V (1/1)) in (B) and from (0.8-0.6 V) to SCC mode (1.05V (1/1)) in (D). When switching to the SCC mode, HCBB needs to spend a short period to accumulate enough energy to raise the output voltage level to meet the requirement of the SCC mode.

The energy delivery efficiency of HCBB is investigated and shown in **Figure 72**. This compares the energy delivered to load with the energy drawn from source per switching (for SCC mode) or per charging and discharging (for CBB mode). An RC load with fixed capacitance 0.1 μ F and variable resistance 1 to 10 K Ω is used. For the SCC mode shown in (A), when the load is heavy (small resistance), the conversion ratios used to deliver power at high voltage level did not work as not enough energy gets into HCBB. For CBB mode, the mode with higher average voltage output did not work when the load is heavy due to the charging speed

being slower than discharging speed. By using bigger capacitors, higher energy delivery efficiency can be achieved compared to using smaller capacitors in the discharging range 1-0.7 V in (B) and 1-0.4 V in (C). In (D), using small capacitors has higher efficiency than large ones in the discharging range 0.7-0.4 V when load is not heavy. Such characterizations may help the development of an optimal task and power scheduling method for an HCBB system.

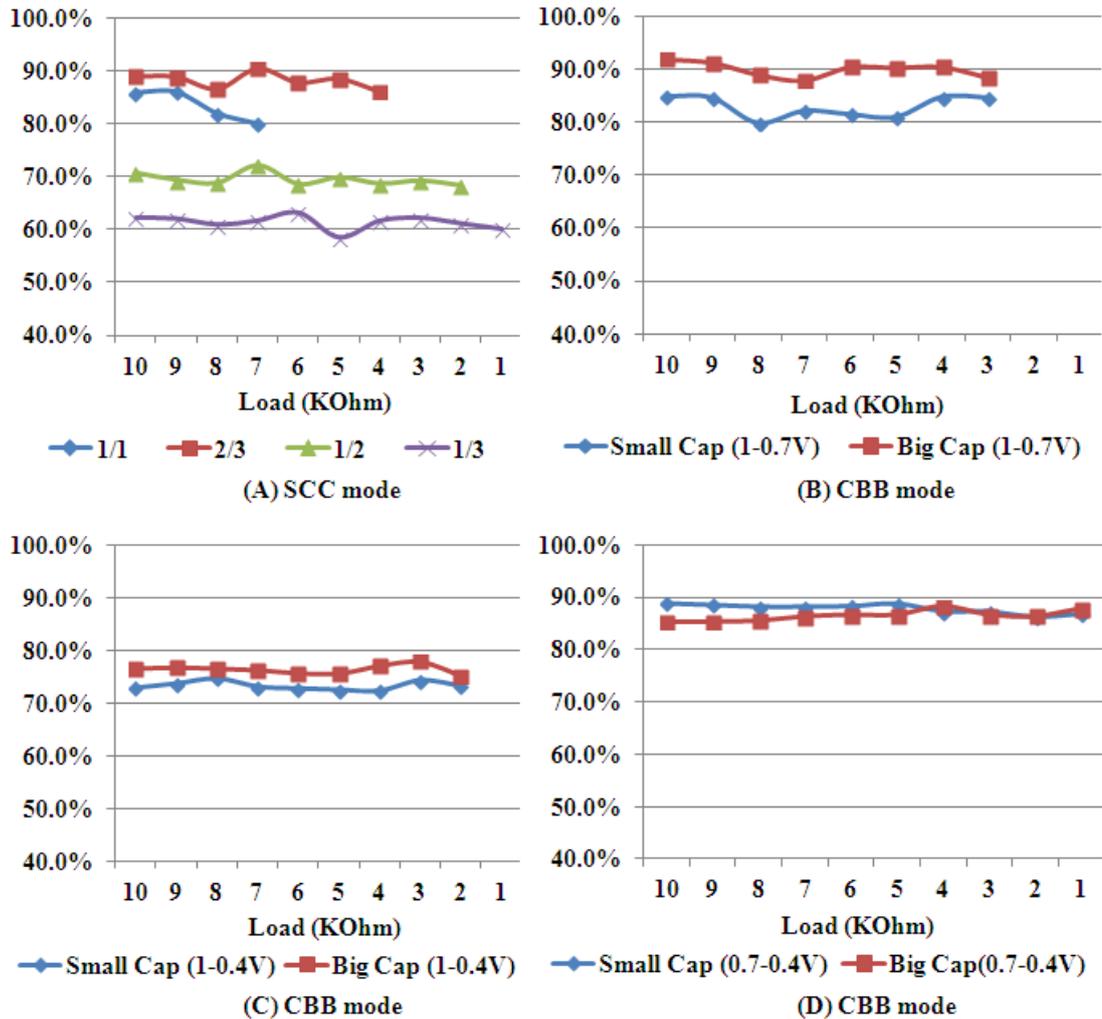


Figure 72. Energy delivery efficiency of HCBB with RC load.

In addition, the HCBB was used in a real asynchronous circuit testing system which investigates the behaviour of such loads under variable VDD, shown in Figure 73. The HCBB PCB working in SCC mode and CBB mode is controlled by FPGA (A). The regulated output power is delivered to a UMC 90nm CMOS technology based self-timed SRAM chip [35] by using a power supply cable connecting the HCBB and the testing chip. The testing chip is controlled by FPGA (B). Figure 74 shows the waveforms of HCBB powering the testing chip including

the HCBB output waveform and the tested SRAM writing acknowledgement signal transition waveform. For CBB mode shown in (A), the signal waveform of the asynchronous memory is modulated by the VDD provided by the HCBB. For SCC mode shown in (B), a stable power supply (1 V) is provided by HCBB to the chip.

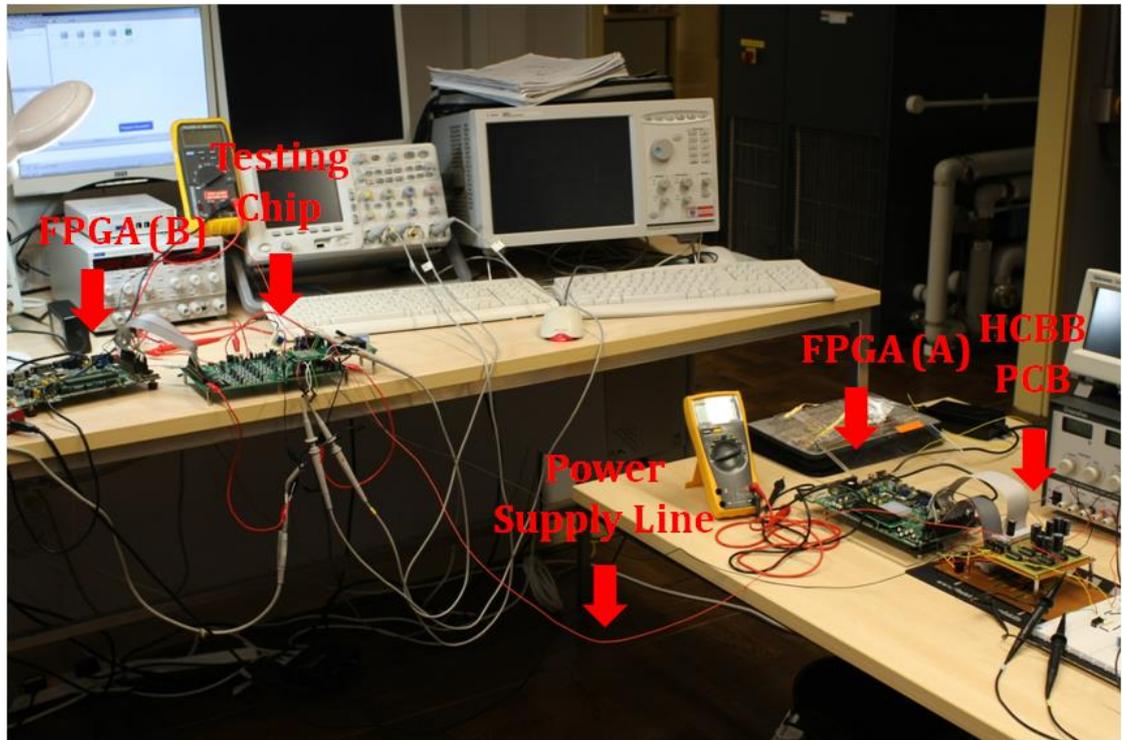


Figure 73. HCBB powering a testing chip: asynchronous self-timed SRAM.

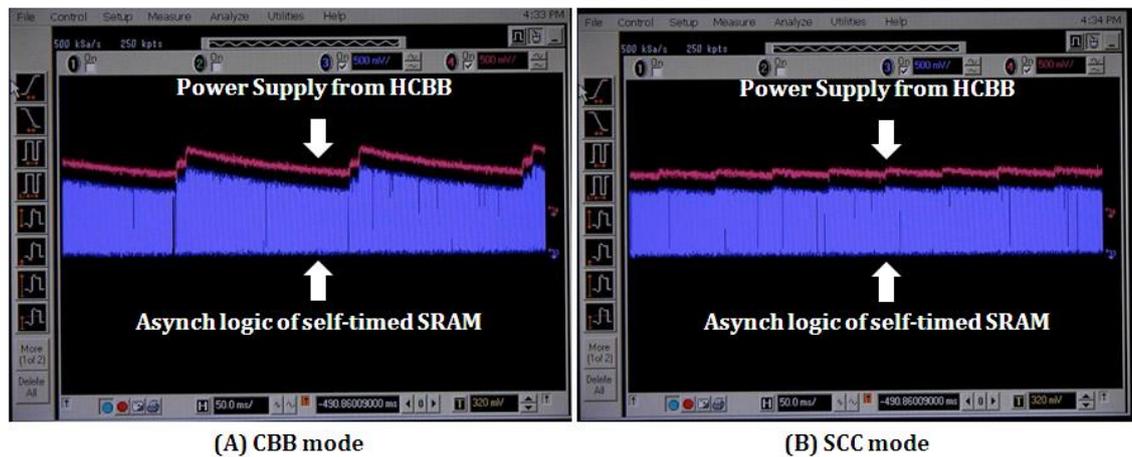


Figure 74. Waveforms of HCBB powering an asynchronous self-timed SRAM chip in CBB mode (A) and in SCC mode (B).

7.6 Summary and Conclusions

This chapter describes a hybrid power delivery method, HCBB, which can work in

SCC or CBB modes. This hybrid structure is developed for EH systems to solve task and power scheduling problems, in which asynchronous loads may call CBB mode or SCC mode from time to time according to harvested energy and tasks. However on-chip capacitive element fabrication is expensive and costs large area compared with logic elements. Since the hybrid structure has the advantage in sharing switches and capacitors for implementing either SCC or CBB mode, the design effectively keep the chip size and fabrication expense as small as possible for the system requiring high flexibility in power delivery, low fabrication costs, and low chip area penalty.

The HCBB structure and working principles are presented in the chapter. Additionally, before fabricating the HCBB on chip, hardware verification is implemented by using PCB and FPGA. Valuable reference data are obtained from the verification. The corresponding control method is developed and implemented on the FPGA. In the hardware verification, the power delivery behaviours of the HCBB are presented in terms of CBB mode, SCC mode, and switching between CBB and SCC mode during the power delivery process.

Besides, the HCBB method is characterized. The energy delivery efficiency is investigated by using SCC and CBB modes to power RC loads with different weight. The HCBB has also been used as a much needed variable power supply in our asynchronous circuit testing system and contributed to the successful testing of our asynchronous SRAM. The asynchronous chip testing system and tested chip signal transition behaviours are presented by using CBB and SCC mode. Through the testing, the asynchronous chip shows a good compatibility in working with the HCBB hardware. This enhances confidence and knowledge of not only HCBB but also pure CBB which previously was only demonstrated through simulations.

Chapter 8

Conclusion and Future Work

For systems depending on EH methods, a fundamental contradiction in the power delivery chain has existed between conventional synchronous loads requiring a relatively stable Vdd and energy transducers unable to supply it. DC/DC conversion has therefore been an integral part of such systems to resolve this contradiction. However, instability of the harvested power may still be passed to computational loads by the DC/DC conversion. On the other hand, asynchronous loads, in addition to their potential power-saving capabilities, can be made tolerant to a much wider range of Vdd variance. This may open up opportunities for much more energy efficient methods of power delivery.

Therefore, this research concentrates on power delivery mechanisms which deliver power directly from EH transducers via on-chip PDUs, bypassing energy storage devices, to asynchronous computational loads to meet the trend of micro-scale EH systems and implement task and power scheduling according to the energy modulated computing method.

8.1 Conclusion

This research firstly presents an investigation on the behaviour and performance of a favourite on-chip DC/DC conversion unit – SCC that targets at delivering a stable power from a relatively stable power source (*introduced in Chapter 4*). In the investigation, the SCC is implemented by hardware and applied to power an asynchronous chip. Ability of regulating various voltage levels using the SCC hardware is verified. At the meantime, the asynchronous circuit shows a satisfactory robustness against radically variable Vdd produced by the SCC through continuously and sequentially changing voltage conversion ratios during the power delivery process.

However, EH systems tend to have highly time-variable power supply. When bypassing off-chip bulky energy storage devices for extremely EH system minimization, normal DC/DC conversion units may be unable to maintain high conversion efficiency under such radically variable power sources. This is confirmed by in-depth investigations on different power delivery mechanisms driving both asynchronous and synchronous loads directly from a harvester source bypassing bulky energy storage devices (*presented in Chapter 5*). Therefore, to step over this problem, a novel power delivery method, which employs a CBB for adaptively storing the energy from the harvesting circuit depending on load and source conditions, is developed. Its advantages, especially when driving asynchronous loads, are demonstrated through comprehensive comparative analysis.

Additionally, the CBB structure is not developed for working with stable power inputs, but its aperiodic and amplitude-flexible approach makes it better suited for temporally storing the energy from an unpredictable power source for use by an asynchronous load. On the other hand, the CBB method represents the first attempt at developing appropriate power and energy delivery units suitable for loads which can tolerate and work well under highly variable Vdds and energy sources which cannot maintain constant outputs. The CBB also provides enough flexibility for intelligent control aimed at maximizing performance, energy efficiency and other quantifiable goals.

Based on the CBB concept, an asynchronous controller is developed for a modified CBB incorporating low-power threshold voltage sensing techniques and variable-Vdd-robustness asynchronous loads to work with tasks (*reported in Chapter 6*). By applying the asynchronous method to the controller design, the whole system is able to get rid of global clocks that have lots of disadvantages. Additionally, the successful asynchronous control design drives a case study that is performed to explore relations between power path and task path. Then a fundamental task and power scheduling method is developed based on the investigated data. Based on the method, the system is able to implement optimizations in harvested energy use or operational life of the CBB PDU powered by a long-life miniature battery.

Based on the power delivery mechanism investigations in the research, CBB and SCC both have their advantages and disadvantages and are therefore suitable for working under different system operating conditions. To deal with different tasks with variable harvested power, the EH system may have a range of operation conditions and thus call for both CBB and SCC type power delivery. Therefore, a hybrid structure HCBB using the same set of capacitors to form both CBB and SCC configurations which can be reconfigured at run time is developed (***shown in Chapter 7***). The HCBB enable the EH system effectively realize a kind of dynamic reconfiguration of power delivery. Additionally, the system size can be saved, as size overheads are especially important as on-chip capacitors for energy storage tending to be huge compared to logic. The HCBB structure is also implemented by hardware and the method of dynamically reconfiguring power delivery is verified.

In this research, the power delivery mechanisms (SCC, CBB, and HCBB) are not only investigated and verified by simulations, but also by hardware implementations which are currently employed for the purpose of chip testing & verification, and micro-scale EH system demonstrations.

8.2 Future work

- **Micro-scale EH System Integration**

Since the CBB concept can be believed as a kind of generalization of SCC and the HCBB method can be considered as an extension of the CBB, the CBB PDU thereby can be implemented in hundreds and thousands ways according to practical applications.

The CBB concept provides a large flexibility for on-chip power delivery in EH systems where energy storage devices are bypassed. Due to the significant progress in micro-scale EH transducer researches, lots of different EH transducers can be integrated on chip (such as vibration, RF and thermal EH transducers). In this case, incorporating such micro-scale EH transducers, CBB units, and asynchronous computational loads (such as asynchronous microprocessors), a fully integrated micro-scale EH system may be achieved on a single chip, gaining smaller system size, higher energy efficiency, more satisfactory voltage variation robustness compared with traditional EH systems. The research of the micro-scale

EH system integration may create huge potentials in practical applications. The real beauties of the integration concept still need to be investigated and methods to implement such integration need to be studied.

- **Task and Power Scheduling**

In the research, a preliminary asynchronous controller is developed for the CBB concept. The charging and discharging processes are according to the first fully charged first discharging rule. Although it has a degree of ability working with tasks, the asynchronous controller still needs incorporating with a task and power scheduler. Unfortunately, they are implemented separately in the research and the scheduler is only implemented in high level without circuit implementations. However, for practical applications, the asynchronous controller and the task and power scheduler should be integrated together on the same circuit level.

Additionally, the task and power scheduling method in the research is fundamental. Only the optimization in harvested energy use and CBB PDU operational life are considered. However, in real systems, there are lots of factors may be considered and optimized such as energy delivery efficiency or even the combination of several factors. Therefore, more sophisticated task and scheduling methods are waiting to be developed to replace this fundamental method. Therefore, lots of load computation and power performance modelling and analyzing work based on the CBB concept is required in order to develop more advanced task and power scheduling methods for the micro-scale EH systems

- **Energy Harvesting Prediction**

EH prediction is also very important and it has not been investigated in this research unfortunately. The input power prediction is helpful to estimate each capacitor charge time. Therefore, it is also helpful to develop more advanced task and power scheduling methods. On the other hand, since the micro-scale EH system in this research bypasses energy storage devices, the ability of energy buffering is not as good as that of traditional EH systems (employing off-chip bulky energy storage devices). Thus, EH prediction may enable the system to implement processing heavy task when harvested energy is abundant and letting loads (or whole system) to go to sleep mode when the harvested energy is very limited. This

effectively help the micro-scale EH system to survive in harsh and radically variable environments and work more efficiently.

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Appendix A: Photos & Pictures

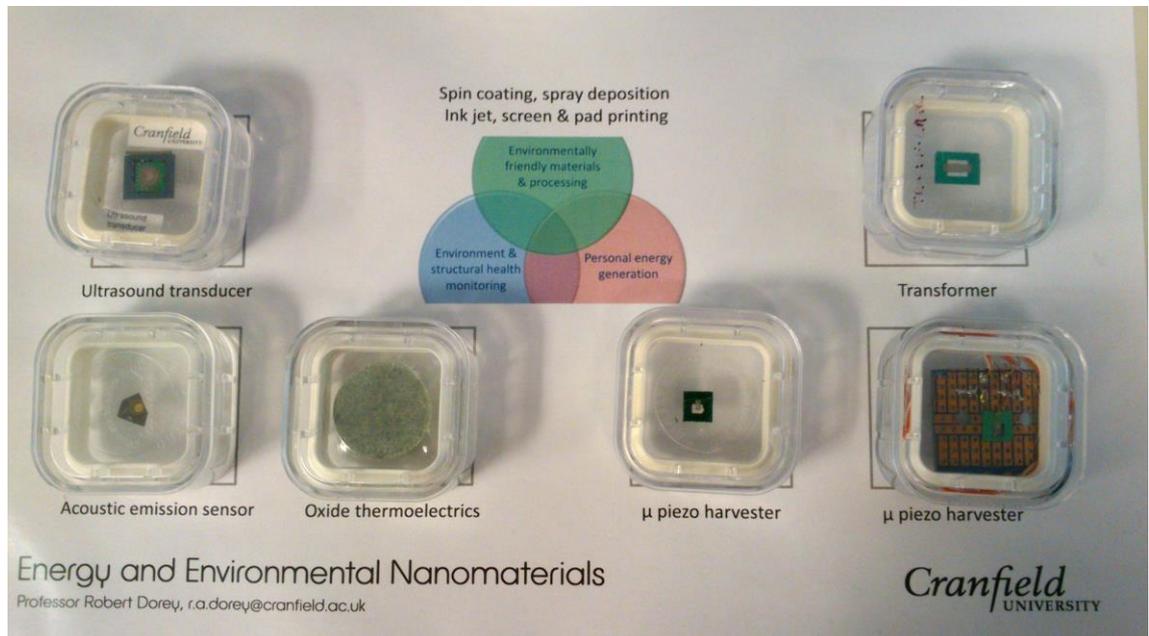
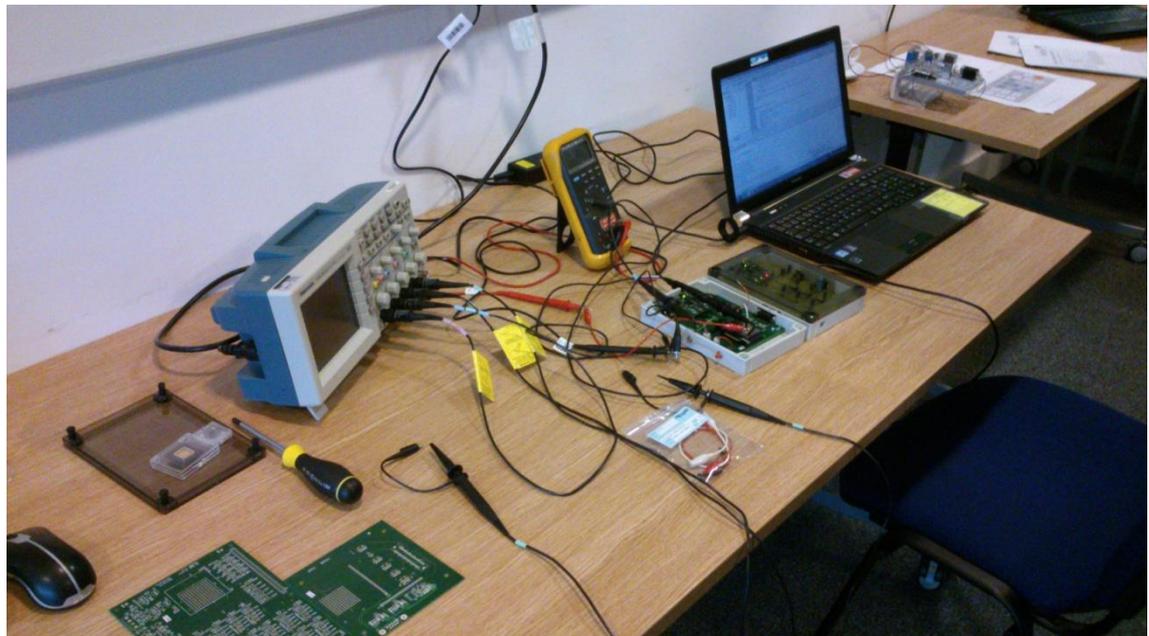


Figure 75. Energy and environmental nano-material demonstration of Cranfield University in Energy Harvesting 2013, London.



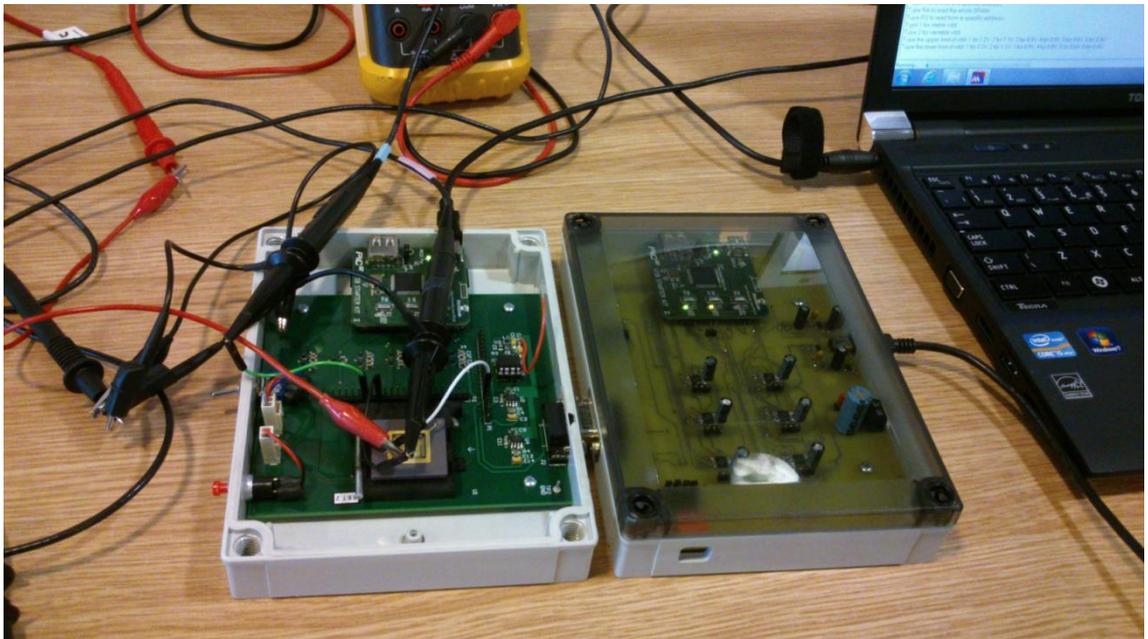


Figure 77. Switched capacitor based variable V_{dd} powered asynchronous self-timed SRAM demonstrators presented in Holistic Energy Harvesting project acceptance meeting at Southampton University, 2nd of July, 2012.

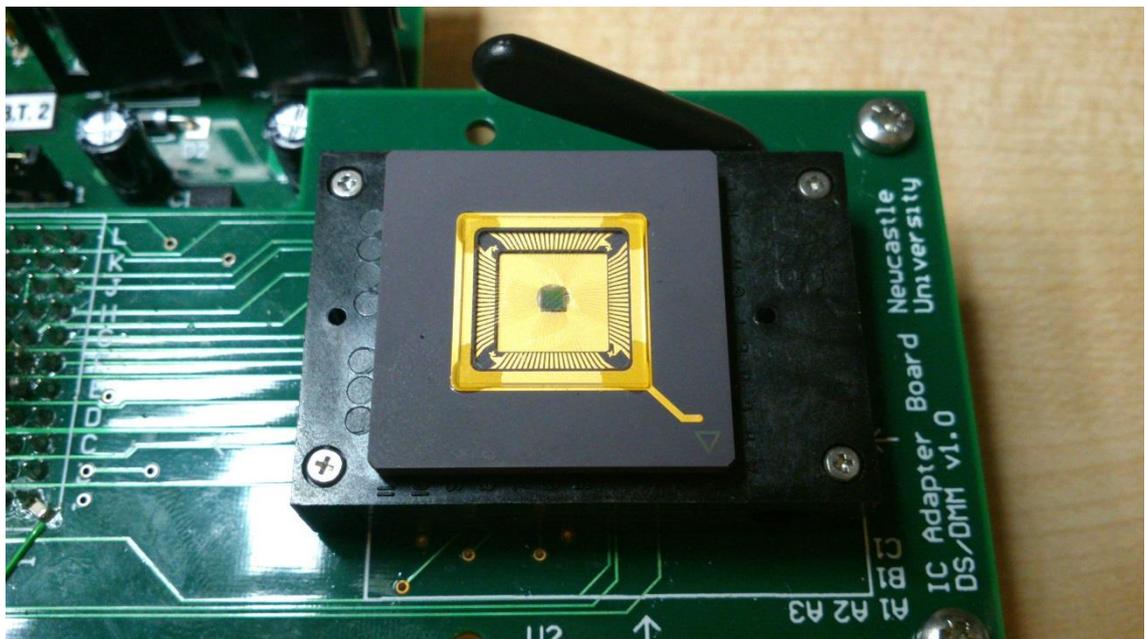


Figure 78. Asynchronous Self-timed SRAM chip [35].

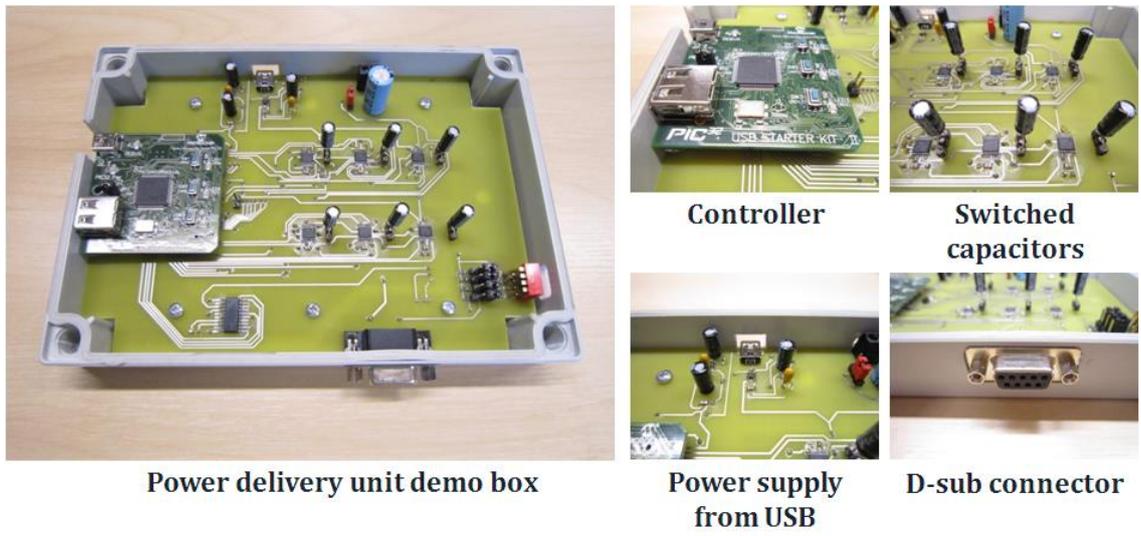


Figure 79. Switched capacitor based power delivery unit demo box hardware implementation.

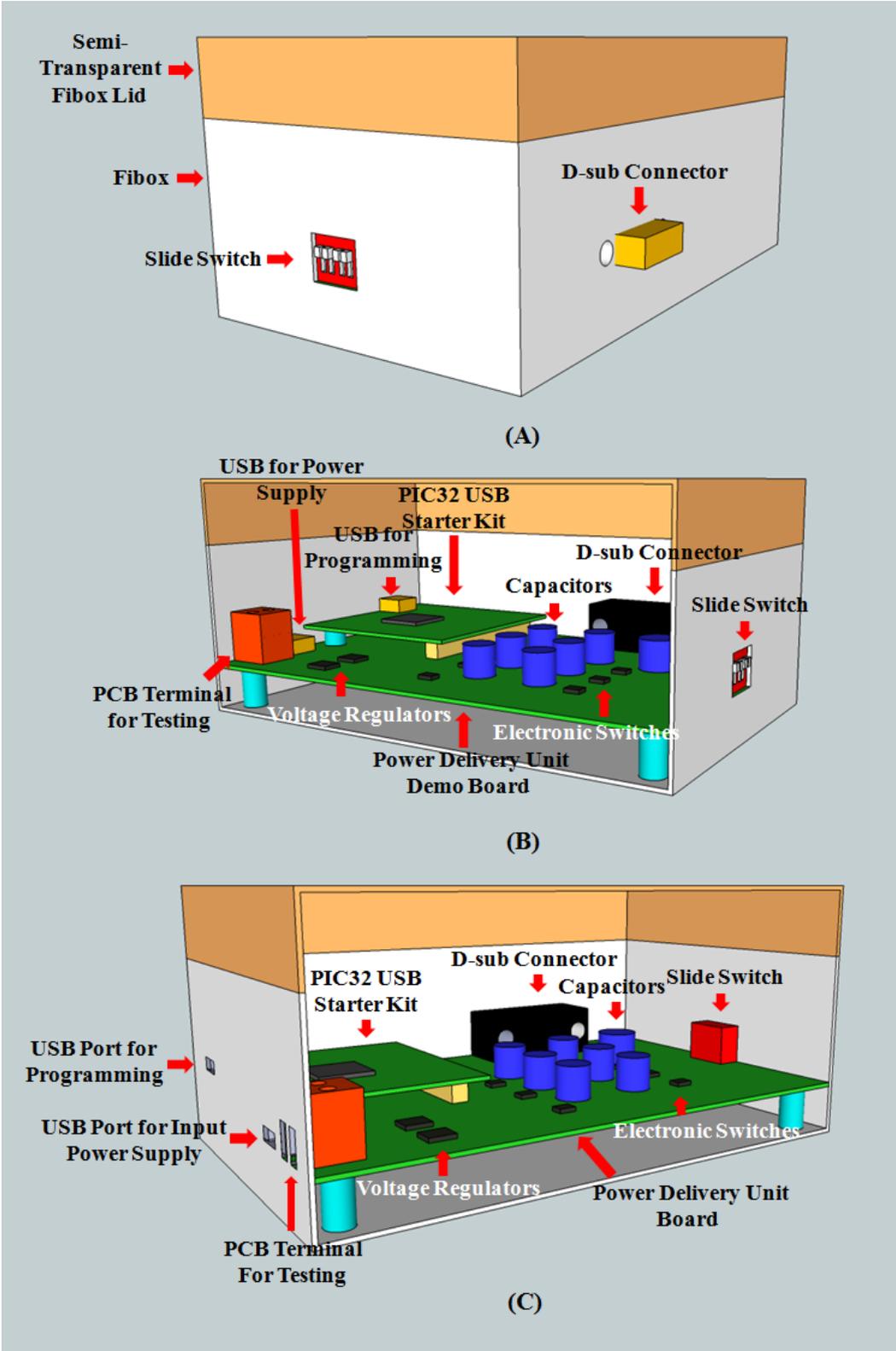


Figure 80. 3D graphs of power a delivery unit demo box.

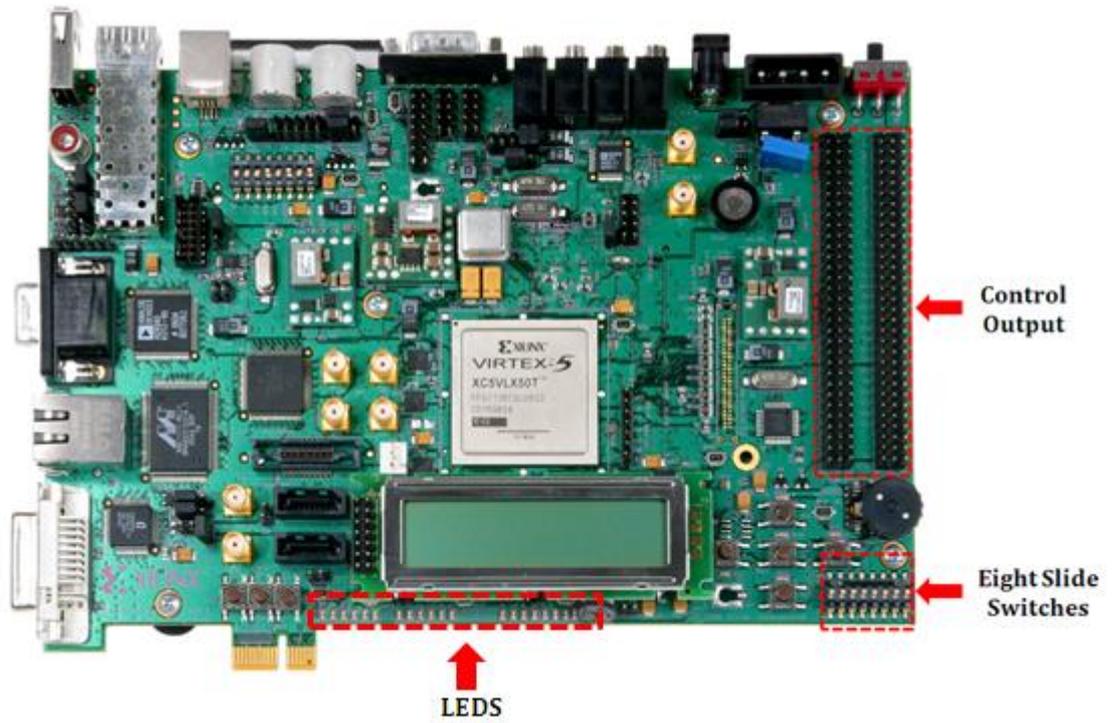


Figure 81. FPGA development kit board Vertex 5 xc5vlx110t.

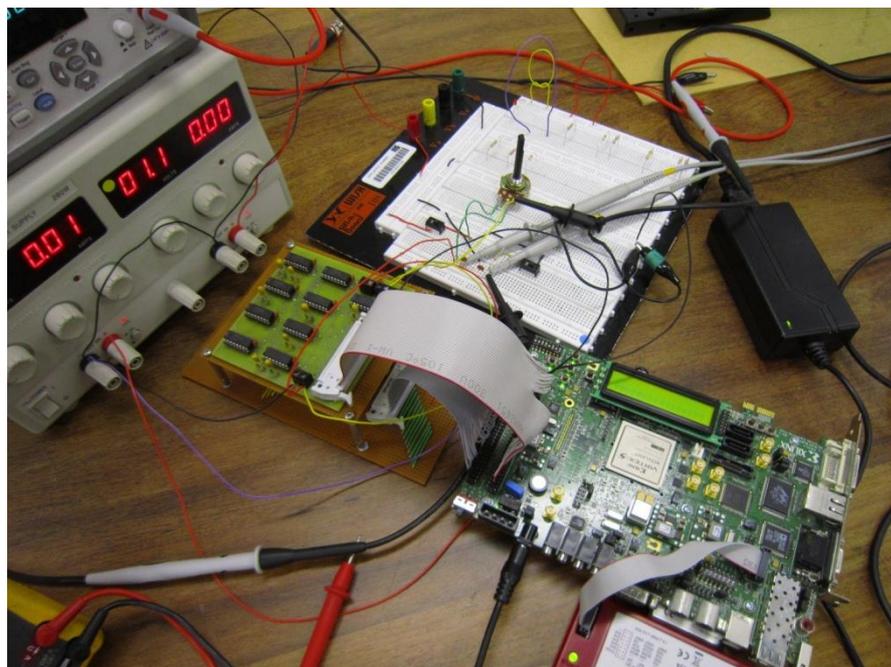


Figure 82. HCBB hardware implementation using HCBB PCB and FPGA.

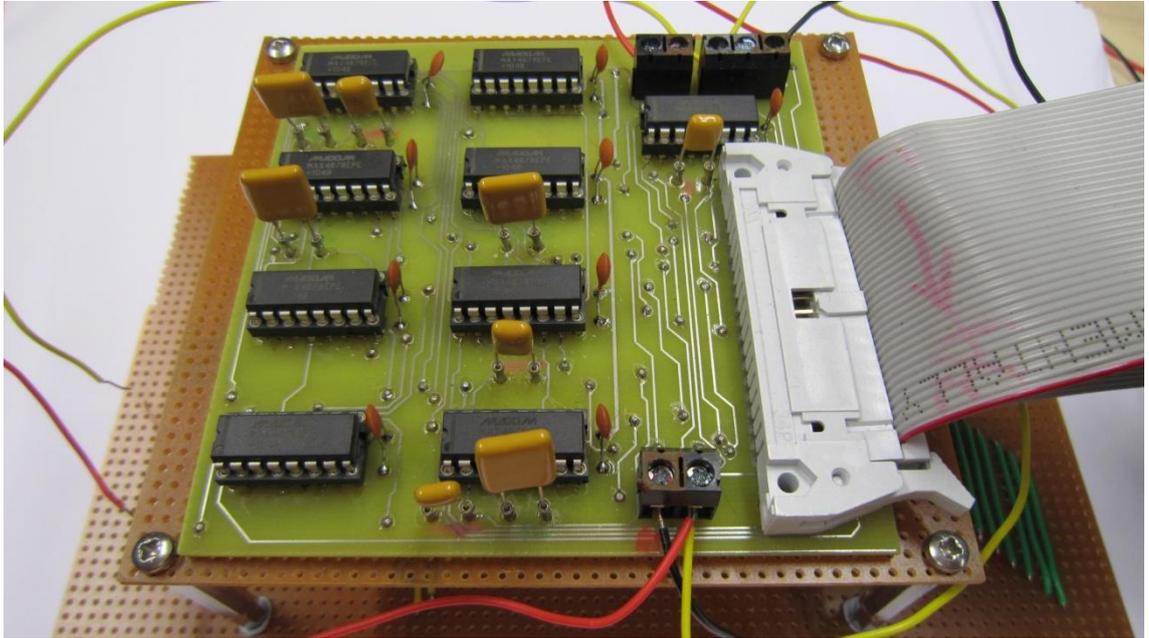


Figure 83. HCBB circuit implemented on PCB.

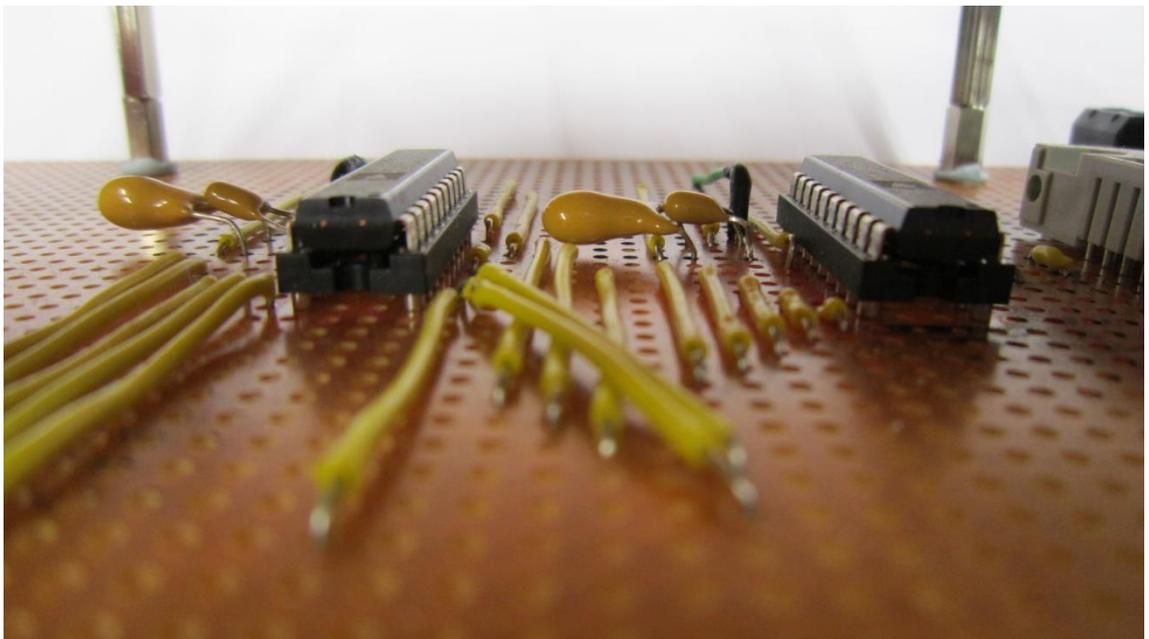


Figure 84. Two ADCs used by HCBB.

Appendix B: Program Flowcharts

- Polling Mode for Both Command and ADC Sensing

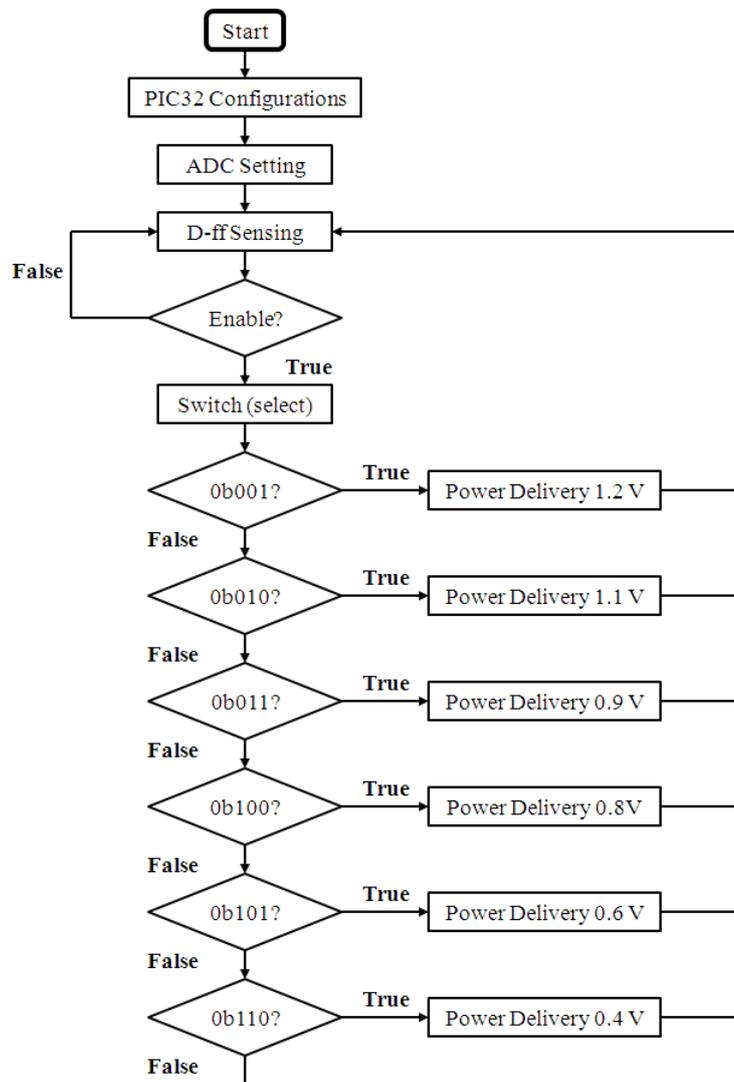


Figure 85. Main program flowchart for SCC control (polling mode for both command and ADC sensing).

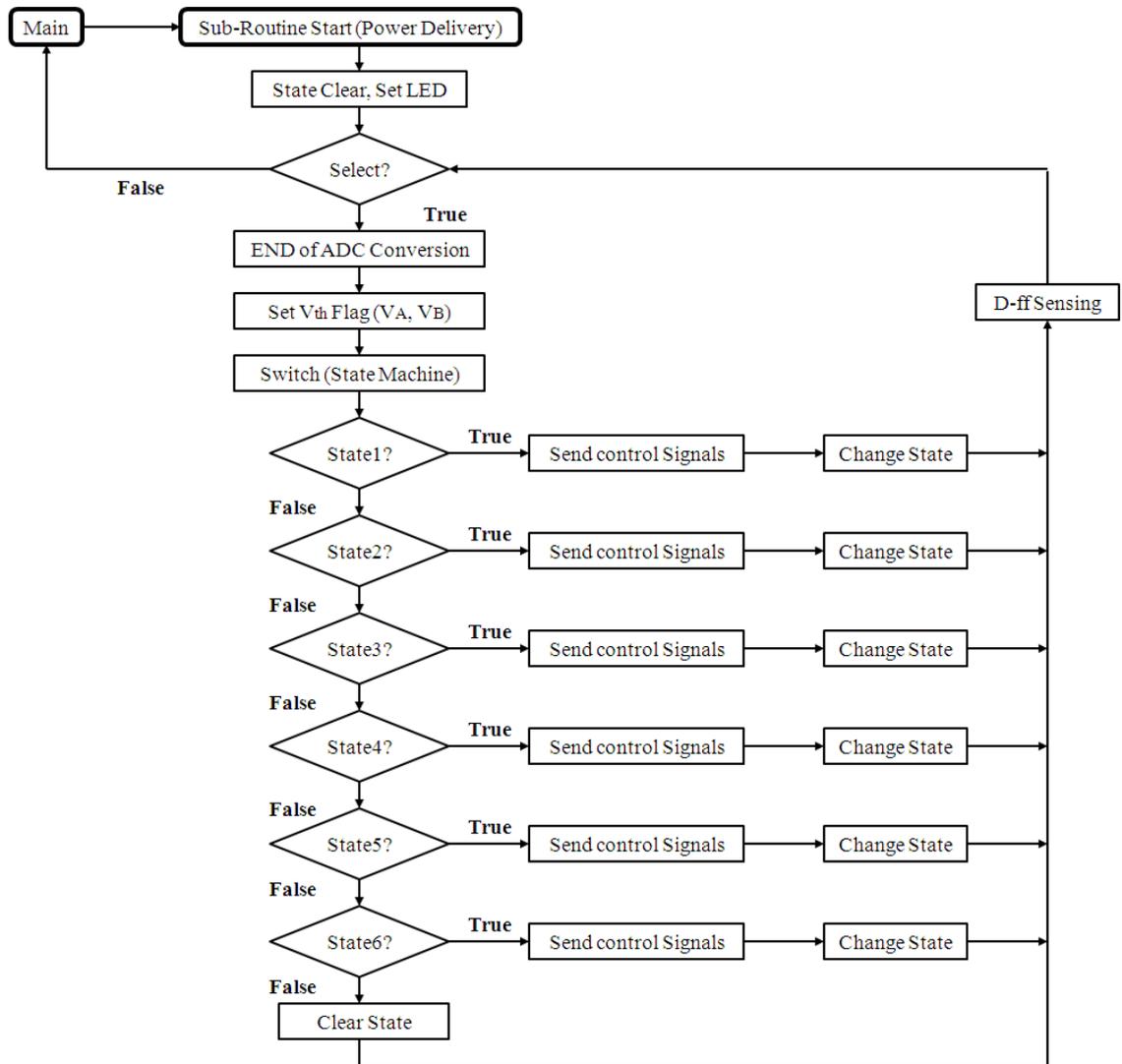


Figure 86. Sub-routine program (Power Delivery) flowchart for SCC control (polling mode for both command and ADC sensing).

- **Interrupt Mode for Both Command and ADC Sensing**

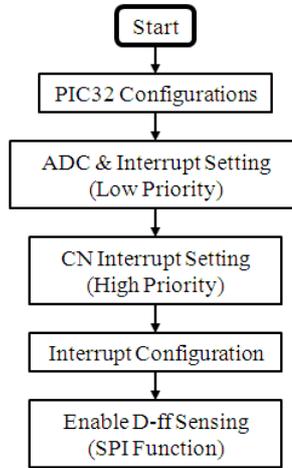


Figure 87. Main program flowchart for SCC control (interrupt mode for both command and ADC sensing).

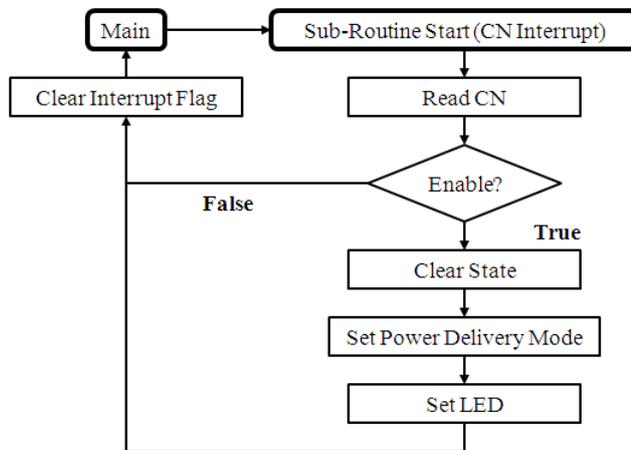


Figure 88. Sub-routine program (CN Interrupt) flowchart for SCC control (interrupt mode for both command and ADC sensing).

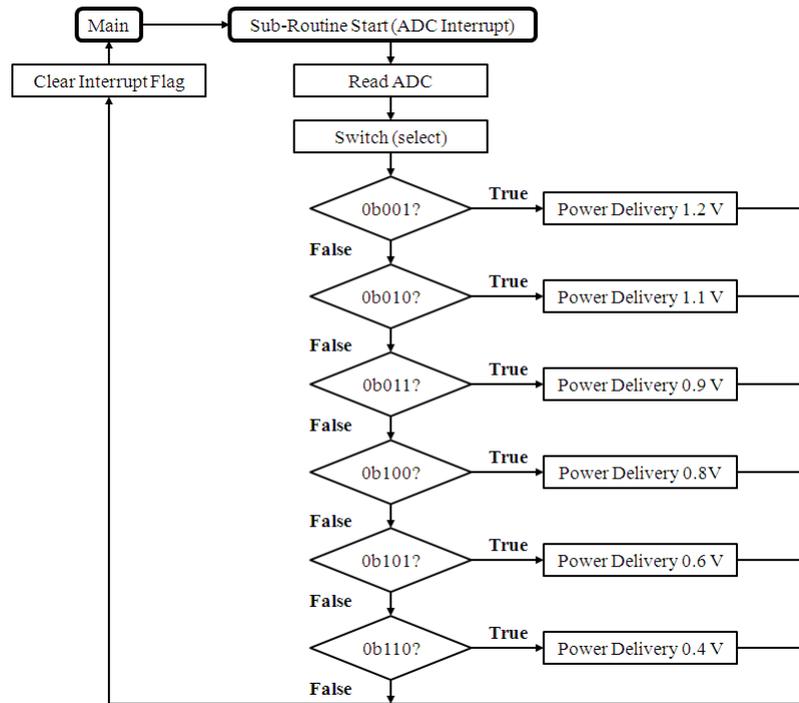


Figure 89. Sub-routine program (ADC Interrupt) flowchart for SCC control (interrupt mode for both command and ADC sensing).

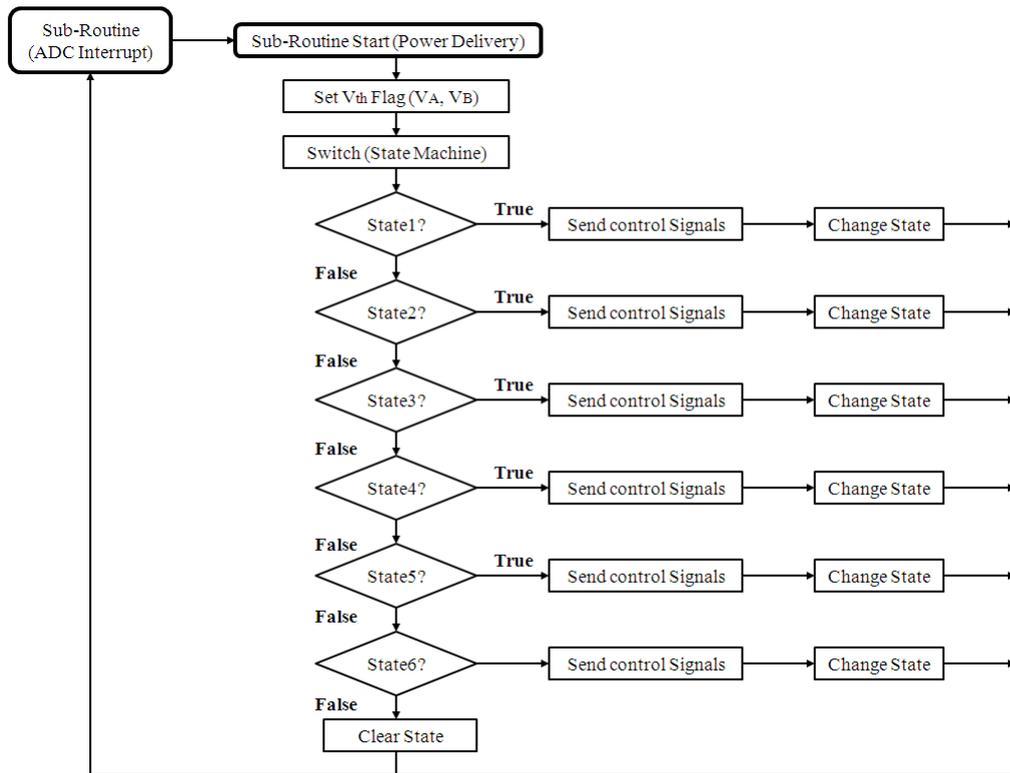


Figure 90. Sub-routine program (Power Delivery) flowchart for SCC control (interrupt mode for both command and ADC sensing).

- **Interrupt Mode for Command Sensing and Polling Mode for ADC Sensing**

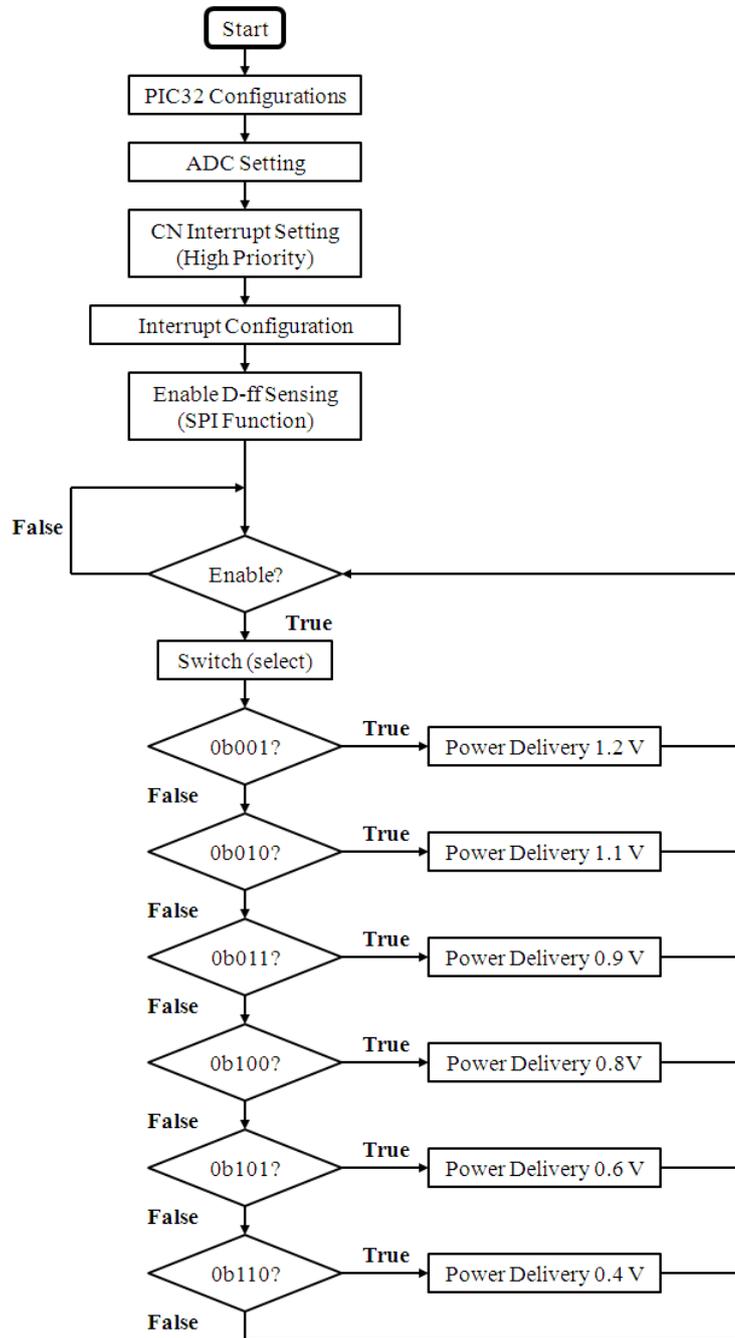


Figure 91. Main program flowchart for SCC control (interrupt mode for command sensing and polling mode for ADC sensing).

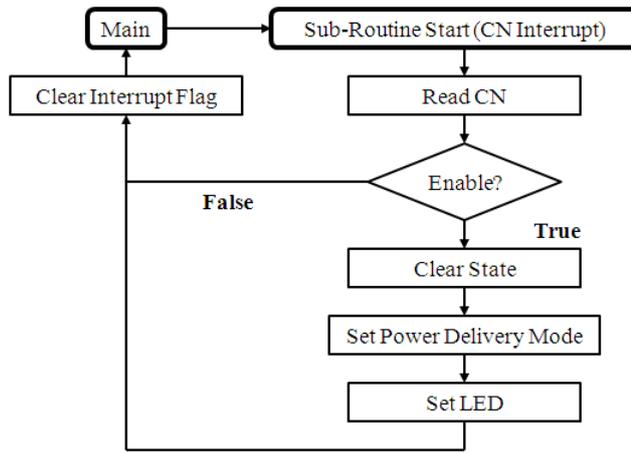


Figure 92. Sub-routine program (CN Interrupt) flowchart for SCC control (interrupt mode for command sensing and polling mode for ADC sensing).

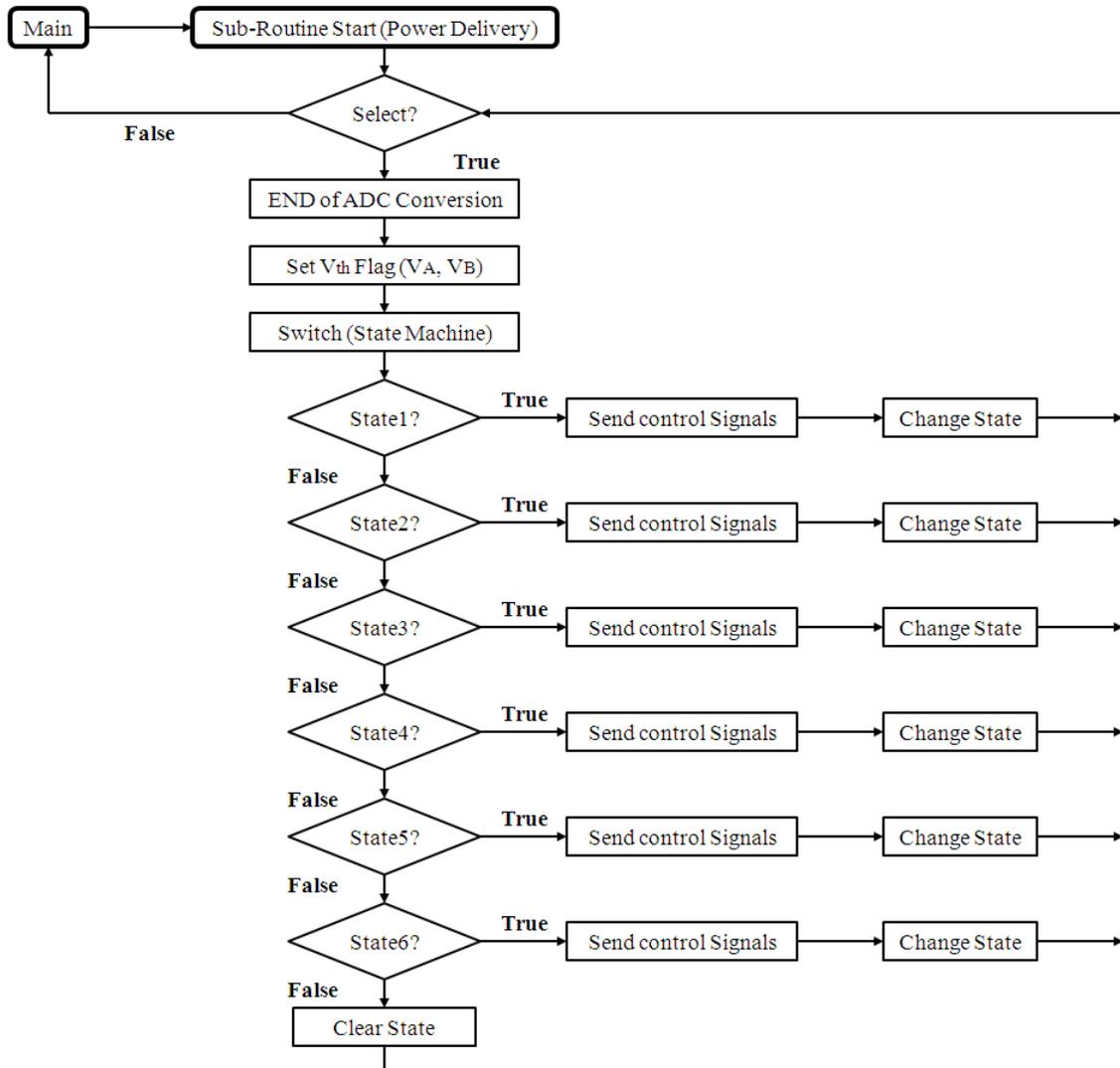


Figure 93. Sub-routine program flowchart (Power Delivery) for SCC control (interrupt mode for command sensing and polling mode for ADC sensing).

Appendix C: EQN Files for CBB

Asynchronous Controller Models

- **CB Ch/DsCh Control Model**

EQN file for model capfsm12

Generated by petrify 4.2 (compiled <unknown compile date>)

Outputs between brackets "[out]" indicate a feedback to input "out"

Estimated area = 37.00

INORDER = ChSense CmpAAv CmpBAv DsChSense StaChPro StaDsChPro
TaskComp ChSwOn CmpARes CmpBRes CmpBSet DsChComp DsChSwOn NextPro
NextTask SetChAv SetDsChAv csc0;

OUTORDER = [ChSwOn] [CmpARes] [CmpBRes] [CmpBSet] [DsChComp]
[DsChSwOn] [NextPro] [NextTask] [SetChAv] [SetDsChAv] [csc0];

[ChSwOn] = CmpAAv CmpARes';

[CmpARes] = StaChPro SetDsChAv' csc0;

[CmpBRes] = CmpBAv DsChSense' DsChComp;

[CmpBSet] = StaDsChPro csc0';

[DsChComp] = CmpBAv' SetDsChAv csc0 + TaskComp;

[DsChSwOn] = StaDsChPro CmpBSet' csc0;

[NextPro] = NextTask' TaskComp' DsChSense' DsChComp;

[NextTask] = CmpBRes' TaskComp CmpBAv';

[SetChAv] = SetDsChAv' + StaChPro;

[SetDsChAv] = ChSense' CmpAAv' NextPro' csc0' + SetDsChAv (SetChAv +
DsChComp') + DsChSwOn;

[csc0] = CmpAAv' csc0 + CmpBAv;

The initial state is unstable. No reset information generated.

Signal SetChAv enabled in the initial state.

- **Charge Sequence Control Model**

```
# EQN file for model chargefsm18
# Generated by petrify 4.2 (compiled <unknown compile date>)
# Outputs between brackets "[out]" indicate a feedback to input "out"
# Estimated area = 31.00

INORDER = ChSwOn1 ChSwOn2 ChSwOn3 SetChAv1 SetChAv2 SetChAv3
SetDsChAv1 SetDsChAv2 SetDsChAv3 ChSense1 ChSense2 ChSense3 StaChPro1
StaChPro2 StaChPro3 csc0 csc1;

OUTORDER = [ChSense1] [ChSense2] [ChSense3] [StaChPro1] [StaChPro2]
[StaChPro3] [csc0] [csc1];

[ChSense1] = ChSwOn1 csc1';
[ChSense2] = ChSwOn2 csc0;
[ChSense3] = ChSwOn3 csc1;

[StaChPro1] = SetDsChAv1' SetChAv1 StaChPro3' csc1 + StaChPro1 csc0;
[StaChPro2] = SetDsChAv2' (StaChPro1' SetChAv2 csc0' + StaChPro2);
[StaChPro3] = SetDsChAv3' (StaChPro1' StaChPro2' SetChAv3 csc0 csc1' +
StaChPro3);

[csc0] = csc0 (StaChPro1' + SetDsChAv1') + ChSwOn2;
[csc1] = ChSwOn1' csc1 + ChSwOn3;

# Set/reset pins: reset(StaChPro1) reset(StaChPro2) reset(StaChPro3) set(csc0)
set(csc1)
```

- **Discharge Sequence Control Model**

```
# EQN file for model dischargefsm8
# Generated by petrify 4.2 (compiled <unknown compile date>)
# Outputs between brackets "[out]" indicate a feedback to input "out"
# Estimated area = 35.00

INORDER = DsChComp1 DsChComp2 DsChComp3 DsChSwOn1 DsChSwOn2 DsChSwOn3 NextPro1
NextPro2 NextPro3 SetDsChAv1 SetDsChAv2 SetDsChAv3 DsChSense1 DsChSense2 DsChSense3
StaDsChPro1 StaDsChPro2 StaDsChPro3 csc0 csc1;
OUTORDER = [DsChSense1] [DsChSense2] [DsChSense3] [StaDsChPro1] [StaDsChPro2]
[StaDsChPro3] [csc0] [csc1];
[DsChSense1] = DsChComp1' DsChSwOn1;
[DsChSense2] = DsChComp2' DsChSwOn2;
[DsChSense3] = NextPro3' DsChSwOn3 csc0';
[StaDsChPro1] = DsChComp2' csc0' DsChSense3' DsChSense2' + SetDsChAv1 csc0 csc1;
[StaDsChPro2] = DsChSense3' csc0';
[StaDsChPro3] = NextPro2 DsChComp3' csc0' SetDsChAv3 + StaDsChPro3 DsChComp1'
DsChSense1' csc0 + csc1' + DsChSense3;
[csc0] = csc0 (NextPro1' + SetDsChAv2' + DsChComp2) + csc1';
[csc1] = NextPro3 (csc1 + NextPro1') + DsChComp3';

# Set/reset pins: reset(StaDsChPro3) set(csc0)
```

Appendix D: Recently Published SCC Results

Comparison with recently published SCC results.

Design	[203]	[204]	[205]	[206]	[147]	[16]
Technology (μm)	0.35	0.35	0.35	0.18	0.13	0.045
Chip Area (mm^2)	7.8	N/A	2.6x2.6	1.6x1.6	1.5x1.5	N/A
Active Area (mm^2)	N/A	0.48	N/A	0.57	0.52	0.16
Total On-Chip Capacitance (nF)	6.72	N/A	1.2	2.4	0.35	1.234
Type of On-Chip Capacitor	3D On Chip Cap	N/A	N/A	MOS Cap	Dual MIM Cap	MOS Cap
Number of Conversion Ratio	1	3	1	5	3	5
Vout (V)	0.8 to 1.5	2	1	0.3 to 1.1	0.3 to 1.1	0.8 to 1
Vin (V)	2.5	15 to 5	5	1.2 & 1.8	1.2	1.8
Minimum Load Current (μA)	500	560	N/A	10	1	100
Load Power Range (mW)	0.4 to 7.5	>1	10	0.005 to 1	0.001 to 0.23	≤ 7.2
Efficiency Range (%)	50 to 66.7	28 to 42	62	50 to 80	30 to 80	≤ 69
Operating Frequency (MHz)	0.2 to 1	1	15	15/7.5/3.75	3.0/3.6/1.8*	30

* In this work, an asynchronous controller is used and the switching frequency is adaptive to load weight. Here the frequencies of three examples reported on the paper are shown.

Appendix E: Discharge Ranges of CBs with Different Capacitance Value

Discharge ranges of CBs with different capacitance value for discharging a same amount of energy to load (low end 0.4 V).

Capacitance (pF)		Discharging Range (V) (1)			Energy (pJ)
	20	1	to	0.4	8.4
1.5x	30	0.849	to	0.4	8.4
2x	40	0.762	to	0.4	8.4
2.5x	50	0.704	to	0.4	8.4
3x	60	0.663	to	0.4	8.4

Discharge ranges of CBs with different capacitance value for discharging a same amount of energy to load (low end 0.45 V).

Capacitance (pF)		Discharging Range (V) (2)			Energy (pJ)
	20	1	to	0.4	8.4
1.5x	30	0.873	to	0.45	8.4
2x	40	0.789	to	0.45	8.4
2.5x	50	0.734	to	0.45	8.4
3x	60	0.695	to	0.45	8.4

Discharge ranges of CBs with different capacitance value for discharging a same amount of energy to load (low end 0.5 V).

Capacitance (pF)		Discharging Range (V) (3)			Energy (pJ)
	20	1	to	0.4	8.4
1.5x	30	0.9	to	0.5	8.4
2x	40	0.819	to	0.5	8.4
2.5x	50	0.766	to	0.5	8.4
3x	60	0.728	to	0.5	8.4

APPENDIX E: DISCHARGE RANGES OF CBS WITH DIFFERENT CAPACITOR
VALUE

Discharge ranges of CBS with different capacitance value for discharging a same amount of energy to load (low end 0.55 V).

Capacitance (pF)		Discharging Range (V) (4)			Energy (pJ)
	20	1	to	0.4	8.4
1.5x	30	0.929	to	0.55	8.4
2x	40	0.85	to	0.55	8.4
2.5x	50	0.799	to	0.55	8.4
3x	60	0.763	to	0.55	8.4

Discharge ranges of CBS with different capacitance value for discharging a same amount of energy to load (low end 0.6 V).

Capacitance (pF)		Discharging Range (V) (5)			Energy (pJ)
	20	1	to	0.4	8.4
1.5x	30	0.959	to	0.6	8.4
2x	40	0.883	to	0.6	8.4
2.5x	50	0.834	to	0.6	8.4
3x	60	0.8	to	0.6	8.4

Discharge ranges of CBS with different capacitance value for discharging a same amount of energy to load (low end 0.65 V).

Capacitance (pF)		Discharging Range (V) (6)			Energy (pJ)
	20	1	to	0.4	8.4
1.5x	30	0.991	to	0.65	8.4
2x	40	0.918	to	0.65	8.4
2.5x	50	0.871	to	0.65	8.4
3x	60	0.838	to	0.65	8.4

APPENDIX E: DISCHARGE RANGES OF CBS WITH DIFFERENT CAPACITOR
VALUE

Discharge ranges of CBS with different capacitance value for discharging a same amount of energy to load (low end 0.7 V).

Capacitance (pF)		Discharging Range (V) (7)			Energy (pJ)
	20	1	to	0.4	8.4
1.5x	30	1.025	to	0.7	8.4
2x	40	0.954	to	0.7	8.4
2.5x	50	0.909	to	0.7	8.4
3x	60	0.877	to	0.7	8.4

