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**State Space Characterisation Under Parameter
Variations and Application to Bifurcation
Based Voltage Sensing**

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STATE SPACE CHARACTERISATION UNDER PARAMETER
VARIATIONS AND APPLICATION TO BIFURCATION BASED
VOLTAGE SENSING

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ABSTRACT

The proliferation of System-on-Chip designs with the integration of analog and mixed signal components on the same platform has led to a dramatic diversification of the specifications for the various circuit blocks. A significant factor contributing to this phenomenon is the dependence of principal circuit behaviour to key system parameters (power supply, operating frequency) occupying either multiple static levels or fluctuating in a dynamic way according to the desired functionality. In addition to high performance applications, parameter variations are also an intrinsic characteristic of energy harvesting designs based on non-deterministic energy sources. In this context, the challenges of analog verification due to the increased number and complexity of operating modes have to be addressed by complementing traditional verification methodology with novel approaches favouring correct by design circuit construction.

This work aims at the investigation of the benefits from the application of dynamical systems theory to the analysis of CMOS circuits under parameter variations. Focusing on circuit blocks which exhibit oscillating modes, the use of nonlinear differential equations for the description of complex dynamics provides valuable insight not possible to be gained by conventional simulation techniques. The explanation with precise mathematical terms of unexpected behaviours leading to operating failures enhances the theoretical basis and contributes actively towards the practical aspects of improving circuit design.

Parameter variations in a circuit displaying oscillating modes may lead to bifurcations which can undermine the correct operation under the predefined specifications. A method based on Floquet theory and Filippov solutions for the exploration of the stability properties of periodic attractors as a system parameter approaches a critical value is developed. Additionally, an automated flow for the characterisation of the structural properties of the state space in unconventional oscillators based on existing techniques and smart implementation of dynamical systems principles on any SPICE simulator complements the set of proposed tools. The verification toolbox provides a solution for the complete mapping of the state space and it can be used not only for the verification of the correct circuit operation but also for the exploration of novel applications of existing structures. Finally, a voltage sensing technique based on the sensing of the onset of an oscillatory mode from a stationary latching behaviour on a circuit which can change operating modes under variable supply voltage is proposed. A circuit realisation of a reference-free and tunable threshold voltage detector is introduced using an autonomous even stage ring oscillator with inherent sensitivity to the power supply.

PUBLICATIONS

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- **I. Syranidis**, D. Giaouris, A. Yakovlev and S. Banerjee, "Stability analysis of limit cycles in CMOS circuits by Floquet theory and Filippov method", in Nonlinear Dynamics of Electronic Systems (NDES), 19th Workshop, India, 2011.

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NOMENCLATURE

A2D	analog to digital
AC	alternate current
AMS	Analog/Mixed-Signal
APS	accelerated parallel simulation
BJT	bipolar junction transistor
CAD	computer aided design
CMOS	complementary metal-oxide semiconductor
CNF	conjunctive normal form
DAE	differential algebraic equation(s)
DC	direct current
DUT	design under test
DVFS	dynamic voltage and frequency scaling
EP	equilibrium point(s)
FPGA	field programmable gate array
FSM	fundamental solution matrix
IC	initial condition(s)
KCL	Kirchhoff's current law
KVL	Kirchhoff's voltage law
LHA	linear hybrid automata
LHPN	labelled hybrid petri nets
MDE	matrix differential equation
MNA	modified nodal analysis
MTBF	mean time between failure
nMOS	N-type metal-oxide semiconductor
ODE	ordinary differential equation(s)
PLL	phase-locked loop
pMOS	P-type metal-oxide semiconductor
POR	Power-on-Reset
PSS	periodic steady state

PVT	process, voltage and temperature
SAT	satisfiability
SMT	satisfiability modulo theory
SOC	System-on-Chip
SPICE	Simulation Program with Integrated Circuit Emphasis
SRAM	static random access memory
TSPV	true single phase clocking
VCO	voltage controlled oscillator
VHDL	Very high speed Hardware Description Language
VLSI	very large scale integration

INTRODUCTION

1.1 MOTIVATION

Analog/Mixed-Signal (AMS) design and verification play an influential role in the further development of the semiconductor industry but they also present many difficult challenges. Although the integration of analog and digital blocks on the same chip results in performance and power efficiency benefits, a series of major problems impede circuit designers. Technology scaling is driven by the digital world and advanced process nodes are not an optimal ground for manufacturing analog functions. The most prominent issue of scalability is that the analog circuits must operate under decreased supply voltage which reduces their operating range and the maximum achievable signal level. Even though different supply voltages can be used for the analog and the digital blocks, increased interference between the two results in fluctuations of the supply voltages, thus, undermining the predefined specifications. Besides the supply voltage complications, the continuously increasing integration rate renders the testability of analog blocks in terms of access in internal circuit nodes extremely difficult. As a result, when a correct by design circuit cannot be constructed, additional circuitry for the implementation of built-in self test is used. Finally, the intensified effect of process and temperature variations in advanced nodes can be ameliorated by self calibration modules which facilitate the smooth progression to newer processes.

The tight interaction of the analog and digital counterparts in a mixed signal design profoundly complicates the verification process. The independent validation of the correct operation of various circuit blocks does not suffice for the validation of the entire design. Besides the essential verification of each analog block in isolation, the designer has to ensure that the analog blocks both operate collectively in harmony and synergetically with the digital block meet the predefined criteria.

Traditional simulation methods not only develop into a major bottleneck in the mixed signal verification process but due to the dramatic diversification of specifications also demonstrate their shortcomings in pure analog environments. A common circumvention to this problem is the over-design of analog blocks with the inclusion of excessive safety margins leading to unreasonable deterioration in area, performance and power metrics. The verification of digitally-controlled analog blocks is another important challenge which indicates the need to either avoid or improve transient simulation. The various operating modes of the analog blocks dictated by different digital inputs along with

the extra complexity imposed by low power techniques such as multiple power domains and power gating, further aggravate the challenge. In order to keep the problems tractable, designers often make numerous assumptions which may be proven wrong after fabrication [1]. These assumptions may lead to undetected failure modes such as oscillator lock-up or pulse swallowing in frequency dividers.

In addition to high performance applications, the emerging field of energy harvesting systems poses further challenges to the verification of the correct operation of circuit blocks. Energy harvesting systems mainly depend on non deterministic power sources which result in an unstable power supply. In order to cope with this uncertainty, circuit designers either alter existing implementations or develop novel designs for certain functions [2, 3]. A wide interval of potential values for the power supply exposes these circuits to a variety of operating conditions which may disclose failure modes that were not accounted for during the pre-fabrication verification phase.

AMS applications are currently one of the major drivers in the electronics and the semiconductor industry [4]. Driven by high demand, the rapid growth of the market has caused existing challenges to surface and many new others to emerge. Despite their undisputed value, existing design methods and tools are highly inefficient in taking into account the plethora of real life design considerations such as process, voltage and temperature variations, power consumption, process constraints and yield. Although the dream of repeating the digital revolution for the creation of highly efficient and fully automated analog design methodologies seems closer than it was 10 years ago, the ingenuity and the knowledge of an expert engineer will still be needed for many years to come. Therefore, there exists both a necessity and an opportunity to develop a verification framework of novel methods, advanced tools and transparent flows based on reliable underlying algorithms and models for the analysis, optimisation and verification of AMS designs.

1.2 RESEARCH GOAL AND MAIN CONTRIBUTIONS

This thesis aims at the assessment of the application of a dynamical systems approach to the analysis and the design of CMOS circuit blocks via the development of realistic dynamical models and the investigation of their behaviour using tools from the dynamical system theory.

Dynamical system theory defines the evolution of the states in a system while focusing on the qualitative transitions among different dynamical regions as inputs and parameters vary. The accomplishment of this objective is articulated in terms of precise characterisation of both the topological features and the corresponding structural properties of the state space.

CMOS circuits are known to exhibit certain forms of behaviour that is outside the scope of the intended specification. The use of nonlinear differential equations for the description of these complex dynamics provides valuable insight not possible to be gained by conventional simulation techniques. The explanation with precise mathematical terms of unexpected behaviours leading to operating failures cannot only enhance the theoretical understanding of such phenomena but also contribute actively towards the practical aspects of improving circuit design and even provide inspiration for novel applications.

The main contributions of this thesis are the following:

- I developed an algorithm for the investigation of the stability properties of periodic solutions in CMOS circuit blocks modelled as a system of ordinary differential equations (ODE). The implementation is based on fundamental dynamical system principles, namely the Floquet theory and the Filippov method.
- I proposed a novel flow for the automated characterisation of the state space in circuit blocks exhibiting oscillating modes. The flow is a combination of existing verification tools interweaved with smart application of principal dynamical system theory using any SPICE simulator.
- I developed a bifurcation based voltage sensing technique and I examined how a transition from a stationary state to motion can be used for the detection of a specific voltage threshold crossing. Based on the that theoretical basis, I investigated the inherent sensitivity of an even stage ring oscillator to supply voltage variations and I proposed a novel reference-free and tunable voltage threshold detector.

1.3 THESIS OUTLINE

This thesis consists of six chapters:

Chapter 2 (*Background*) introduces the basic terminology, concepts and latest research in the three main areas involved in this work: dynamical systems, formal analog verification and voltage sensing.

In Chapter 3 (*Stability analysis of periodic orbits in CMOS circuits*), an algorithm for the stability analysis of periodic solutions in CMOS circuits is developed and implemented using Matlab. A method for the creation of an ODE circuit model based on Kirchhoff's current law (KCL) and a piecewise short channel transistor model is presented. The stability properties of periodic attractors are examined using Floquet theory and Filippov method. An application of the proposed algorithm on a toggle element with variable input frequency concludes the chapter.

Chapter 4 (*State space characterisation in CMOS oscillators*) presents a novel flow for the automated verification via state space characterisation of CMOS blocks exhibiting oscillating

modes. The characterisation proceeds in two independent stages. One stage involves the exhaustive detection and stability analysis of equilibrium points (EP) in the state space using a satisfiability (SAT) based methodology along with basic dynamical system theory. The other stage is concerned with the proof of (non-)existence of periodic orbits in the state space under certain operating conditions using vector field modelling and simulations.

Chapter 5 (*Voltage sensing based on transient mode switching*) introduces the theoretical basis behind a reference-free voltage sensing technique and it investigates how a change in operating modes due to a bifurcation in a system can signal a voltage threshold crossing. A circuit realisation of the method is demonstrated on an even stage ring oscillator with inherent sensitivity to power supply variations. Detailed analysis reveals the complex dynamics and reinforces the proposed sensor as a viable on-chip voltage monitoring solution.

Chapter 6 (*Conclusions*) summarises the contributions of this thesis and discusses directions for future research.

Appendix A includes information about the parameter values used in simulations throughout this work.

2

BACKGROUND

The work presented in this thesis spans three separate areas of research. Firstly, dynamical systems theory provides the mathematical toolbox for the circuit modelling and analysis at an elementary level using ODE. Secondly, formal verification techniques for analog designs are used and integrated into a novel flow for the automated study of certain circuit properties. Thirdly, the application of the findings on the area of voltage sensing completes the bigger picture.

This chapter introduces the basic terminology, concepts and latest research on these areas. Given the vast research space of these fields, only the pieces needed for the complete understanding of the material in this work are presented in detail. Additionally, strict mathematical definitions are avoided and relevant descriptive examples are used instead.

2.1 DYNAMICAL SYSTEMS

2.1.1 *Definition*

A *dynamical system* is a triple $\{T, X, \Phi\}$, where T is the time, X is the state space and Φ is the law of evolution. In simple terms, it is a way of describing the behaviour of a system as it progresses into different states over time, starting from an initial state and following a constant set of laws.

Most natural and artificial systems in disciplines such as engineering, economics, neuroscience and astronomy are represented by mathematical models which are used to make reasonable predictions about future behaviour. In many cases these mathematical models are translated to a set of differential equations that describe the state of the systems undergoing variations over time.

Electronic circuits can be considered to be a collection of discrete elements (capacitors, resistors, inductors, transistors etc.) governed by the fundamental KCL and Kirchhoff's voltage law (KVL). As a result of the basic component definitions, the extracted system for each nonlinear circuit can also be described by a set of ODE. In fact, many of the analyses in the state of the art simulators still use this modelling approach, which was introduced in the early 70's with the SPICE simulator.

In the following sections, each component of a dynamical system is introduced in sufficient detail.

State Space

State space (or phase space) is the set X of all possible states of a dynamical system. Every state of the system, as described by its

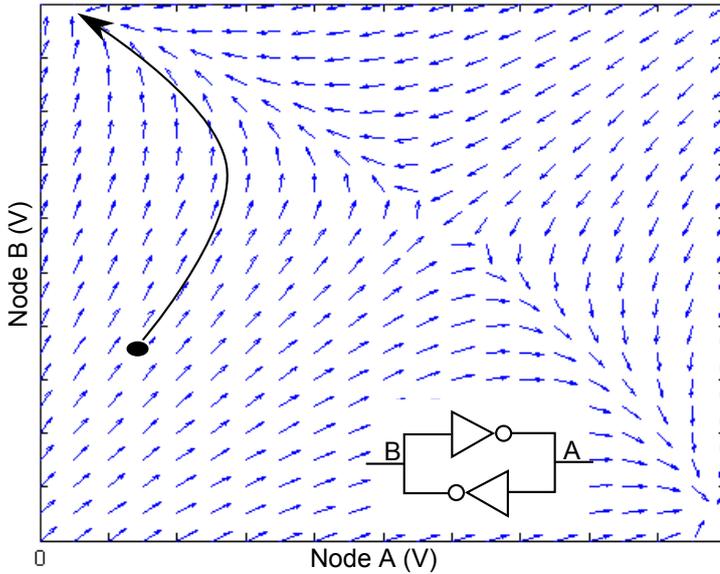


Figure 1: Two-dimensional vector field and a representative solution for a pair of cross-coupled inverters.

state variables, corresponds to a specific point in the state space. For the two-dimensional case, where $X \in \mathfrak{R}^2$, the state space is called *phase plane*.

A better understanding of the behaviour of a dynamical system is achieved by visualizing the geometrical objects that appear in its state space. Given an initial state (or initial condition (IC)), the application of the evolution rule yields a trajectory (orbit) in the state space. The selection of a different IC corresponds to a different trajectory. The set of all trajectories is called *phase portrait* of a dynamical system. For the visualization of the phase portrait only representative trajectories are selected.

An alternative visualization method similar to the phase portrait can be used for 2nd and 3rd order systems. Let a system be defined by a set of ODE written in the form $\dot{V} = f(V(t))$. The right-hand side of this equation calculated at different points V produces a set of solution vectors. The function f that connects \dot{V} to $f(V(t))$ is called *vector field*. Geometrically, these vectors correspond to the direction of the solution flow. Figure 1 shows the vector field and a representative trajectory starting from a random initial condition for a pair of cross-coupled inverters.

The vector field plot can reveal significant information about a system. One of the most straightforward analyses of a vector field is the study of *nullclines*, the geometrical shapes generated by the set of points which produce solution vectors with at least one component equal to 0. The points where nullclines intercept are of major importance because they coincide with the solutions of a system. Additionally, nullclines can be a useful tool for qualitative analysis.

Time

A dynamical system evolves with time t . Time can be either continuous or discrete. Systems modelled with continuous time $t = \mathbb{R}$ are called *continuous-time* dynamical systems and those with discrete time $t = \mathbb{Z}$ are called *discrete-time* dynamical systems. Discrete-time systems can be found in nature and in many other scientific disciplines such as engineering and economics. In this work only continuous-time dynamical systems are considered.

A further distinction can be done in continuous-time dynamical systems according to the effect of time on the vector field of the governing equations. When there is no explicit dependence of the right-hand side of the ODE system on time, the system is called *autonomous*. On the contrary, when the evolution law changes over time, the system is called *non-autonomous*.

Evolution Rule

The most prominent component of a dynamical system is the evolution rule that determines the subsequent states at future times, given a specific IC. In respect to the evolution rule, dynamical systems are divided into two major categories: *smooth* and *piecewise smooth* (or non-smooth). Let the mathematical model of a system be described by $\dot{V} = f(V(t), t)$. The system is said to be smooth if f is differentiable everywhere. If the evolution law is given by various functions f for N different regions of the state space, the system is non-smooth. The general form of a non-smooth system is:

$$\dot{V} = f(V(t), t) = \begin{cases} f_1(V(t), t) & \text{for } V \in \mathfrak{R}_1 \\ f_2(V(t), t) & \text{for } V \in \mathfrak{R}_2 \\ \dots & \\ f_N(V(t), t) & \text{for } V \in \mathfrak{R}_N \end{cases}$$

In this case, the state space is partitioned by $(N - 1)$ hypersurfaces which are called *switching manifolds*. Additionally, $\mathfrak{R}_1, \mathfrak{R}_2, \dots, \mathfrak{R}_N$ do not overlap and cover the whole state space.

Systems with discontinuous right-hand side can be found in nature or they can be a result of a modelling approach. In any case, special care needs to be taken for the analysis using dynamical system methods. A detailed analysis and relevant examples can be found on Chapter 3, where a piecewise transistor model is considered.

2.1.2 Geometrical properties of the state space

State space analysis is a powerful tool for the understanding of the behaviour of a dynamical system. The solutions of the ODE model governing a system lead to a set of geometrical structures

in the state space. These structures manifest themselves as stationary states, periodic solutions and irregular motions. Their location and characterization can reveal invaluable qualitative information. Further details about their properties are presented in the following sections where the ODE model $\dot{V} = f(V(t))$ is assumed.

Stationary solutions and stability

An *equilibrium point* of a dynamical system described by set of ODE is a solution that does not vary with time. These time independent solutions are also called stationary states and exist as points in the state space. A solution v_e is an EP, if $f(v_e) = 0$. It is worth noting that in low dimension systems, equilibria can be located in the state space at the nullcline interceptions. However, finding all EP of a system can be a tedious procedure.

One of the most important general properties of EP in the state space is their stability. *Stability analysis* determines if an EP is attracting or repelling nearby solutions and can be determined by calculating the eigenvalues of the Jacobian matrix of the ODE on the EP. The *Jacobian matrix* of a system is the matrix of all partial derivatives of the vector field with respect to state variables:

$$\text{Jac} = f_v = \frac{\partial f_i}{\partial v_j} = \begin{pmatrix} \frac{\partial f_1}{\partial v_1} & \frac{\partial f_1}{\partial v_2} & \cdots & \frac{\partial f_1}{\partial v_n} \\ \frac{\partial f_2}{\partial v_1} & \frac{\partial f_2}{\partial v_2} & \cdots & \frac{\partial f_2}{\partial v_n} \\ \vdots & \vdots & \ddots & \vdots \\ \frac{\partial f_n}{\partial v_1} & \frac{\partial f_n}{\partial v_2} & \cdots & \frac{\partial f_n}{\partial v_n} \end{pmatrix}$$

An equilibrium is called *asymptotically stable* if all the eigenvalues of the Jacobian have negative real parts. Geometrically, this means that the solutions in the state space with IC in the vicinity (*domain of attraction*) of the EP will be attracted back to the EP as time approaches infinity. On the contrary, an EP is unstable, if at least one eigenvalue has a positive real part. In this case, a small initial perturbation will result in a large deviation and the solution will be repelled from the EP. It is important to note that the study of the stability is local in nature and it is defined for a small initial perturbation.

The classification of the EP can be done in a systematic way by calculating the eigenvalues of the Jacobian matrix on each EP. In the following section, the basic types of EP relevant to the understanding of the material in this work are presented. A generic two- and three-dimensional system is assumed and a visual geometric representation of the different type of EP in the state space is given.

The Jacobian of a smooth two-dimensional system has two eigenvalues μ_1 and μ_2 . These eigenvalues can be either real or complex conjugates. An EP can be classified as:

NODE: $\mu_1, \mu_2 \in \mathfrak{R}$ with $\mu_1 \cdot \mu_2 > 0$ and $\mu_1 \neq \mu_2$

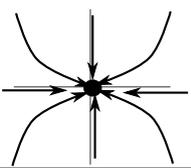
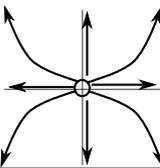
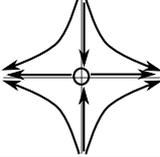
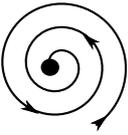
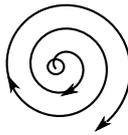
TYPE	Stable	Unstable
Node		
Saddle		
Focus		

Figure 2: Classification of equilibrium points in two dimensions.

When both eigenvalues are negative, small perturbations die out and the node is stable. On the contrary, when both eigenvalues are positive, even a small perturbation leads the solution away from the EP and the node is unstable.

SADDLE: $\mu_1, \mu_2 \in \mathfrak{R}$ with $\mu_1 \cdot \mu_2 < 0$

When the eigenvalues have different signs, the EP is called saddle and it is always unstable.

FOCUS: μ_1, μ_2 are complex conjugates with $\text{Re}\{\mu_1\}, \text{Re}\{\mu_2\} \neq 0$

The orbits near a focus appear as a spiral. Similarly to a node, an EP with negative real part is called stable and with positive real part is called unstable.

A visual inspection of the phase portrait near the EP is shown in Figure 2.

Expanding the classification for three-dimensional systems, it is noted that either one or all three eigenvalues of the Jacobian matrix in this case are real:

NODE: $\mu_1, \mu_2, \mu_3 \in \mathfrak{R}$ and have the same sign

Similarly to the two-dimensional case, when all the eigenvalues are positive (negative) the node is unstable (stable).

SADDLE: $\mu_1, \mu_2, \mu_3 \in \mathfrak{R}$ and have both signs

When there is at least one positive and at least one negative eigenvalue the equilibrium is called saddle and it is always unstable.

FOCUS-NODE: $\mu_1 \in \mathfrak{R}, \mu_2, \mu_3$ are complex conjugates and all have same sign real part

The equilibrium is unstable (stable), when the real part is positive (negative).

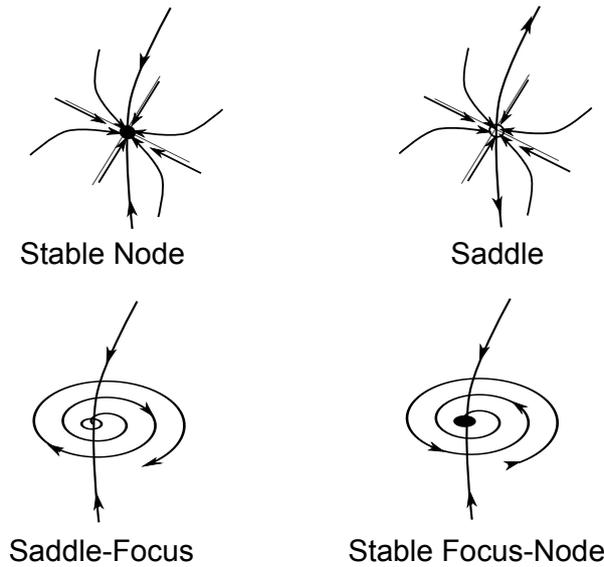


Figure 3: Phase portraits of a selection of three-dimensional equilibria.

SADDLE-FOCUS: $\mu_1 \in \mathfrak{R}$, μ_2, μ_3 are complex conjugates and $\text{Re}\{\mu_1\}, \text{Re}\{\mu_2\}$ have opposite sign to μ_1

In this case the EP is always unstable.

The above classification concerns only stationary solutions with eigenvalues of non-zero real part which are called *hyperbolic*. EP that have one or more eigenvalues with zero real part are called non-hyperbolic and play an important role in the qualitative changes of a system under parameter variations.

Periodic solutions and stability

A solution v of a dynamical system is called periodic if it repeats itself every time t_{PER} (period) such as $v(t + t_{\text{PER}}) = v(t) \forall t$. The periodic orbit in the state space is a closed trajectory called *cycle*. An isolated closed trajectory is called *limit cycle*, meaning that its neighbouring trajectories are not closed but spiral either towards or away from the limit cycle.

Similarly to an EP, an important characteristic of a limit cycle is its stability properties. A stable limit cycle is one which attracts all neighbouring trajectories as time approaches infinity. Such limit cycle is called *attractor*. On the contrary, a limit cycle is unstable, if all neighbouring trajectories are repelled by it.

The analysis of the stability of periodic solutions in smooth systems can be determined mainly by two mathematical tools: the *Poincare map* or the *Floquet theory*. The Poincare method, named after the father of dynamical systems, Henry Poincare, is based on the sampling of the state variables at discrete time points on a Poincare surface and the subsequent study of the resulting discrete-time dynamical system. On the other hand, Floquet theory depends on the analysis of the eigenvalues of the *Monodromy matrix* describing the solution of the system along a periodic or-

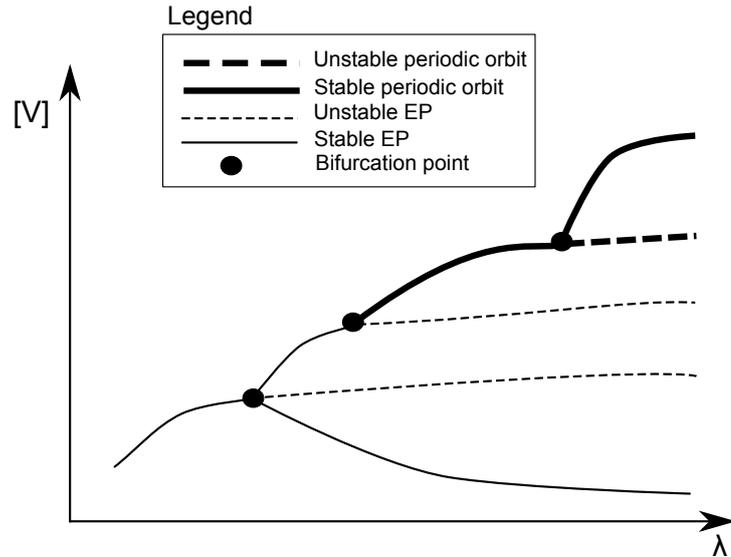


Figure 4: Fictitious bifurcation diagram of generic state variable dependent scalar measure [V] versus bifurcation parameter λ .

bit. Detailed analysis of the Floquet method is given in Chapter 3, where a novel stability analysis method for CMOS circuits is introduced.

2.1.3 Qualitative changes under parameter variations

The evolution rule in most real-life applications depends on a set of independent parameters which describe certain system properties. Examples for these parameters are the control voltage in a voltage controlled oscillator (VCO), the input frequency of a frequency divider, the transistor width of an inverter and the ambient temperature of a temperature sensor. Parameter dependence can be even observed system-wide on chips using the advanced scheme of dynamic voltage and frequency scaling (DVFS) [5]. In many cases, knowledge of the behavioural changes that a system undergoes when a parameter is varied is crucial for its smooth and continuous operation.

The branch of dynamical systems related to the effect of parameter change in a system is called *bifurcation theory*. A bifurcation of a dynamical system is a qualitative change in its state space dynamics under parameter variations. The term "qualitative change" refers to the appearance of topologically inequivalent structures in the state space. For instance, as a parameter is increased in a system, a stationary stable EP may give birth to a periodic solution or two new stable EP. The fictitious bifurcation diagram in Figure 4 shows the structural changes in the state space as the bifurcation parameter λ is increased. The corresponding legend describes the representation of stable and unstable solutions used in this work.

Not all bifurcations are directly observable in the state space. For this reason, a distinction between local and global bifurcations exists. When the analysis for the detection of a qualitative change needs to be performed in a close neighbourhood of an EP, the bifurcation is called local. On the contrary, when focusing on a small part of the state space is not adequate but a complete observation of the state space transformation is necessary, the bifurcation is called global. Closely related to the study of global bifurcations are the notions of *homoclinic* and *heteroclinic* orbits. An orbit Γ starting from a point x_0 in the state space is called homoclinic to an equilibrium x_e , if the solution converges to x_e as time approaches $\pm\infty$. Heteroclinic to equilibriums x_{e1} and x_{e2} is an orbit that converges to x_{e1} as time approaches $+\infty$ and to x_{e2} as time approaches $-\infty$.

The complete qualitative profile of a dynamical system under parametric variations can be depicted on a *bifurcation diagram*. This diagram is a useful way to concisely present information about the behaviour of the system and the transitions to different operating modes for a certain parameter range. One-parameter bifurcation studies can be plotted on a two-dimensional plot, where the horizontal axis is the varying parameter and the vertical axis is a scalar measure V of some state variables. The selection of V depends on the particular system and it is done in a way that allows the display of maximum information on the bifurcation diagram. For two-parameter bifurcations, a more complicated three-dimensional figure, with two axes being the parameters under investigation, can be generated.

The exhaustive identification and characterization of the structural information of a bifurcation diagram is non-trivial and for many complex systems can not be performed at all. Numerical algorithms based on continuation methods are implemented for the solution of this problem. The initial step of a continuation strategy is the location of an EP or a periodic solution for a specific parameter value. Then, by varying the parameter of interest and successively solving the ODE system, a branch of solutions is produced and the bifurcation diagram is plotted. Continuation strategies (called homotopy methods) are also used as a means of overcoming convergence difficulties on a circuit simulators during the DC operating point analysis.

Bifurcations of equilibrium points

One of the most common local bifurcations involving EP in any dimension is the *saddle-node bifurcation* (or fold bifurcation). This phenomenon describes the collision and disappearance of two equilibria in the state space and in the simplest form (normal form) it can be characterized by the 1st order equation:

$$\frac{dv}{dt} = \alpha + v^2$$

with α being the bifurcation parameter and v the state variable. When $\alpha < 0$, there is one unstable EP (saddle) and one stable

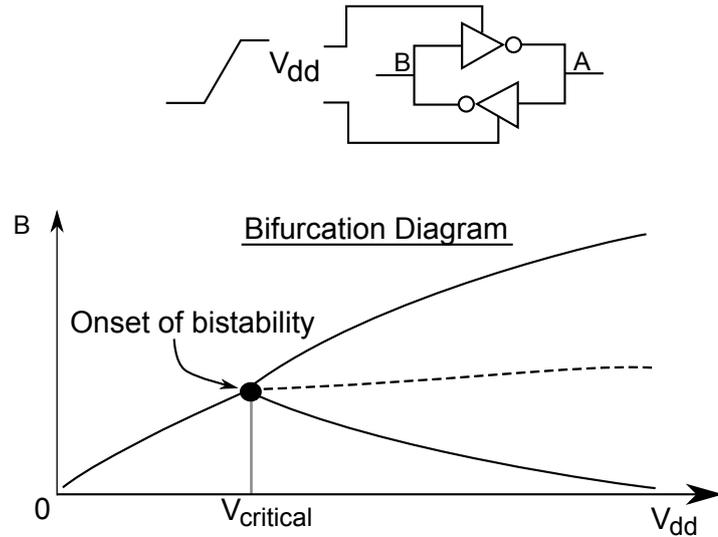


Figure 5: Supercritical pitchfork bifurcation responsible for the onset of bistability in a bistable element as the supply voltage exceeds a critical value.

EP (node). As α approaches 0, the two solutions converge to the same point and at the bifurcation point $\alpha = 0$ they consolidate. Further increase of α to the positive side of the real axis leads to the annihilation of the solutions. Despite the qualitative change, the residue of the catastrophe is still apparent in the state space as the local region attracts nearby trajectories and delays their evolution. The saddle-node bifurcation in higher dimensions is quite similar to the 1st order case. The bifurcation takes place in a subspace of dimension one while the remaining dimensions simply attract or repel the solutions to that subspace. Finally, the point in the bifurcation diagram where a saddle-node bifurcation occurs is also called turning point because the solution seems to "turn". There is no solution on one side but two solutions are born on the other side of a turning point leading to a new branch.

A special case of the saddle-node bifurcation can be encountered when the two EPs in the state space rest on a homoclinic loop. In this case, the vanishing of the saddle-node results in the birth of a limit cycle. This global bifurcation is called *saddle-node homoclinic bifurcation*.

A common local bifurcation which leads to the intersection of two branches in the bifurcation diagram is the *pitchfork bifurcation*. This bifurcation is usually encountered in systems with symmetry and its normal form is given by the following ODE:

$$\frac{dv}{dt} = \alpha \cdot v \pm v^3$$

with α being the bifurcation parameter and v the state variable. A distinction is made based on the sign of the cubic term of the above equation. When the term is positive, the case is called *supercritical pitchfork bifurcation*. For negative values of α there is a stable EP and as the bifurcation parameter exceeds 0 the

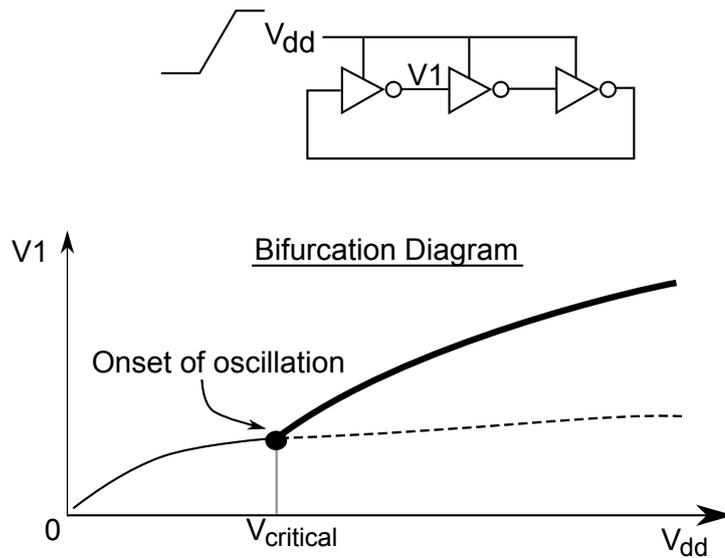


Figure 6: Andronov-Hopf bifurcation responsible for the onset of oscillation in a three-stage ring oscillator as the supply voltage increases to nominal value.

initial branch turns unstable and two new stable branches appear. Figure 5 shows this phenomenon on a bistable element under the power-up operating phase. Initially, a stable EP exists in the state space but as V_{DD} exceeds a critical value the bifurcation signals the onset of bistability. When the cubic term is negative, the case is called *subcritical* pitchfork bifurcation. For positive values of α there is an unstable EP and as the bifurcation parameter crosses 0 the initial EP is substituted by three new EPs, two of which generate unstable branches and the third changes the stability of the initial branch.

Bifurcations of periodic solutions

Periodic solutions undergo bifurcations that impact their existence, structure and stability properties. A commonly encountered bifurcation involving a limit cycle is the *Andronov-Hopf bifurcation*. It is a local bifurcation which denotes the birth or the death of a limit cycle through the change of the stability of an EP via a pair of purely imaginary eigenvalues. As in the pitchfork bifurcation, a supercritical and a subcritical case can be identified. In the supercritical case, when the bifurcation parameter exceeds the critical point, a stable EP becomes unstable and a rising amplitude limit cycle appears. On the contrary, a subcritical case results in the appearance of a stable EP and an unstable limit cycle from an initially unstable stationary solution. The most common occurrence of the Andronov-Hopf bifurcation is on the onset of oscillation in ring oscillators. The bifurcation diagram of Figure 6 depicts the qualitative changes that take place as the power supply V_{DD} is increased from 0V to a constant value. Initially, only a stable EP exists in the state space but as V_{DD} crosses a

critical value, which depends on process parameters and transistor sizes, a stable periodic orbit is created. Additionally, the initial EP changes stability and turns unstable.

Another important type of bifurcation is the *period doubling*. It involves only periodic solutions and it describes the creation of a limit cycle having twice the period of the original orbit. In the supercritical case, which is of interest in this work, as the bifurcation parameter crosses the critical value, a stable limit cycle of period T bifurcates to an unstable limit cycle of the same period, while a new periodic solution of period $2T$ appears in the state space. Also, it is worth noting that a common pathway for dynamical systems to irregular motion (chaotic behaviour) is a succession of period doubling bifurcation.

2.1.4 *Analysis of electronic circuits using dynamical systems theory*

The mathematical toolbox provided by dynamical systems theory has always been at the forefront on the analysis of electronic circuits. Besides the fundamental formulation of differential algebraic equation (DAE) in all SPICE-like circuit simulators, plenty of different mathematical tools are used to tackle specific circuit problems related not only to the analysis but also to the design of novel circuit structures.

In recent years, there has been an increasing amount of literature on the stability analysis of SRAM cells. The main part of a typical SRAM cell is a pair of cross-coupled inverters and its phase plane contains two stable EPs and one unstable EP which is usually called metastable. Despite the simplicity of the design, an SRAM cell is a nonlinear system governed by complex dynamics. The goal of the stability analysis is to determine the maximum amount of input noise that the cell can tolerate without changing its state during the hold, read and write operations. Traditionally, the characterization of an SRAM cell has been done using the butterfly curves [6] generated by the simulation of an equivalent static circuit. The result of this analysis is the static noise margins which served the industry well for many years.

Advances in the fabrication process and technology scaling have considerably decreased the noise margins mainly because of the accompanying scaling of the supply voltage. In addition, increased process variability results in significant device variations that directly influence the stability margins. For these reasons, the notion of dynamic stability margins was introduced, trying to capture the nonlinear dynamical characteristics of an SRAM cell and to provide important design information. Zhang et al [7] apply dynamical system theory and based on a simple ODE model for the SRAM cell derive a closed form expression that determines if the perturbation induced by noise source of a certain magnitude is suppressed or flips the state of the cell.

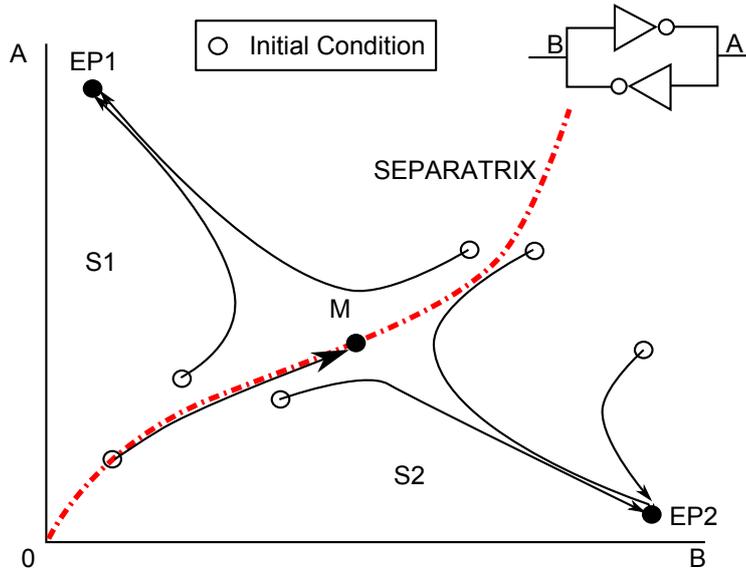


Figure 7: Bistable element separatrix and trajectories starting from random IC in the state space.

The main focus of the dynamic analysis is the location of the *separatrix* in the state space. The separatrix can be regarded as the set of points that drive the cell to the metastable state M . Geometrically, it is a boundary which separates the state space into two areas $S1$ and $S2$ which correspond to two sets of IC that lead respectively to the stable equilibria $EP1$ and $EP2$ (Figure 7). The stability of the cell is lost when an external noise source forces the state variables to cross the separatrix. A fast SRAM separatrix tracing algorithm with SPICE-level accuracy for the study of the variability on a cell is presented in [8, 9]. First, the metastable point is located and then the two sections of the separatrix are traced by running two transient simulations with backward-time integration. The IC for the simulations are taken by slightly perturbing the unstable EP to the opposite directions of the separatrix branches. Unfortunately, the accuracy of this method is accompanied by a high level of complexity for the implementation, as an alteration of the SPICE simulator code must be done. A trade-off between a speed and complexity can be achieved by an alternative method presented in [10], which does not require a custom simulator. The basic characteristic of this approach is the generation of a two-dimensional vector field for an SRAM cell by running a set of DC simulations. The separatrix is then traced by vector interpolation starting at the neighbourhood of the metastable point. An advantage of this method is that it can successfully be applied to an arbitrary SRAM cell.

Circuit analysis based on dynamical system theory has also been extensively applied to the field of synchronization and arbitration of digital systems. In its most basic form, a synchronizer is nothing more than a two-input latch connecting two different time domains on a chip. Similar in structure to an SRAM cell, the core of its operation is a bistable element responsible for an

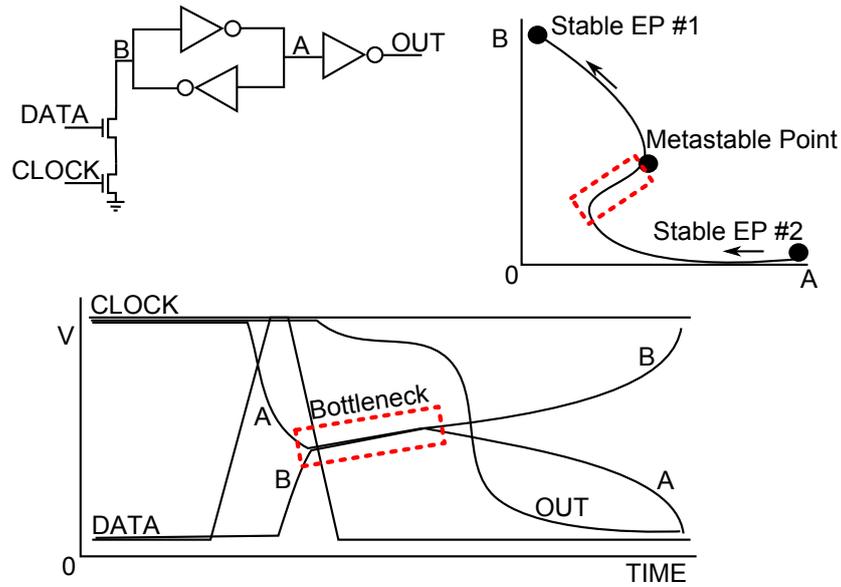


Figure 8: Metastability illustration on a Jamb latch synchronizer [11].

unstable solution in the state space which is the reason for the highly undesirable phenomenon of metastability. When the time difference of the two synchronizer inputs is below a critical value, the resolution time of the synchronizer can increase considerably because the solution of the system is led to the bottleneck introduced by the metastable point. Figure 8 illustrates this behaviour on a Jamb latch used as a synchronizer both with a signal plot of the node voltages versus time and with a plot on the AB space where the stable EP and the metastable point are clearly visible. The modelling of metastability is done using a small-signal ODE model for the cross-coupled inverter pair [11] and the quantitative characterization of this phenomenon is achieved by the expression of mean time between failure (MTBF).

The most prevalent way to analyse a synchronizer behaviour and calculate MTBF is simulation based on numerical integration. However, increasing operating frequencies make the calculation of the low synchronizer failure probabilities difficult because of the numerical instability errors due to the floating-number resolution of the simulators. A solution for this problem is offered in [12] where the authors propose a custom simulation method that combines the traditional simulation with a small-signal dynamical model for the operation around the unstable EP.

A small signal ODE model was also introduced for the analysis of the three-way arbiter in [13]. The authors initially classify all possible stable and unstable states of the circuit depending of the input combinations. Then, they discuss a treacherous oscillatory state which can undermine the correct operation of the circuit (Figure 9). They conclude with the presentation of findings about the effect of different circuit parameters (asymmetry in capacitive load, transconductance, parasitics) based on the ODE

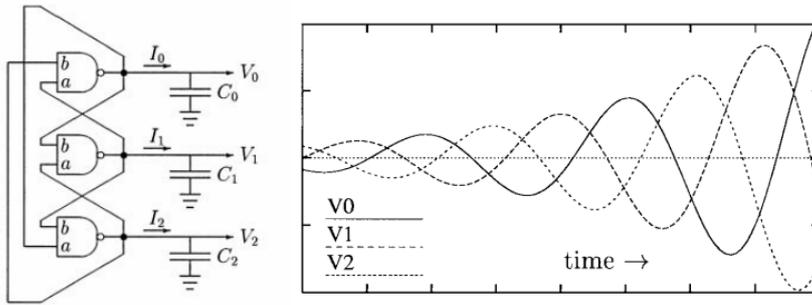


Figure 9: Simplified tri-flop circuit and plot of the node voltages displaying the onset of oscillatory behaviour [13].

model of the circuit. Maevsky et al in [14] extend the analysis by providing a detailed set of oscillatory conditions using a more accurate dynamical circuit model.

In general, bifurcations are regarded undesirable phenomena because they alter the predefined behaviour of a system. Nevertheless, qualitative changes in the state space via parameter control can give birth to new ideas for applications that take advantage of these occurrences [15]. The authors of [16, 17] apply rigorous dynamical systems theory and propose a method for the stability analysis of periodic orbits in DC-DC converters based on the ODE model of the circuit. They also describe the bifurcation that takes place as the input voltage is increased and propose a converter for the delay of the bifurcation based on the valuable information extracted by the dynamical analysis. A case where the occurrence of a bifurcation is beneficial for the circuit is given in [18] where a novel CMOS differential positive feedback amplifier is analysed. According to the amplifier's dynamics described by the nonlinear model of the circuit, the author proves that detecting the critical point and digitally tuning the circuit's parameters during operation in order to keep the operating point near the bifurcation area, is an effective way to increase the amplifier gain. In another study [19], the different modes of free-running oscillators are analysed and dependence of their stability properties on circuit parameters such as bias voltages is studied using bifurcation theory. It is worth noting that bifurcations can also be used as a means of circuit synthesis. Researchers in [20] designed a silicon neuron with controlled spiking based on a saddle-node bifurcation. The nullcline-based methodology assists the circuit synthesis and enables the biasing of a circuit to the desired section of the parameter space. Finally, authors in [21] provide a qualitative analysis for a toggle element under input frequency variations. A detailed analysis with a similar example using the stability analysis proposed in this thesis can be found in Chapter 3.

As it was described earlier, bifurcations are the means for the transition from a stationary or regular motion to an irregular motion called chaos. Chaotic behaviour has traditionally been

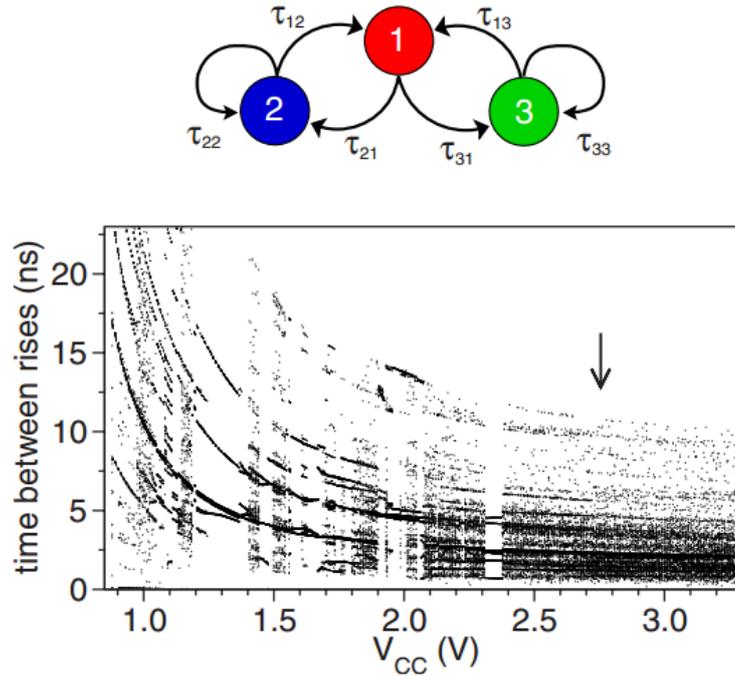


Figure 10: Network diagram of autonomous Boolean network and resulting bifurcation diagram under variable supply voltage V_{CC}) [23]. The "time between rises" refers to the time difference between two successive rising transitions of a node voltage of the network.

observed in many microelectronic circuits. For instance, in an older study [22] chaotic behaviour is observed in a CMOS ring oscillator. Although many occurrences of chaos have been described, the general consensus is that in the micro- and nano-regime chaotic behaviour is difficult to control.

Despite the difficulties in harnessing chaotic behaviours in CMOS circuits, chaos has always been a fascinating subject for scientists and researchers. Two of the latest developments in this area are Boolean chaos and chaos computing.

Boolean chaos is a combination of deterministic chaos, a fast divergence of solutions starting in nearby IC in the state space, and Boolean networks, a simplified description of nonlinear networks using a switch-like behaviour [24]. The application of the theoretical findings of Boolean chaos was demonstrated in an autonomous network of three basic XOR gates connected to each other with independent delays (Figure 10 top). In [23], it is shown that the consideration of the power supply as bifurcation parameter in the circuit leads to windows of periodic behaviour among a plethora of chaotic orbits in the bifurcation diagram (Figure 10 bottom). The ultra-wideband frequency spectrum of this circuit is proposed as an inexpensive source in spread-spectrum communication systems.

Chaos computing [26] is a general theoretical framework for the exploitation of chaotic behaviour in favour of computational flexibility. The main idea is the usage of a single polymorphic

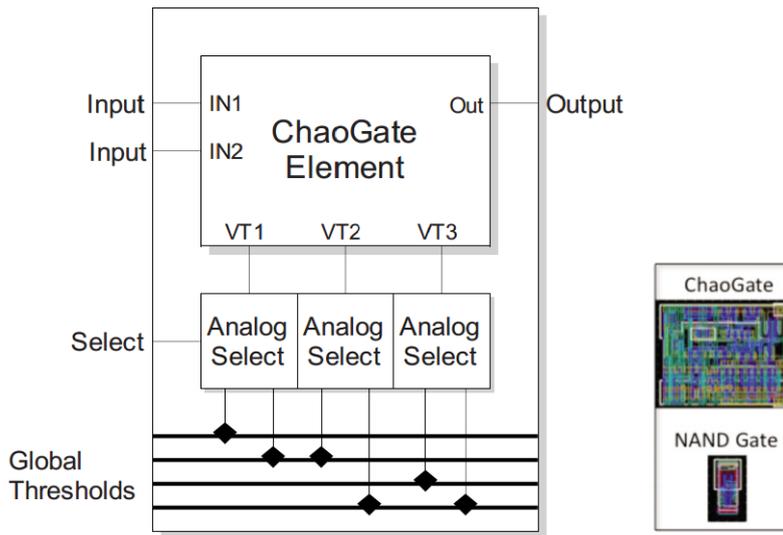


Figure 11: On the left side, schematic representation of a morphable gate with two inputs and one output. The functionality of the gate (AND, OR, XOR) can be controlled by the global control voltages VT_1 , VT_2 and VT_3 through an analog multiplexer. On the right side, comparison between a conventional NAND gate and a chaogate VLSI implementation [25].

chaotic element described by a nonlinear ODE model for the emulation of many different logic gates and the ability to select among a set of operating behaviours by controlling an external system parameter. An element based on the above principle allows a flexible and dynamic system architecture which can offer a wide range of advantages in comparison to current reconfigurable systems (e.g. FPGA). The study in [27] presents a circuit implementation using discrete components and show how the dynamic control of an external voltage signal determines the logic operation of a generic logic gate (chaogate Figure 11). Additionally, the authors of [25] claim that a proof of concept VLSI chip was able to perform according to theory and managed to change its arithmetic functionality (multiplier, adder) in less than one clock cycle.

In another study, a nonlinear approach for controlling chaos in a PLL is proposed [28]. The control algorithm and the mathematical methods are presented in detail, although verification of the findings is given only by simulations.

2.2 FORMAL VERIFICATION OF ANALOG DESIGNS

2.2.1 Introduction

Formal verification is a systematic process of ensuring through exhaustive algorithmic techniques that a design implementation satisfies the requirements of its specification [29]. This definition captures some important elements: systematic, exhaustiveness,

specification. The verification engineer initially specifies a set of properties that need to be checked, such as temporal logic expressions. The properties that need to be checked are then input in a verification tool that applies different algorithms on the design model which can be mathematically described in a plethora of ways (differential equations, symbolic, hybrid etc.). These algorithms exhaustively explore the design model until initial set of properties is verified or disproved. The main advantage of formal verification methods is the exhaustiveness of the final result. If the mathematical representation of a system is correct and the set of properties precisely characterize the required specifications, then the engineer can be certain that the result of the analysis is valid throughout the given design space.

In recent years, formal approaches have gained ground and utterly advanced digital circuit design. Standard simulation based techniques have been reinforced by newly developed algorithms that can handle Boolean functions. These advances led to the radical update of the digital design flows and the integration of novel CAD tools that allowed the verification and fabrication of designs consisting of hundred of millions of devices.

Despite the advances in digital design, formal verification of AMS designs is still lagging. The most prominent verification method for circuit blocks such as operational amplifiers, comparators, A2D converters and VCO is still SPICE simulation. Although updated computing and modelling algorithms which can exploit multicore computing environments can be found in state of the art commercial simulators (Cadence APS simulator), the foundation of the analog circuit verification remains similar to the foundational principles of the first SPICE simulator many decades ago.

The answer to the question, "Do analog designers need novel formal verification methods?", is quite straightforward. The challenges for AMS designs have been constantly increasing during the last years. On a fundamental level, most fabrication processes are not analog-friendly as they are optimized for the digital part of the circuit. Also, technology scaling introduced many additional variables that need to be taken into account during the design and verification phase. Process, voltage and temperature variations span wide operating ranges. Moreover, physical effects not prominent in previous technology nodes start to play an important role and they must be accounted for.

The correct operation of the circuit across the many corners of the design space needs to be verified. Currently, this is achieved by running a large amount of simulations which is extremely time consuming. Moreover, the results of the simulation runs cannot be considered exhaustive. For example, even if a design under test is simulated for a large number of parameter values and successfully meets the specifications, the designer can never be certain that the actual design will still function properly after fabrication because a certain untested parameter value may

lead to a failure. Formal verification of AMS designs can improve the predictability and allow correct by design circuits. The main problem with the application of digital domain formal methods to the analog domain is the continuity of the voltage and current variables which represent useful circuit quantities.

Verification methods for analog circuits can be grouped into two main categories: simulation and formal verification. SPICE simulation is still the verification cornerstone for analog designs. In order to better cover the expanded verification space, the analog designer uses methods such as corner and Monte Carlo analysis. In corner analysis, the design under test (DUT) is simulated under all process corners and the verification is successful when the specifications are met in every corner. Apart from the inability to guarantee correct circuit operation for the whole continuous parameter space, this method often leads to overdesign. On the contrary, Monte Carlo analysis generates statistical distributions based on a large number of simulation runs. Regardless of total simulations the design can never be exhaustively verified.

Formal analog verification can be split into theory proving methods and state space exploration methods. In theory proving, a mathematical proof that the specifications are met by a model is constructed using inference rules and axioms. Satisfiability Modulo Theory (SMT) solvers are usually used in theory proving. A disadvantage of this method is the high dependence of the outcome on the correct problem understanding and input generation by the user. State space exploration methods can be easily automated but suffer from the state explosion problem, which can be alleviated in certain problems by abstraction and refinement techniques [30]. These methods can be further split into equivalence checking and model checking. On one hand, in equivalence checking, the outputs of two different models are compared for a set of similar input conditions without the need of a mathematical proof. On the other hand, in model checking all possible behaviours of a design are described by a transition system that covers the state space.

Verification of analog and AMS designs using formal techniques is difficult to follow a generalized scheme because of the different analyses (DC operating point, transient, AC, period steady state (PSS) etc.) and the numerous properties needed to be verified. Ideally, the input of a formal verification algorithm would be a netlist and a set properties that need to be proved and the output a YES/NO answer with some additional hints for the alteration of design in case of a negative output.

In this work, exhaustive detection of the operating points of a circuit is required in order to prove correct functionality. The analysis used by state of the art simulators for the establishment of the DC operating point of a circuit is called DC analysis. Its main drawback is the local nature of the search algorithm which only returns one operating point depending on the initial solution guess. In this section, the DC analysis of the SPICE simulator

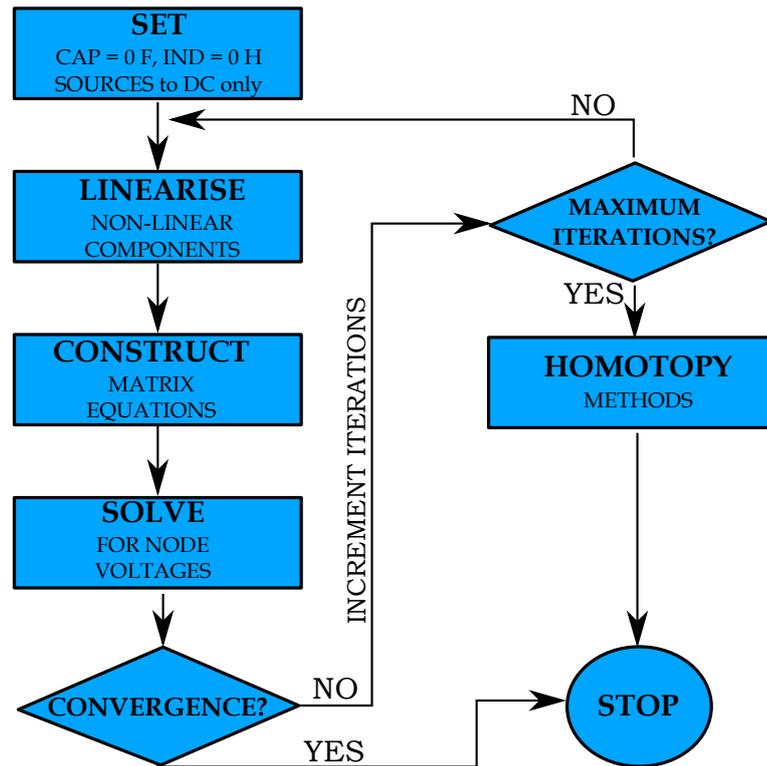


Figure 12: Flowchart for the DC algorithm in SPICE simulators.

is presented in detail in order to elucidate the problems that may arise by its use. The formal approaches in the literature that attempt to substitute or augment DC analysis follow. Completing the bigger picture, this section closes with the main advances in the formal analog verification accompanied by the application of the techniques in real life examples.

2.2.2 Locating equilibrium points

DC operating point algorithm

DC analysis is used to establish a single operating point of the circuit under verification. It is an important analysis, either as a stand alone tool or as an initial step for the successful completion of other analyses such as the transient, the AC and the PSS.

As the notion of time does not exist in DC analysis, capacitors, inductors and time varying supplies receive special treatment. By default, the capacitors in the circuit are replaced with open circuits (0F capacitance), the inductors are replaced with short circuits (0H inductance), the static supplies operate under their nominal values and only the DC component is used for the time varying signal sources.

DC analysis is an iterative process of circuit linearisation and solution until certain convergence criteria are met. The basis of the analysis is KCL enhanced by KVL equations where necessary. Using nodal analysis, the matrix equation:

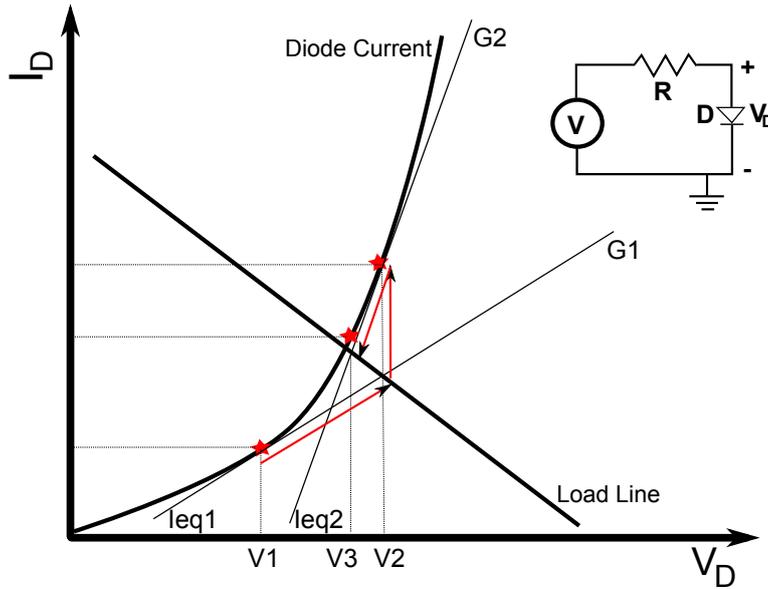


Figure 13: Graphical representation of the Newton algorithm.

$$\mathbf{Y} \cdot \mathbf{v} = \mathbf{J}$$

which describes the circuit is constructed. \mathbf{Y} is the nodal admittance matrix, \mathbf{J} is the current source vector input and \mathbf{v} is the input vector of the node voltages. The elements of the nodal matrix equation are filled by the simulator in a procedural way. The contribution of each circuit element is characterized by a matrix stamp and its location in the nodal matrix is defined by the connection of the element terminals to the circuit nodes as described in the circuit netlist.

DC analysis is straightforward in circuits with only linear components. Nonlinear devices such as diodes, CMOS and BJT transistors add an extra linearisation step in the nodal equation construction. For these devices the simulator based on the model equations calculates a linearised equivalent set of values (G_{eq} , I_{eq}) which functions as a matrix stamp. For the linearisation of the nonlinear components, the Newton-Raphson method is used. As the exact operating point of nonlinear devices is not known, an initial guess for the Newton-Raphson iterations is chosen by the simulator based on the estimated operating region that is set on the device. An overview of a typical DC algorithm for SPICE simulators is presented in Figure 12.

The iterative linearisation procedure can be graphically seen in Figure 13 on the simple diode-resistor circuit. The diode equations are used to calculate the tangent $G1$ and the I_D axis intercept of the tangent I_{eq1} at the first guess $V1$. These are used along with the resistor and supply to construct and solve the matrix. This gives a new voltage $V2$. This is the first Newton-Raphson iteration. From this second voltage, the tangent to the curve is calculated again. The first derivative of the diode curve equation supplies the slope of the tangent $G2$. The Y axis intercept I_{eq2} is calculated as well. The new matrix derived from the

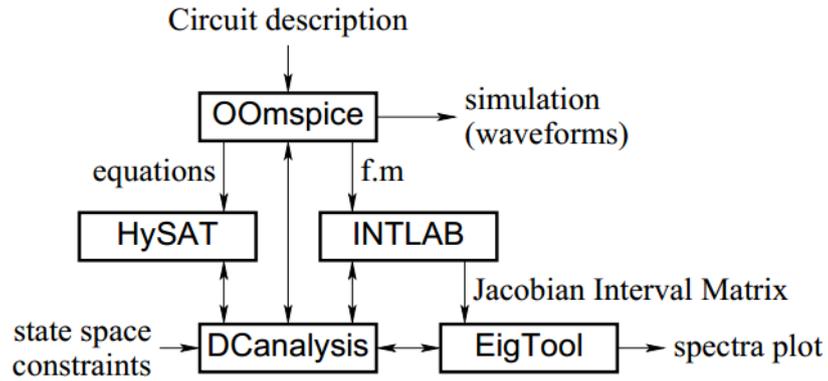


Figure 14: Proposed flow for the analysis of DC operating points [31].

circuit can now be constructed and solved. From this matrix, a new solution V_3 for the operating point is calculated. This is the end of the second iteration.

In this example, each time the solution gets closer, but the exact solution can never be achieved. The simulator stops iterating when certain convergence criteria are met. These criteria are based on the difference between two successive iterations for the nonlinear branch currents, the node voltages and the KCL on each node. They are controlled by a set of variables set by the user ($IABSTOL$, $VABSTOL$, $RELTOL$).

The convergence of Newton-Raphson method is not guaranteed for every circuit. In case of non-convergence, the simulator resorts to continuation methods controlled by the homotopy parameter. These methods modify the circuit so that the solution is easy to compute and then gradually change the circuit back to its original form. The default option *gmin stepping* works as follows. A simulation is performed with 1 Ohm resistors placed in parallel with all nonlinear devices making the circuit very linear, so the simulator will succeed in calculating the voltages. If the solution does not converge, the *gmin* resistors are lowered in stages until 1mOhm is reached. When convergence is reached, the simulator slowly increases the value of the resistors while using the previous solution as the first guess for the current solution. The simulator continues to increase the value of the *gmin* resistors until they reach the value set by *gmin*.

Finding multiple DC operating points

Zaki et al [31] present a novel flow for the analysis of DC operating points. A set of public tools (HySat, IntLab, EigTool) along with the proprietary OOmspice symbolic circuit model generator is used (Figure 14). Initially, a symbolic circuit model is generated by OOmspice and fed into HySat in combination with a set of state space constraints. HySat is an unsatisfiability solver for boolean combination of arithmetic constraints and its output are a set of intervals that may contain a DC operating point. The regions identified by Hysat are then further refined by IntLab. For the hyperrectangles that contain an EP, a Jacobian inter-

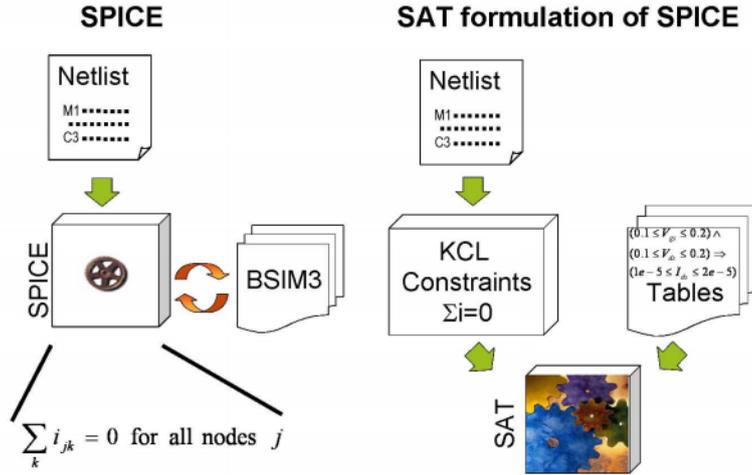


Figure 15: Comparison between SPICE and SAT-based circuit simulation [30].

val matrix is produced and the concept of matrix pseudospectra is used in order to check for stability. Finally, the spectrum is plotted using the EigTool. Although this method was successfully applied to a series of trivial circuits, it still carries a few drawbacks. Firstly, Oomspice creates a symbolic representation of the circuit using simple transistor equations. In practice, due to this limitation the results of the analysis can never reflect the actual DC operating points of a real life circuit. Also, symbolic circuit models are known to have inherent scalability problems. Secondly, the proposed flow integrates many tools from different areas and the increased complexity is a limiting factor for its practical application.

Tiwarly et al [30] also use boolean satisfiability methods for the detection of DC EP. They present a SPICE-like simulator called fSpice that solves the multiple DC operating points problem as a satisfiability problem. The basic differences to the conventional SPICE flow can be seen in Figure 15. A transistor level netlist is generated and given as an input to the solver (Yices [32] is used in this study). The analysis of the netlist automatically creates a set of constraints based on the fundamental KCL equations that is also used by traditional SPICE engines. The V-I nonlinearity imposed by the circuit elements is captured as conservative approximations in the form of tables and since the input is a set of intervals, the output is a set of interval as well. The SAT-Solver exhaustively searches the state space for intervals with potential solutions. The final output is a set of intervals that may contain a solution. The uncertainty exists because the conservative way of creating the V-I tables. An advantage of this method is the fully automated flow that does not need user intervention and also the ability to create custom constraints based on parameters such as W , L , tox etc. A detailed analysis of this method is presented in Chapter 4.

Authors in [33] present a pen and pencil approach for the detection of all DC points in an even stage ring oscillator. The analysis begins with the formulation of a set of KCL equations for each node of the circuit and the DC EP are located by searching where the total current flowing into each node is zero ($\frac{dV}{dt} = 0$). By taking into account simple observations about the monotonicity of the transistor current, the authors first simplify the problem to a search in a two-dimensional space and then further reduce it to a one-dimensional search. The major advantage of this approach is the simplicity both in terms of understanding and application. On the negative side, this method is mainly applicable to structures bearing similar characteristics as the even stage ring oscillator analysed in this study and it is difficult to be generalized.

In a more broad overview of the DC analysis literature many studies based on a wide variety of ideas attempt to find most operating points of a circuit. Initially used in diode and BJT circuits [34], a mathematical concept called deflation is applied to CMOS circuits [35]. The main characteristic of this approach is the modification of the equations describing the circuit in order to avoid the already calculated solutions and retain only the remaining solutions. Although not formal in nature, in most of the analysed circuits the DC op number agrees with the expectations. On a completely different approach, Crutchley and Zwolinski [36] propose the use of ideas from evolutionary computing for the detection of multiple EP. In particular, they show how Evolution Strategies and Differential Evolution can be applied to DC analysis and they present the advantages over the Newton-Raphson method. A new hybrid algorithm called Differential Evolution Initialized Newton-Raphson that has the advantages of both worlds is proposed and a custom built SPICE compatible evolutionary circuit simulator (Evolutionary Analogue Circuit Simulator) is presented.

2.2.3 *Verifying other properties*

As the formal analog verification methods are not yet mature enough in order to be implemented in a generalized verification framework, the scientific literature is abundant in ad hoc solutions. Most of these solutions tackle very specific verification questions and they can be applied on restricted circuit classes only. Their fundamental difference is the modelling approach which is the basis for the subsequent analysis techniques.

Significant advances in analog verification methods have been achieved by Yan and Greenstreet [37, 38, 39] with their Coho verification tool. Their analysis is based on a reachability method for verifying real circuits. In general, given a system with a predefined set of rules T and acceptable states, reachability refers to whether a specific state is reachable from an initial state by successively applying T . In Coho, an approximation of the non-linear ODE model \dot{x} of the circuit is generated by using linear

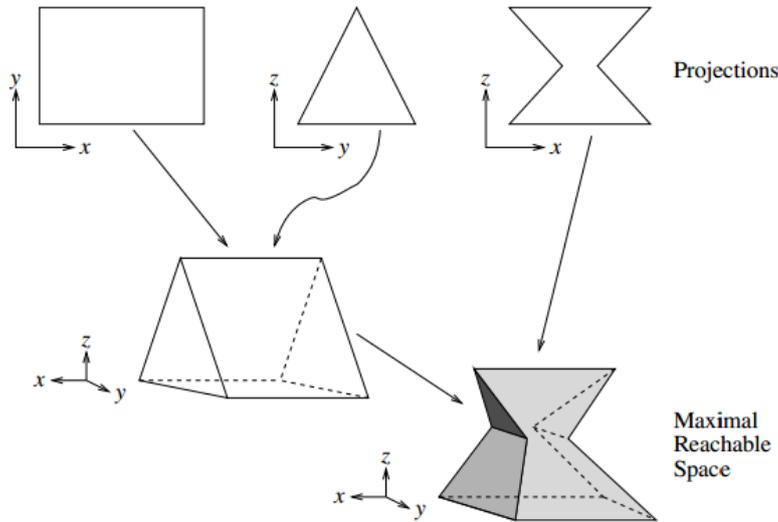


Figure 16: Projectagon representation in three-dimensional space [37].

differential inclusions of the form $Ax + b - u \leq \dot{x} \leq Ax + b + u$ and the reachable space is expressed in terms of projectagons which are projections of high-dimensional polyhedra onto high-dimensional subspaces (Figure 16). The inequalities introduced by the modelling approach are expressed as linear programming inequality constraints, efficiently solved by Coho's linear solver. Because of the overapproximation of the reachable space the results of this analysis are sound and formal in nature. Coho has been successfully used for the verification of a high speed toggle element and also for an arbiter circuit.

Circuits exhibiting periodic behaviours are attractive candidates for reachability methods. Verification of cyclic properties can be done by proving the existence of a cyclic invariant. In plain words, it must be shown that all behaviours starting from a set of initial states T return to a subset of T . The aim of the formal verification of oscillator properties is to expand the single trajectory produced by traditional simulation techniques (shooting method, harmonic balance) and to consider multiple traces in the neighbourhood of the periodic orbit simultaneously. In [40], the dynamics of a differential VCO are modelled using the PHAVer solver. PHAVer operates on linear hybrid automata (LHA) which by definition contain both discrete and continuous components. Similarly to differential inclusions, LHA are characterized by a set of states and linear inequalities defining transitions. For the computation of the reachable states, PHAVer uses a polyhedral representation and overapproximation based on affine dynamics. The novelty of this research is the implementation of forward and backward abstraction refinement techniques for the faster and more computationally effective calculation of the behavioural invariants in situations where using only forward reachability fails to produce a successful result. Figure 17 shows a comparison of the basic forward reachability analysis algorithm against the enhanced version with forward/backward

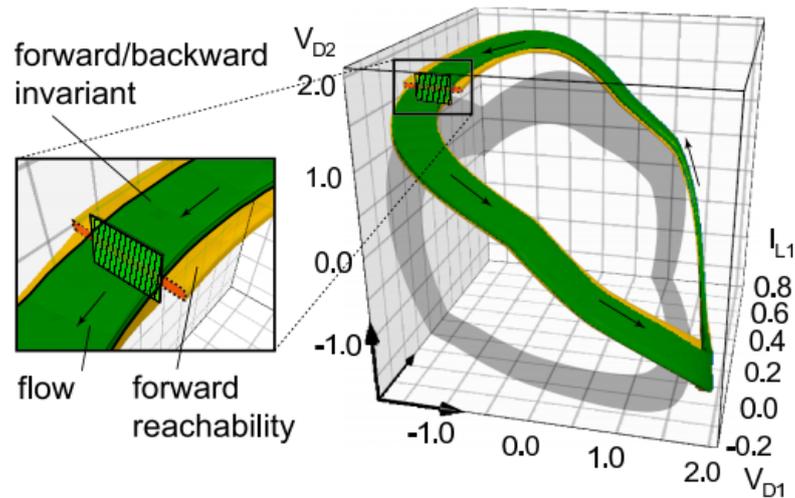


Figure 17: Comparison of typical forward reachability analysis with enhanced forward/backward refinement version in VCO [40].

refinement. In the first case the solver failed to calculate an invariant (yellow stripe) but using forward/backward refinement, a set of final states confined in the IC set were computed and an invariant was proven (green stripe). Although these techniques can be extended to include parametric variations, it is worth noting that they currently use a basic transistor model.

A different modelling approach for AMS designs focusing on overcoming the problems of previous models (timed automata, timed Petri nets, hybrid automata, hybrid Petri nets) targeting the VHDL-AMS compiler is presented in [41]. The labelled hybrid Petri nets (LHPN) model is used for the verification of a switched capacitor integrator circuit. The advantage of this model is that it can be easily generated by a standard hardware description language for AMS circuits or even directly from simulation results. Verification of LHPN properties is achieved using reachability analysis and a novel algorithm using a process that allows zones to describe continuous variables changing at variable rates is presented. The major bet of this methodology is the additional improvements to tackle the scalability problem.

In a more analog-centric formal verification domain, many researches propose solutions to different problems. Steinhorst and Hedrich [42] propose the improvement of the verification coverage of analog circuit blocks by state space guided simulation by developing a property verification and an equivalence checking methodology. Their analysis is based on the transfer of the continuous state space of the circuit described by modified nodal analysis (MNA) equations of the form $f(\dot{x}(t), x(t), u(t)) = 0$, where $u(t)$ is the input signal, to a discrete graph data structure. Effectively, the state space is partitioned into areas of homogeneous behaviour represented by hypercubes and input stimulus is generated by optimally visiting all discrete areas of the state space. A top level of view the methodology can be seen in

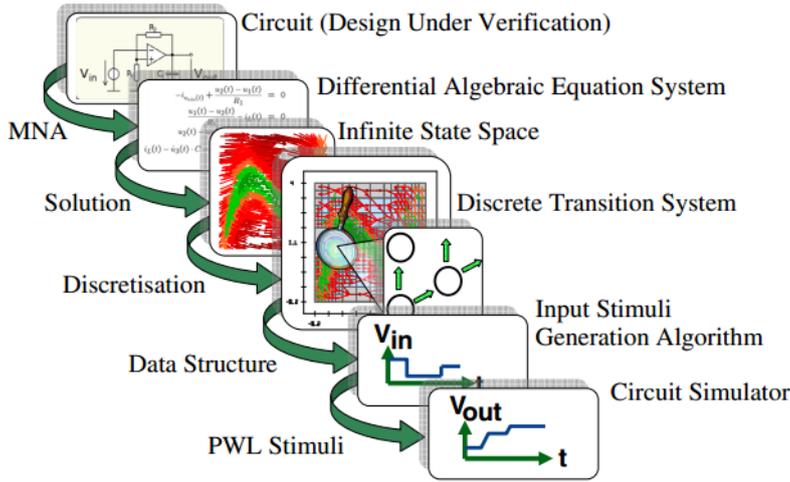


Figure 18: Analysis flow for the verification coverage of analog circuit blocks by state space guided simulation using discrete state space modelling [42].

Figure 18. The algorithm was successfully applied for the verification of overshoot properties of a Sallen-Key biquad low pass filter and also for the equivalence checking of a second order delta sigma modulator to a simple behavioural model. The advantage of this methodology is the automated nature of the input stimuli generation which can be accompanied by visual inspection from a verification engineer because of the transparency of the analysis.

Focused on the formal verification in the presence of noise and process variation, researchers in [43] model and verify an inverting Op-Amp and a Band Gap reference circuit using MetiTraski. MetiTarski is an automatic theorem prover based on a combination of resolution and a decision procedure for the theory of real closed fields. Starting from an ODE description of a circuit, a stochastic process representing the noise behaviour is included in the equations. The resulting set is a system of SDE that can be fed in the solver along with a representation of the verification property as an inequality over special functions. The proposed approach is limited to linear invariant designs and requires manual labour for the generation of the SDE.

On a similar subject, Grabowski et al [44] propose a semi-symbolic modelling and simulation approach in order to tackle the problems of device mismatch and process variation. They reformulate the basic MNA equations in order to include vectors containing parameter expressions based on affine arithmetic. The result of the simulation is not a single trace but a range capturing all potential simulation results obtained by varying a parameter in a certain range. A proof of concept simulation is presented on an active bandpass filter but the complexity of the methodology and the need for a custom simulator is a major disadvantage.

2.3 VOLTAGE SENSING

2.3.1 *Introduction*

In recent years, increased demand for high performance applications has paved the way for the proliferation of System-on-Chip (SOC) designs which provide a common ground for the integration of different building blocks on the same chip. The co-existence of the analog and the digital domain rendered multiple power supply levels necessary. Furthermore, advanced schemes such as the dynamic voltage and frequency scaling [45] can dynamically adjust the supply voltage to predefined levels in order to optimise the performance and power profile of a design.

In addition to the recent advances in high performance applications, the emerging field of energy harvesting systems [46, 47] has gained the interest of the research community. These systems depend on unpredictable power sources and the determinism of the power supply can not be guaranteed. The most common design consists of a series connection of an energy harvester followed by a rectifier and a DC-DC converter charging a supercapacitor, which acts as the power supply for the load. The main disadvantages of this design are the large energy loss on the converter and the need for an off-chip capacitor. Novel ideas to tackle these problems include the proposal to completely remove both the converter and the capacitor in order to power the load using an AC power supply directly from the rectifier [3].

Power supply voltage and internal subsystem voltages can no longer be considered static parameters in a system. For this reason, constant monitoring of the operating conditions must be performed in order to allow for an optimal decision making process. In most cases, monitoring can be efficiently implemented using voltage sensors. The detection of a specific voltage level and the generation of a signal for the communication of that event is called voltage sensing. Voltage sensing can mainly take two different forms according to the desired functionality. On the one hand, if a single voltage level needs to be detected, the voltage sensor will output a single activation signal as the specific voltage threshold crossing takes place in either direction. On the other hand, if a node voltage needs to be constantly monitored, the voltage sensor will output a monotonic digital code corresponding to the entire monitoring voltage interval.

Voltage sensing is a necessary process in a wide range of applications. Naturally, this leads to the development of many different designs in order to meet a diverse set of specifications. One of the most important characteristics of a voltage sensor is the response time which is defined as the interval between the time a specific voltage value registers in the circuit and the time an output signal from the sensor is generated in order to inform another block about that event. In case of a continuous monitoring block using a digital code for each sensed voltage level,

the resolution of the sensing plays a crucial role. The resolution can be defined as the voltage interval that corresponds to two successive digital codes and depending on the application it has to fulfil certain criteria. Higher resolution results in a more accurate representation of the voltage levels to be sensed, albeit increased accuracy usually is a trade-off and it negatively affects other specifications. Another important consideration in the design of voltage sensors is the need for a stable voltage reference or lack thereof. Stable references are hard to be obtained in energy harvesting environments and thus reference-free operation is a major advantage. Finally, the generic specifications of power, area and resilience to PVT variations cannot be neglected. Power consumption during operation for continuous monitoring sensors and during stand-by mode for threshold crossing sensors should be kept to the minimum. Also, area is directly related to the complexity of the sensor. The use of analog components such as resistors and capacitors involves a huge area penalty and should be avoided.

2.3.2 Voltage sensors

The main term in the literature used to describe voltage sensors detecting a specific voltage threshold crossing is Power-on-Reset (POR). POR can be either used as an independent monitoring solution in energy harvesting systems in order to notify the rest of the circuit about supply voltage fluctuations or as a component of a system wakeup circuit which is used during the power-on procedure in high performance applications in order to provide predictability in the initial conditions for the system.

In [51] a POR design (Figure 19.D) for reliable power-on operation consisting of only three transistors and two capacitors is proposed. The input to the circuit is the rising power supply with a wide range of final values and the output is a pulse of a desired width after a programmable delay dt . Moreover, many delay elements can be cascaded in order to produce a longer delay which may be useful in some applications. Although the main consideration behind this design is not to monitor specific voltage levels but rather to generate a delayed pulse following the supply voltage during ramp-up, the low power consumption, the relatively low layout footprint and the wide operating range make it a viable solution for a wide range of applications.

The divergence of the two nodes in a cross-coupled pair of inverters from the metastable point to the two stable EP in the state space during power-up is caused by the various noise sources in the actual circuit. This phenomenon is used in [48] for the generation of a signal notifying the rest of the circuit that a certain voltage level was crossed. The nodes of the cross-coupled pair are connected to an XOR gate and when the voltage difference between them is more than a certain value, the XOR registers that event and produces a high output (Figure 19.A). The capac-

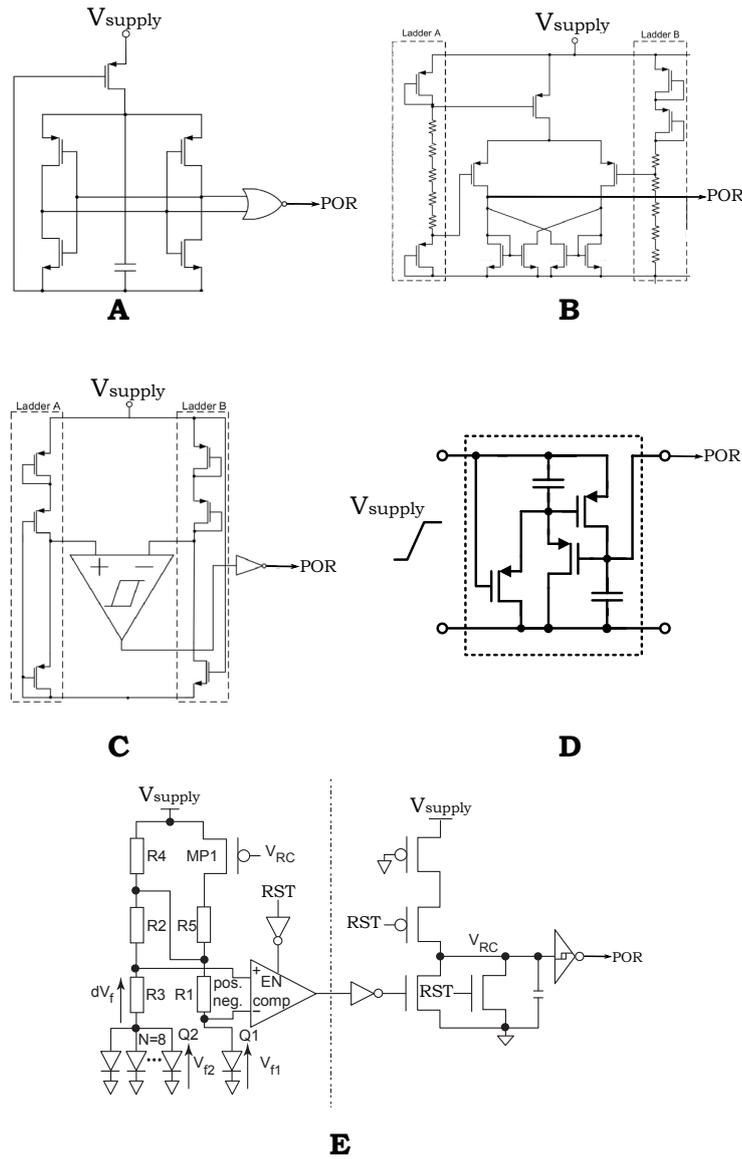


Figure 19: Five designs of POR circuits (A in [48], B in [49], C in [50], D in [51] and E in [52]).

itor connected to the source of the pMOS transistors allows for some programmability in the delay between detection of a certain supply voltage and the generation of the XOR output. Despite the simple design, the predictability of the operation due to PVT variations cannot be guaranteed, so this design is not appropriate for medium to high precision voltage detection.

A design termed Mode Selector and a modified version with upgraded characteristics is presented by the authors in [49] and [50]. The initial version (Figure 19.B) consists of two resistor ladders that control the rising and the falling detection levels. When a rising power supply crosses a certain threshold V_{ris} , the POR signal is enabled and it remains enabled until a lower threshold V_{fal} is crossed in the opposite direction. In the modified version of Figure 19.C, the resistors are replaced by active loads which results in an improvement in the power consumption. Al-

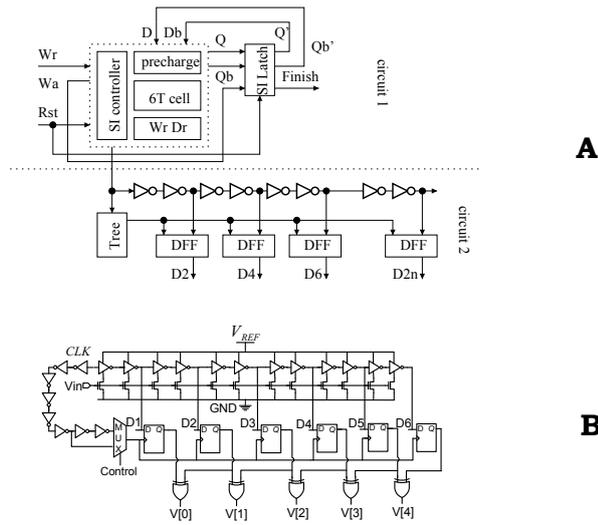


Figure 20: Voltage sensors with digital code generation (A in [53] and B in [54]).

though this circuit can perform well in an energy harvesting environment for coarse detection of relatively high voltage levels, accurately setting V_{ris} and V_{fal} is inherently limited in smaller technology nodes with lower supply voltages.

Figure 19.E shows another double-sided (detection of both rising and falling supply voltage) POR design which is a part of a system wakeup circuit in [52]. A simple bandgap reference structure is used to minimise the effects of process and temperature variations and by connecting it to a feedback loop with the V_{RC} signal, a falling power supply can also be detected. The POR output signal can be generated for a wide range (1.1V-2V) of input voltages but the complexity of the design and the use of analog devices significantly increase both the active layout area and the power consumption, thus restricting the use of this POR only to specific applications.

Accurate voltage monitoring can be easily achieved with an A2D converter which can translate a continuous voltage level to a discrete value represented by a binary vector. Unfortunately, this solution is highly intrusive and it cannot be used as the basis for an on chip monitoring solution. It has many major disadvantages such as the need for a stable voltage reference, large layout area and increased power consumption, and it is not an appropriate solution for most applications.

An alternative solution targeting mainly energy harvesting systems is presented in [53]. The main idea of the proposed design (Figure 20.A) is the generation of a digital code for each sensed voltage level by using the difference in the latency of two circuits powered by the same power supply. A speed independent SRAM, whose read or write operation completion time depends on the power supply is used as circuit 1. Circuit 2 is a simple chain of inverters with registers connected to every second

node of the chain. The measurement begins with an input signal which starts a read or write operation on the SRAM cell. At the same time the value of the initial inverter is flipped. When the SRAM operation finishes, the output of the flip-flops is read to determine how many inverters changed state. The number of inverters tracks the power supply and the digital code generated corresponds to a specific voltage level. Simulations showed the viability of the method for supply voltages as low as 0.2V in a 90nm technology node but further studies that take into account process and temperature variations are yet to be conducted.

An ultra low voltage sensor with resilience to process and temperature variations is presented in [54]. The circuit (Figure 20.B) consists of a series of current starved inverters and flip-flops connected to every second inverter of the chain. A reference voltage of 0.5V powers the design and the variable voltage level to be sensed is provided as an input to the pull-down section of each inverter. A digital code is generated for each input voltage between 0.3V and 0.5V. The resolution of the sensor is around 50mV.

STABILITY ANALYSIS OF PERIODIC ORBITS IN CMOS CIRCUITS

3.1 INTRODUCTION

Periodic solutions are a common phenomenon in CMOS circuits blocks. They can be observed in a wide range of circuit classes such as amplifiers, mixers, filters and N-stage inverter oscillators. Oscillating circuits can be either autonomous or driven depending on the presence of a time-varying external stimulus.

One of the most important characteristics of a periodic orbit is its stability properties. The basic idea behind stability is that after a small perturbation, the solution converges back to the orbit. This perturbation from the initial orbit can be a result of parameter variation that may happen in real time during circuit operation (e.g. power supply fluctuation).

The stability of periodic solutions in CMOS circuits and dynamical systems in general is of major importance and failure to account for it prior to fabrication may lead to system malfunction. We often come across the term *loss of stability*. A loss of stability is directly related to a bifurcation. It can be clearly deduced by the presentation of basic bifurcation phenomena in Chapter 2 that bifurcations are responsible for significant qualitative changes that lead to irregular behaviours in a circuit. A common example is the "pulse swallowing" of the frequency divider in a PLL block [1]. Proper characterization of the stability and the stability margin of an orbit (the maximum allowable parameter variation that does not alter the stability properties) is crucial.

In this chapter, we develop an algorithm for the stability analysis of periodic orbits in CMOS circuits based on fundamental mathematical principles of dynamical systems. A transistor is regarded as a voltage controlled current source described by a quadratic short channel piecewise model (Section 3.2.1). A non-smooth ODE model is constructed by applying KCL on the circuit and the stability properties are extracted based on the Floquet theory. Because of the discontinuity of the model, the Floquet method is complemented by the Filippov method which guarantees the soundness of the results. The algorithm is implemented using exclusively Matlab scripts. Additionally, the proposed method is verified on an autonomous three-stage ring oscillator and an example of bifurcation detection due to stability loss that demonstrates the value of the method is presented for a high speed toggle element. The trade-off between accuracy and complexity, the straightforward implementation and the soundness of the final results are the main advantages of the pro-

posed approach on the qualitative analysis of circuit oscillating behaviour.

The PSS response of a circuit can be directly computed in commercial simulators by either the Harmonic Balance in the frequency domain or the Shooting method in the time domain [66]. The stability properties of a circuit can be computed as a by-product of the PSS analysis. Selting et al [67] use the provisional results of Harmonic Balance to calculate the Monodromy matrix and then the Floquet multipliers that determine the stability. In a similar approach [68], using results from the Harmonic Balance analysis, a pure frequency domain tool for the computation of the local stability of periodic solutions based on Floquet Theory and Fourier series expansion is developed. Both of these methods yield satisfactory results but their main drawback is the complexity of the implementation. Obtaining intermediate simulation results during PSS analysis requires access and modification of the internal algorithms of the simulator. In case of state of the art commercial simulators, under the hood access is not possible. Additionally, as loss of stability through bifurcation is a qualitative phenomenon, the accuracy of the above methods adds limited value to the extracted results. The same qualitative results can be acquired by using a simple transistor model and the mathematically sound and easily implemented method presented in this chapter.

The remainder of the chapter is structured as follows. In Section 3.2 the basic short channel transistor model along with a generic method for the construction of an ODE model for any CMOS circuit is presented. Sections 3.3 and 3.4 introduce the fundamental mathematical tools used for the stability analysis algorithm, namely the Floquet theory and the Filippov method. The Matlab implementation of the stability algorithm is described in 3.5. Finally, 3.6 concludes the chapter with the application of the algorithm to a three-stage ring oscillator and a toggle element with variable input frequency.

3.2 CIRCUIT DESCRIPTION

3.2.1 *Transistor model*

The fundamental building block of CMOS integrated circuits is the transistor. In most semiconductor manufacturing processes two types of transistors are mainly used: the pMOS and the nMOS. Both types have four terminals, namely the gate G, the source S, the drain D and the bulk B. The symbol used in the schematic representation of circuits is shown in Figure 21. In reality, transistors are symmetrical devices and the identification of the source and the drain can be done only after the terminal voltage levels are known. The applied gate voltage controls the width of the conducting channel and thus the current flowing through the device.

The development of mathematical models for the simulation of the actual transistor behaviour is a fundamental prerequisite for the design of integrated circuits. The state of the art model used by the vast majority of commercial simulators is the BSIM4 model [69]. It is a high accuracy complex model based on a set of equations describing physical properties, process information, temperature effects and several other physical properties. For the complete characterization of the actual operation of CMOS devices, a set of a few hundred user-defined parameters is included in the BSIM4 model. However, the higher degree of complexity leading to greater accuracy is accompanied by more complicated algorithms and time-consuming simulations.

The transistor model selected for the work presented in this chapter is an updated version of the classic quadratic model for long channel devices. The initial version has been the industry's standard for hand calculations for many years. The enhancements introduced take into account the velocity saturation effects that are prominent in deep submicron devices. Using this model, the transistor can be considered a voltage controlled current source with three operating regions: cutoff, linear and saturation. The subthreshold conduction mode could also be included but it is omitted for simplicity. The drain to source current I_{DS} is a piecewise function of the terminal voltages. It should be noted that this model does not take into account the bulk (B) pin of the devices. Although trivial and with a small number of parameters, this model captures the actual characteristics of the real device with good precision. A comparison with the BSIM4 model is shown in Figure 22. The equations of the drain to source current I_{DS} for the three operating regions are the following:

Cutoff region

$$I_{\text{cutoff}} = 0$$

, if $V_{GS} - V_T < 0$

Linear region

$$I_{\text{linear}} = \frac{W}{L} \cdot \frac{\mu_e \cdot C_{\text{ox}}}{1 + \frac{V_{DS}}{E_c \cdot L}} \cdot \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) \cdot V_{DS}$$

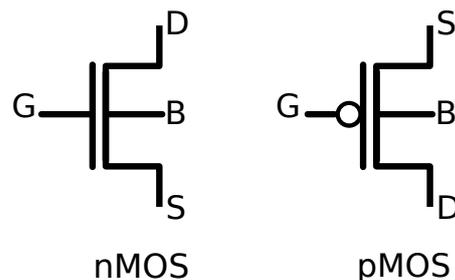


Figure 21: nMOS and pMOS transistor symbols.

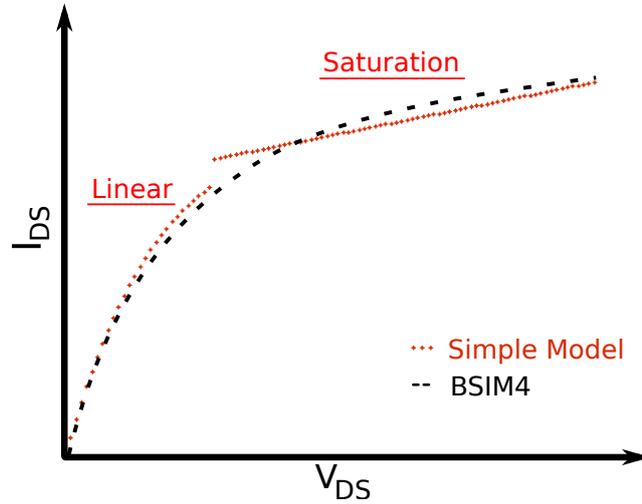


Figure 22: Comparison between BSIM4 and short channel model.

, if $V_{GS} - V_T > 0$ and $V_{SAT} > V_{DS}$

Saturation region

$$I_{\text{saturation}} = v_{\text{sat}} \cdot C_{\text{ox}} \cdot W \cdot \frac{(V_{GS} - V_T)^2}{(V_{GS} - V_T) + E_c \cdot L} \cdot (1 + \lambda \cdot V_{DS})$$

, if $V_{GS} - V_T > 0$ and $V_{SAT} < V_{DS}$

where

- W transistor width
- L transistor length
- v_{sat} saturation velocity
- μ_e carrier mobility
- C_{ox} gate oxide capacitance
- E_c magnitude of the vertical field
- λ channel length modulation effect
- V_T threshold voltage
- V_{GS} voltage difference between gate G and source S
- V_{DS} voltage difference between drain D and source S

Additionally, V_{SAT} is the saturation voltage defined as:

$$V_{SAT} = \frac{(V_{GS} - V_T) \cdot E_c \cdot L}{(V_{GS} - V_T) + E_c \cdot L}$$

The equations presented above are valid only for nMOS transistors. For pMOS transistors the source to drain current I_{SD} can be found by substituting V_{GS} with V_{SG} , V_{DS} with V_{SD} and the negative pMOS threshold voltage V_T^p with $|V_T^p|$.

3.2.2 ODE circuit model

The circuit analysis using a dynamical systems approach requires the formulation of a representative ODE circuit model. All the circuits discussed in this thesis consist exclusively of a set of nMOS and pMOS transistors and as a result, the modelling will be focused on capturing the dynamics of this specific circuit class. However, additional elements such as resistors and capacitors can be easily included in the model.

The basic tool for the construction of an ODE system for the circuit is KCL. KCL states that the algebraic sum I of all the currents entering a node is equal to zero for every time instance t . The node voltages serve as the state variables for the ODE system and their introduction to the equations is achieved by assuming a constant capacitance from every internal node to the ground. The fundamental equation $I = C \cdot \dot{V}$ describing the current flowing through the capacitor transforms the KCL equations into a system of ODE. Additionally, a separation between internal nodes and input nodes is assumed. Power supply, ground and external time dependent signals compose the set of the input nodes.

Several assumptions were made in order to keep ODE circuit model simple. First, each nodal capacitor represents the parasitic capacitance effects introduced by the transistors. In reality, the value of the capacitance is variable and depends on the transistor terminal voltage levels. Second, each capacitor is assumed to connect each node of the circuit to the ground. The actual parasitic capacitance profile of the circuits is more complicated and includes direct connections between the circuit nodes. Finally, the current flowing into the gate of the transistors is considered negligible and is not taken into account in the calculations.

Putting the pieces together, let the voltages of the internal nodes of a circuit be the state variables and the components of a vector V . Applying KCL and substituting the transistor currents using the model described in 3.2.1, the ODE model of the circuit is $\dot{V} = f(V(t))$. In case of time dependent external inputs, the system is non-autonomous and it is modelled by:

$$\dot{V} = f(V(t), t) \quad (1)$$

This expression can be written :

$$\dot{V} = C^{-1} \cdot M \cdot I_{DS}(V(t), t) \quad (2)$$

where

- C diagonal matrix of the internal node capacitances to the ground
- M matrix of elements with values 0, 1, -1 depending on the contribution of each transistor to KCL on each node
- I_{DS} vector with the transistor currents

If a circuit has N internal nodes and TR transistors, $V \in \mathbb{R}^N$, $C \in \mathbb{R}^{N \times N}$, $M \in \mathbb{R}^{N \times TR}$ and $I_{DS} \in \mathbb{R}^{TR}$.

To elucidate the ODE model procedure, the bistable element of Figure 23 is considered. Capacitances C_1 and C_2 represent the lumped parasitic capacitance of each node. KCL is applied to both nodes of the circuit giving the following two equations:

$$\begin{aligned} I_1 + C_1 \cdot \dot{V}_1 &= I_2 \\ I_3 + C_2 \cdot \dot{V}_2 &= I_4 \end{aligned}$$

Rearranging yields :

$$\begin{bmatrix} \dot{V}_1 \\ \dot{V}_2 \end{bmatrix} = \begin{bmatrix} C_1 & 0 \\ 0 & C_2 \end{bmatrix}^{-1} \cdot \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \end{bmatrix} \cdot \begin{bmatrix} I_1(V_1, V_2) \\ I_2(V_1, V_2) \\ I_3(V_1, V_2) \\ I_4(V_1, V_2) \end{bmatrix}$$

The modelling of the current I_{DS} as a piecewise function is important from a dynamical systems perspective. The ODE model of the circuit will be non-smooth with the state space divided into $3T$ different regions. These regions will be separated by $(3T - 1)$ hypersurfaces called switching manifolds.

3.3 FLOQUET THEORY

Floquet theory provides the mathematical basis for the stability analysis of a system. The basic characteristic of this method is the direct observation of the evolution of a perturbation along a periodic solution. This is achieved by the linearisation of the periodic orbit using Taylor series expansion. Assume that a non-linear smooth dynamical system

$$\dot{x}(t) = f(x(t), t) \tag{3}$$

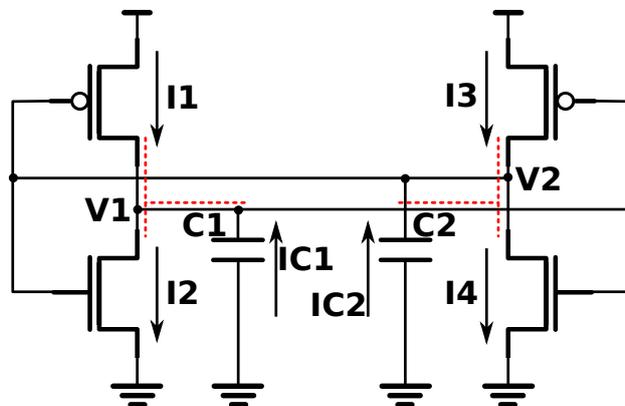


Figure 23: KCL in bistable element.

with $x \in \mathbb{R}^N$ exhibits periodic behaviour. Let the periodic solution be $x_P(t)$ and the period T . At time t_0 , the IC $x_P(t_0)$ is perturbed to $x_{PP}(t_0)$. The initial perturbation is expressed as $y(t_0) = x_{PP}(t_0) - x_P(t_0)$ and the time dependent perturbation as $y(t) = x_{PP}(t) - x_P(t)$. A graphical representation can be found in Figure 24.

Thus, the perturbed trajectory is:

$$x_{PP}(t) = x_P(t) + y(t) \tag{4}$$

Replacing in Equation 3:

$$\dot{x}_P(t) + \dot{y}(t) = f(t, x_{PP}(t)) \tag{5}$$

Expanding $f(t, x_{PP}(t))$ about the time dependent unperturbed periodic solution using Taylor series and discarding higher order terms yields:

$$f(t, x_{PP}(t)) = f(t, x_P(t)) + \left. \frac{\partial f(t, x_{PP}(t))}{\partial x_{PP}(t)} \right|_{x_P} \cdot (x_{PP}(t) - x_P(t)) \tag{6}$$

Replacing Equation 4 to Equation 6, Equation 6 to Equation 5, using Equation 3 and rearranging yields:

$$\dot{y}(t) = \left. \frac{\partial f(t, x_{PP}(t))}{\partial x_{PP}(t)} \right|_{x_P} \cdot y(t) \tag{7}$$

The matrix $Jac(t, x_P(t)) = \left. \frac{\partial f(t, x_{PP}(t))}{\partial x_{PP}(t)} \right|_{x_P}$ is the Jacobian matrix of the system around the periodic orbit that plays an important role in the description of the effect of the initial perturbation on the system. Due to the time varying nature of the $Jac(t, x_P(t))$, it is not generally possible to construct a closed-form expression which can be used to determine stability. Equation 7 corresponds

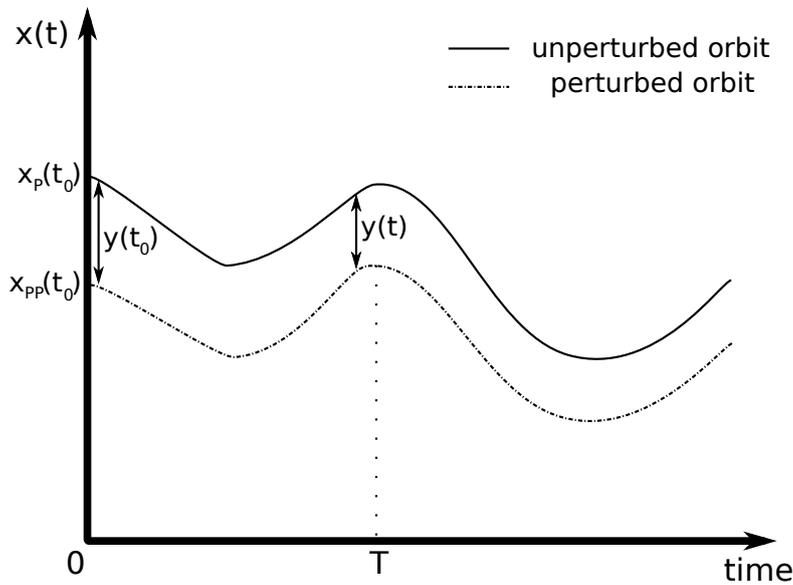


Figure 24: Example of parallel evolution over time of an orbit and its perturbed counterpart.

to a linear system with n linearly independent solutions that can be expressed in a matrix form:

$$\Phi(t, t_0, y(t_0)) = [\varphi_1(t, t_0, y(t_0)) \cdots \varphi_n(t, t_0, y(t_0))] \quad (8)$$

The matrix Φ is called fundamental solution matrix (FSM) and obeys Equation 7. Substituting Equation 8 in Equation 7:

$$\frac{d\Phi(t, t_0, y(t_0))}{dt} = \text{Jac}(t, x_p(t)) \cdot \Phi(t, t_0, y(t_0)) \quad (9)$$

Equation 9 is a matrix differential equation and its solution can be calculated numerically. For $t = 0$, $\Phi(0)$ is equal to the identity matrix \mathbf{I} . The matrix $\Phi(T, t_0, y(t_0))$ after time $t = T$ is called Monodromy matrix. The eigenvalues of the Monodromy matrix, called *Floquet multipliers*, determine the stability of the system. If the absolute value of the real parts of the eigenvalues lie inside the unit circle, the perturbation will decay and the system is stable.

In practice, apart from the significance of the Floquet multipliers, the FSM Φ can be used for the calculation of the time dependent perturbation along the periodic orbit between two time instances t_i and t_f :

$$y(t_f) = \Phi(t_f, t_i, y(t_i)) \cdot y(t_i) \quad (10)$$

3.4 FILIPPOV METHOD

The application of Floquet theory for the stability analysis of non-smooth systems needs to be adjusted to account for their special structure. The basic feature of a non-smooth system is the multiple expressions of the vector field for different regions of the state space. This category includes the ODE circuit model described in detail in 3.2.1 because of the piecewise definition of the transistor current.

The major addition to the mathematical formulation of 3.3 is a more detailed treatment of the FSM at the time of vector field change. Let the term *switching* describe the crossing from one region of the state to another. A problem arises because of the non-unique definition of the FSM on each switching hypersurface. Filippov provided a solution to this inconsistency by proposing a matrix S to map $\Phi(t_{p-}, t_0, y(t_0))$ to $\Phi(t_{p+}, t_0, y(t_0))$. The matrix S is called *Saltation matrix* and can be regarded as an FSM from time t_{p-} to t_{p+} :

$$S = \Phi(t_{p+}, t_{p-}) \quad (11)$$

Filippov systems are part of discontinuous dynamical systems which can be described by a set of first order ODEs with a discontinuous right-hand side. Exceptional work on this field has been conducted by Leine [70] who applied the theory on mechanical and electrical systems. It should be noted that non-conventional bifurcations can occur in Filippov systems but in this work the

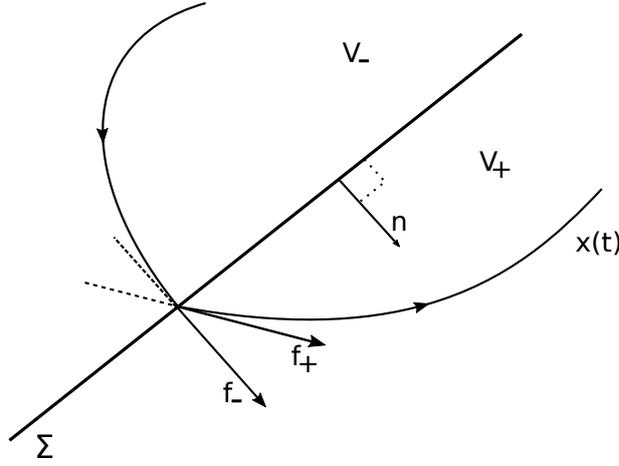


Figure 25: Solution $x(t)$ as the system crosses from region V_- to V_+ through the surface h and switches from vector field f_- to f_+ .

main objective of the application of Filippov method is to present an accurate analysis in a mathematical sense.

Replacing Equation 11 in Equation 10, the Saltation matrix is the connecting element between the time dependent perturbation before and after the switching:

$$y(t_{\Sigma+}) = S \cdot y(t_{\Sigma-}) \quad (12)$$

The strict mathematical derivation of the expression for the Saltation matrix has been calculated in [70]. It is:

$$S = I + \frac{(f_+ - f_-) \cdot n^T}{n^T \cdot f_- + \left. \frac{\partial h}{\partial t} \right|_{t_{\Sigma}}} \quad (13)$$

Consider Figure 25 for a graphical explanation of the terms in Equation 13. Let V_- and V_+ be two regions of the state space separated by the switching surface Σ . $x(t)$ is the periodic solution and f_- , f_+ the vector fields before and after the switching. Additionally, $h(t_{\Sigma}, x(t_{\Sigma}))$ is the algebraic expression for the switching surface Σ and n is the normal to that surface. Finally, I is the identity matrix. Assume a periodic solution $x(t)$ of period T for an ODE system with a distinct vector field for each of its two state space regions $R1$ and $R2$. Also, let $x(t)$ cross the switching surface from $R1$ to $R2$ at time t_{Σ} . Using Floquet theory and accounting for the switching with Filippov's method, the Monodromy matrix can be composed as :

$$\begin{aligned} & \Phi(t_0 + T, t_0, y(t_0)) \\ &= S_2 \cdot \Phi(t_0 + T, t_{\Sigma+}, y(t_{\Sigma+})) \cdot S_1 \cdot \Phi(t_{\Sigma-}, t_0, y(t_0)) \end{aligned} \quad (14)$$

where $t_{\Sigma-}$ and $t_{\Sigma+}$ are the time instances before and after the switching. It is evident from Equation 14 that the composition of

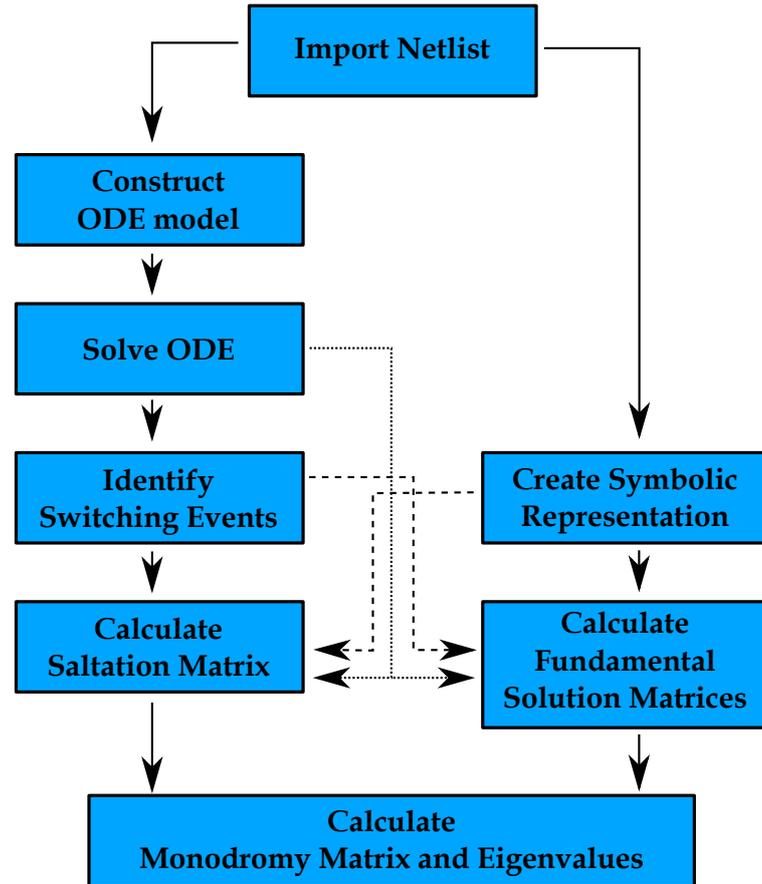


Figure 26: Flow chart of the stability algorithm implementation.

the expression for the Monodromy matrix can be generalized for any number of crossings to different regions of the state space by calculating the Saltation matrices of the switching events.

3.5 IMPLEMENTATION DETAILS

The method for the stability analysis of CMOS circuits was implemented using Matlab scripts. An overview of the different blocks is presented on the flow chart in Figure 26. Initially, a SPICE-like netlist containing information about device parameters, circuit description and simulation details is created. Then, the ODE model of the circuit is constructed. Finally, all time dependent terms and functions of those terms, namely the node voltages, the transistor currents, the saturation voltages and the input signals as defined in Equation 2, are represented by symbolic variables. This representation is advantageous for the calculation of the switching hypersurfaces and the Saltation matrices. In general, using symbolic variables in simulations of large systems is computationally prohibitive but in this work we are mainly interested in circuit blocks comprised of only a few transistors. For this reason, symbolic calculations do not pose a constraint and can be used effectively.

The solution of the ODE circuit model is calculated using numerical simulation and the initial value problem is solved using Matlab. The initial solution of the simulation is any reasonably selected point of the N-dimensional state space. The simulation is run for an arbitrary time and is stopped when periodic behaviour is observed. The solution points of one complete period are then interpolated and all the time instances where switching events occur are identified. The switching hypersurfaces for those events are the algebraic expressions of the current constraint of the transistor responsible for the switching. In some cases, more than one transistors change operating region at the same time. For simplicity, the average algebraic hypersurface is computed on these instances.

For the calculation of the Monodromy matrix the values of the terms of an equation similar to Equation 14 must be computed. The Saltation matrices at the switching instances are found using the symbolic representation of Equation 13 calculated at t_{Σ} . The FSM between two time instances are the solution of the matrix differential equation (MDE) 9. In Matlab, for the solution of the MDE, the values of the Jacobian matrix along the periodic orbit are needed. These are calculated using the interpolated solutions of the circuit ODE model.

3.6 EXPERIMENTS

The validity and the usefulness of the proposed method is demonstrated with a series of simulations on real-life circuits. Firstly, a three-stage ring oscillator is used. The simplicity of the circuit allows for the detailed application of the stability algorithm and the verification of the actual results. Secondly, the more elaborate Yuan and Svensson toggle element is the basis of the next set of experiments. The rich state space characteristics of this circuit under parameter variations is studied and the suitability of the proposed algorithm for the bifurcation analysis of a system is demonstrated.

3.6.1 *Three-stage ring oscillator*

The 3rd order ODE model of the three-stage ring oscillator in Figure 27 is constructed according to 3.2. The capacitors C1, C2 and C3 represent the internal node capacitances of the circuit. Details about the model parameter and capacitance value selection can be found in Appendix A. Bounded by the minimum and maximum values for the node voltages (ground and power supply), a random point of the three-dimensional space is selected as the IC for the simulation and the initial value problem is solved until periodic behaviour of period T is observed. The state space of the oscillator for time T is plotted in Figure 28. The red dots are time instances when the ODE model switches to a different vector field or, to put it simply, the switching events. The ODE

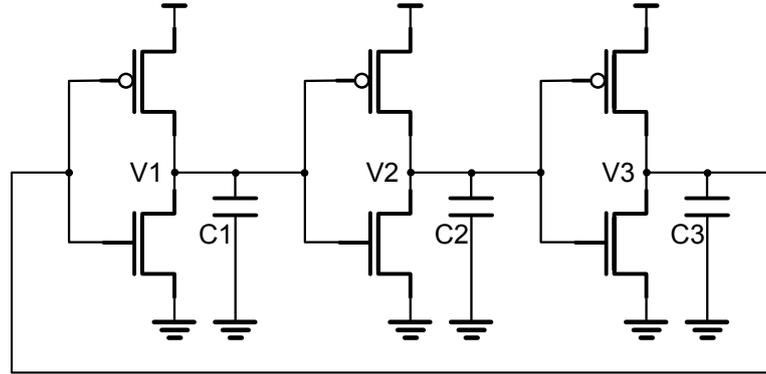


Figure 27: three-stage ring oscillator.

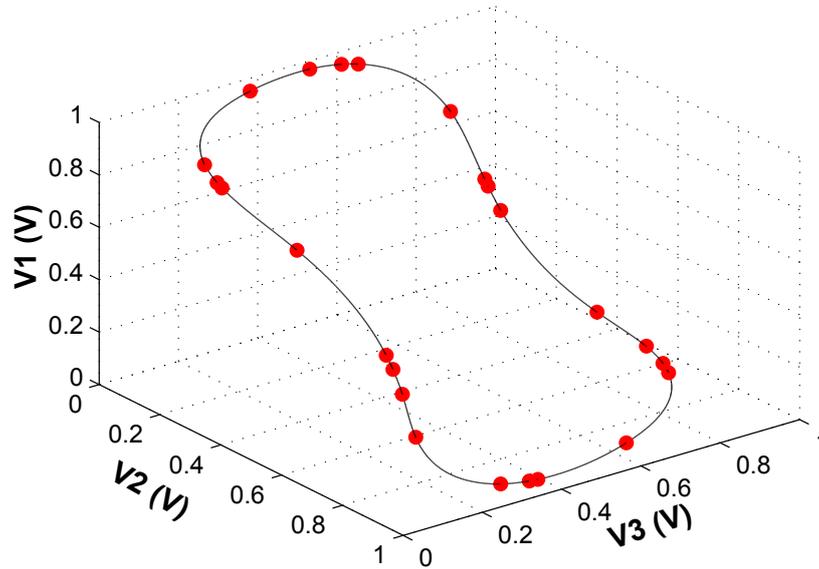


Figure 28: One period of the periodic solution in a three stage ring oscillator plotted in the three-dimensional space with red dots denoting the switching events.

model parameters selected for this simulation result in 23 switching events. Consequently, for the calculation of the Monodromy matrix as in Equation 14, a product of 23 Saltation matrices and 24 FSMs is produced.

The Monodromy matrix for the circuit is:

$$\Phi(T, 0) = \begin{bmatrix} 0.8730 & -0.7758 & -0.1478 \\ -0.1241 & 0.1103 & 0.0210 \\ -0.0802 & 0.0713 & 0.0136 \end{bmatrix}$$

The eigenvalues of $\Phi(T,0)$ are the Floquet multipliers of the system that determine the stability of the orbit. They are equal to:

$$\text{Eig} = \begin{bmatrix} 0.997 \\ 0.000025472 \\ 0.000000009 \end{bmatrix}$$

It is evident that all three eigenvalues lie inside the unit circle. Thus, the periodic orbit is stable, which of course is to be expected. It should also be noted that the largest eigenvalue is particularly close to unity, as the circuit is autonomous and it does not depend on external stimulus. In theory, the value of this eigenvalue should have been exactly 1. The slight discrepancy can be accounted for by the integration and interpolation errors during the linearisation of the periodic orbit.

The accuracy of the linearisation can be checked by using Equation 10. According to it, the time dependent perturbation of the periodic orbit after time T can be calculated, if the initial perturbation and the Monodromy matrix are known. In order to validate the theory, a simulation is run for time T . The IC initC and the final solution FS are:

$$\text{initC} = \begin{bmatrix} 0.517972 \\ 0.980964 \\ 0.013295 \end{bmatrix}, \text{FS} = \begin{bmatrix} 0.515107 \\ 0.981379 \\ 0.013554 \end{bmatrix}$$

A graphical representation of this analysis for the three node voltages of the circuit is given in Figure 29. Following the initial simulation (black plots in Figure 29), a perturbation vector PV is added to the initC . PV is equal to:

$$\text{PV} = \begin{bmatrix} 0.015 \\ 0.015 \\ 0.015 \end{bmatrix} \text{ Volts}$$

A second simulation is run from the new IC $\text{initC}_{\text{new}}$ and the new final solution newFS is found (red plots in Figure 29):

$$\text{initC}_{\text{new}} = \begin{bmatrix} 0.532972 \\ 0.995964 \\ 0.028295 \end{bmatrix}, \text{newFS} = \begin{bmatrix} 0.514681 \\ 0.981439 \\ 0.013594 \end{bmatrix}$$

Thus, the actual perturbation AP of the solution after time T is:

$$\text{AP} = \begin{bmatrix} -0.000426 \\ 0.000059 \\ 0.000040 \end{bmatrix}$$

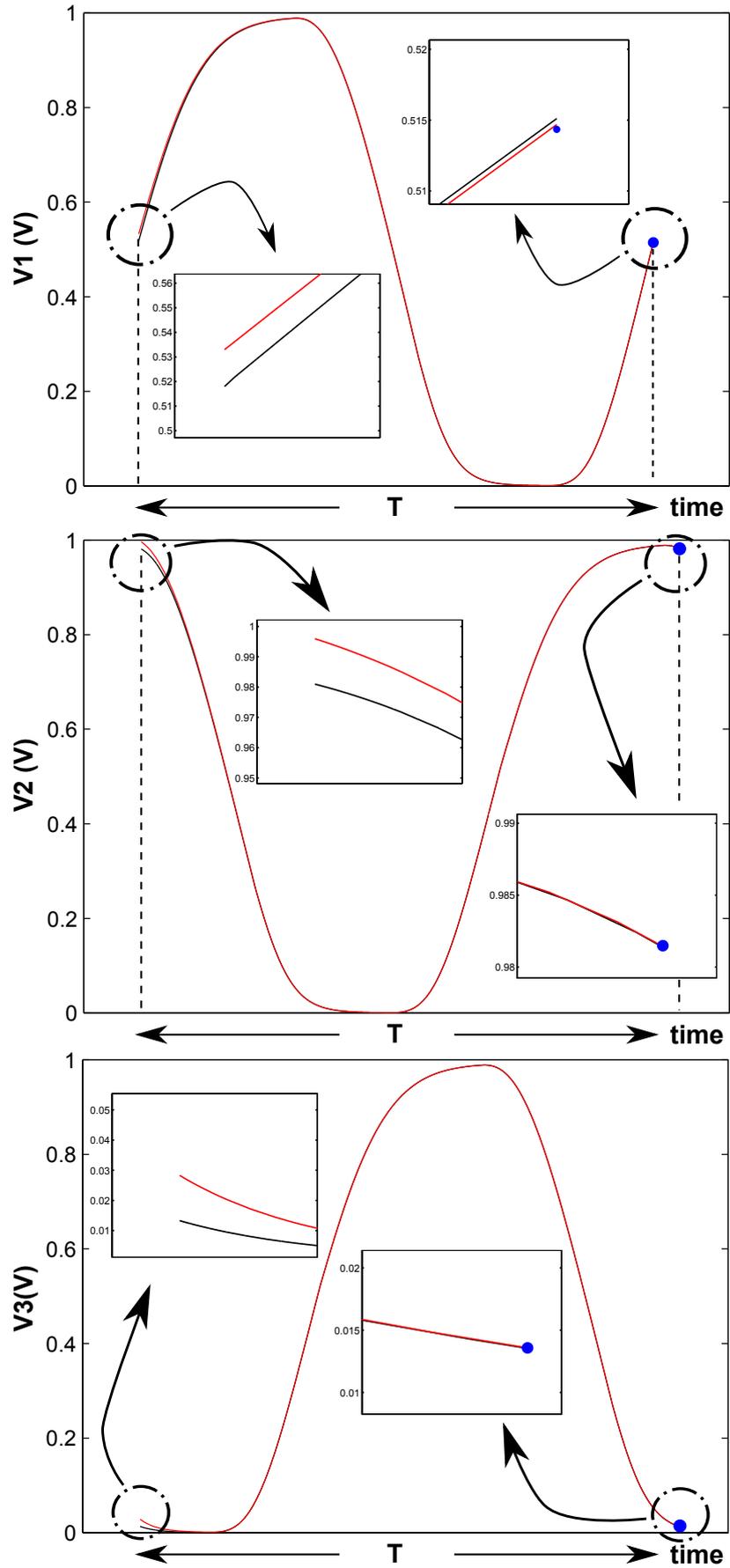


Figure 29: Detailed plots of node voltages over time for perturbed and unperturbed solutions. Blue dots are the solutions predicted using the Monodromy matrix.

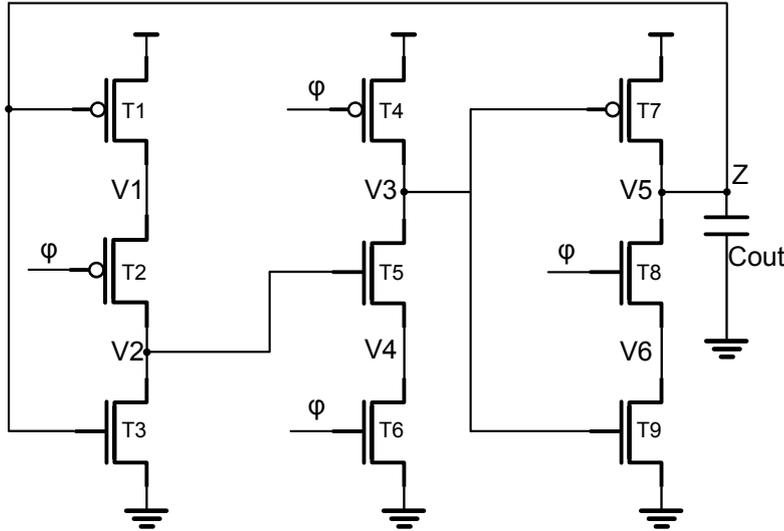


Figure 30: Yuan and Svensson toggle element.

The expected perturbation EP (blue dots at time T in Figure 29) according to Equation 10, given that $\Phi(t_f, t_i, y(t_i)) = \Phi(T, 0)$ and $y(t_i) = PV$, is:

$$EP = \Phi(T, 0) \cdot PV = \begin{bmatrix} -0.000760 \\ 0.000108 \\ 0.000070 \end{bmatrix}$$

These results are in a very good agreement and thus the predictive potential of the Monodromy matrix is validated.

3.6.2 Yuan and Svensson toggle element with variable input frequency

The toggle element in Figure 30 was initially developed by Yuan and Svensson as a latching component of their True Single Phase Clocking (TSPC) circuit techniques [71]. The basic characteristics of the proposed novel latches were both the potential for a dramatic increase of the clock frequency and the reduction of the skewing problems in a circuit. Because of their speed, in recent years TSPC latches are the preferred choice for the design of prescalers in PLLs [72].

In the configuration in Figure 30, the output Z is fed directly back to the input of the latch, thus creating a frequency divider. C_{out} is the input capacitance of the subsequent circuit block. The input signal ϕ is a sinusoidal signal of frequency f and the output Z is a signal of half the input frequency. In more detail, when the input makes a low to high transition, the output must go either from high to low or from low to high. When the input makes a high to low transition the output z remains unchanged. Therefore, the value of the output changes every other change of the input (period-2 specification).

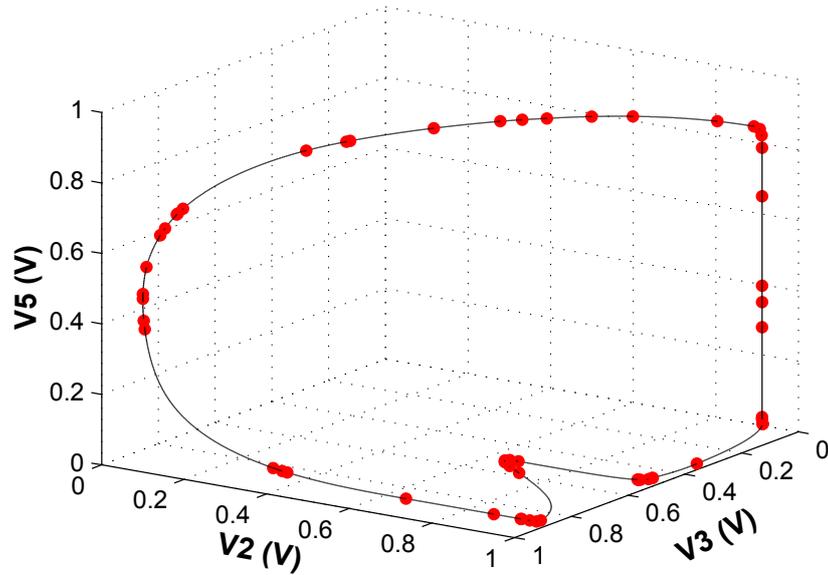


Figure 31: One period of the periodic solution in a toggle element plotted in the three-dimensional space with red dots denoting the switching events.

The toggle belongs to the class of non-autonomous (driven) circuits. Increasing the frequency of the input signal ϕ can lead to a violation of the period-2 specification of the circuit. In an older study [21], Greenstreet and Cahoon showed that the operation of the circuit is capped by an upper input frequency limit, further of which the output Z shows a period-3 behaviour. The results presented in this analysis update these findings and show that the violation of this upper threshold leads to a period-4 behaviour, meaning that the period of the output Z is one quarter that of the input. The difference in the findings is a result of the updated transistor models for short channel devices. We use the method presented in this chapter to trace the stability properties of the circuit as the input frequency approaches this upper limit.

A solution in the three-dimensional state space comprised of the node voltages $V2, V3$ and $V5$ is presented in Figure 31. The output of the circuit for a sinusoidal input of frequency $f = 12\text{GHz}$ ($\phi = 0.5 \cdot \sin(2 \cdot \pi \cdot f)$) is plotted. The exact values for the model parameters for this experiment can be found in Appendix A.

The red dots in Figure 31 represent the switching events occurring in the system. A number of 56 switchings can be spotted for the specific simulation. According to Equation 14, the Monodromy matrix of the system will be a product of 56 Saltation matrices and 57 FSMs:

$$\Phi(T, 0) = \Phi_{57} \cdot S_{56} \cdot \Phi_{56} \cdots S_2 \cdot \Phi_2 \cdot S_1 \cdot \Phi_1$$

An evaluation of the application of Equation 10 is given in Figure 32. All the node voltages of the circuit for time T are plotted in black. A perturbation of 20mV is added on top of each IC and the resulting solution is plotted in red. The blue dots at

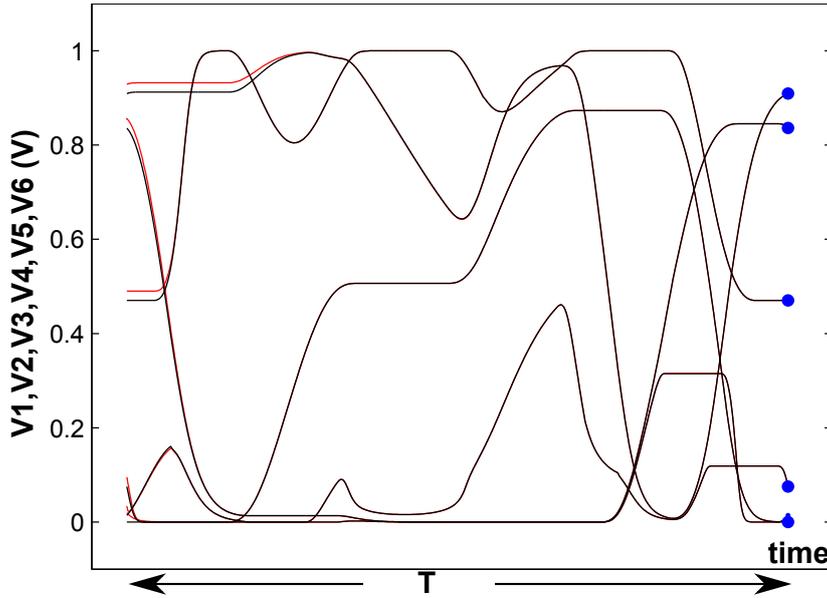


Figure 32: Plot of the node voltages over time for perturbed and unperturbed solutions. Blue dots are the predicted final condition using the Monodromy matrix.

time T are the predicted final solutions based on the use of the Monodromy matrix. Despite the higher complexity of the circuit in comparison to the three-stage ring oscillator, it can be seen that the solutions are in very good agreement.

Following the initial analysis for a fixed input frequency of 12GHz, a series of simulations were performed by varying the input frequency f until the period-2 specification of the circuit is violated. Figure 33 presents the the solution of the ODE model for time T and input frequencies from 12GHz to 13.911GHz. The dashed arrows point at the direction of an increasing frequency f . From a circuit perspective, the contraction of the attractor observed in Figure 33 denotes the increasing difficulty of the design to respond within the decreasing time available according to the specifications.

The Monodromy matrix for the circuit operating under an input frequency of 13.911GHz is:

$$\Phi(T,0) = \begin{bmatrix} -1.6e-04 & -7.3e-03 & 2.2e-04 & 2.1e-05 & 9.7e-06 & 3.0e-07 \\ -1.9e-02 & -8.8e-01 & 2.9e-02 & 2.8e-03 & 1.1e-03 & 3.5e-05 \\ 2.9e-03 & 1.2e-01 & -4.3e-03 & -4.2e-04 & -1.6e-04 & -5.2e-06 \\ -1.3e-02 & -6.0e-01 & 2.0e-02 & 1.9e-03 & 7.8e-04 & 2.4e-05 \\ 3.9e-04 & 1.7e-02 & -3.1e-04 & -3.0e-05 & -2.6e-05 & -8.6e-07 \\ 4.5e-05 & 2.0e-03 & -2.8e-05 & -2.7e-06 & -3.1e-06 & -1.0e-07 \end{bmatrix}$$

The corresponding eigenvalues of $\Phi(T,0)$ are equal to:

$$\text{Eig} = \begin{bmatrix} -8.8667e-01 \\ -7.0644e-05 \\ 2.5030e-07 \\ -3.9594e-19 \\ 2.8001e-18 \\ 3.5591e-22 \end{bmatrix}$$

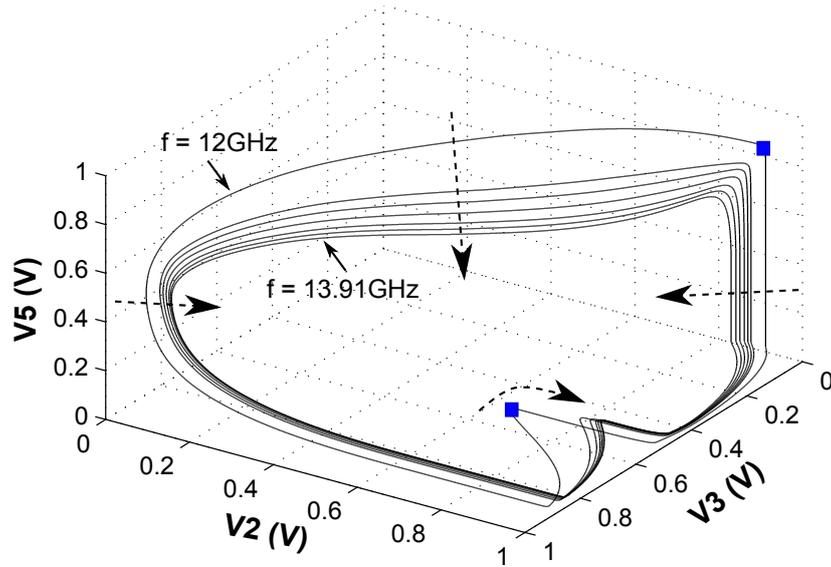


Figure 33: Contraction of the period-2 limit cycle as the input frequency is increased from 12GHz to 13.91GHz. Two successive blue dots denote time equal to T .

As the input frequency f is increased further, a period doubling bifurcation occurs. Figure 34 shows the behaviour of the circuit for a frequency $f = 14\text{GHz}$. A period-4 output is observed and the circuit fails to perform according to the initial specification. By applying the stability analysis method presented in this chapter at each periodic orbit as the frequency is increased, a clear mathematical explanation of the behaviour of the circuit can be obtained. Figure 35 traces the Floquet multipliers of the Monodromy matrix of the system for different frequencies. Only the three largest by absolute value eigenvalues are presented. The value of rest is less than 10^{-9} and they do not offer any insights for the analysis. As the input frequency is increased from 12GHz to 13.911GHz, the value of one of the eigenvalues (red dots in Figure 35) increases until it approaches the unit cycle on the negative real axis and this signals the forthcoming period doubling bifurcation in the system.

3.7 SUMMARY AND CONCLUSIONS

Parameter variations in a circuit displaying oscillating modes may lead to bifurcations which can undermine the correct operation under the predefined specifications. The structural stability of a periodic orbit can be checked by calculating the Floquet multipliers of a system using tools from dynamical system theory.

In this chapter, a novel method for the exploration of the stability properties of a circuit is presented. A simple piecewise transistor model is used and the fundamental KCL is applied in order to construct an ODE model of the circuit. Floquet theory is applied in order to calculate the Monodromy matrix and the

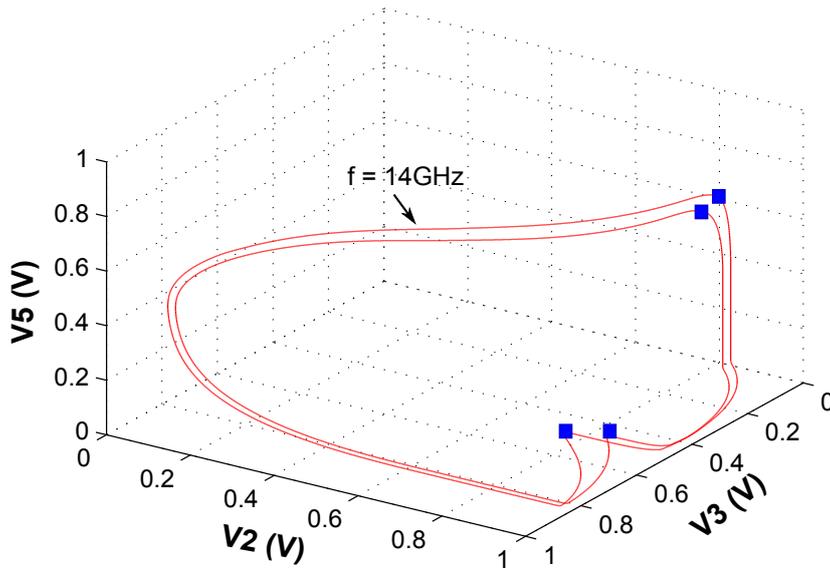


Figure 34: Period-4 limit cycle after bifurcation at 14GHz. Two successive blue dots denote time equal to T .

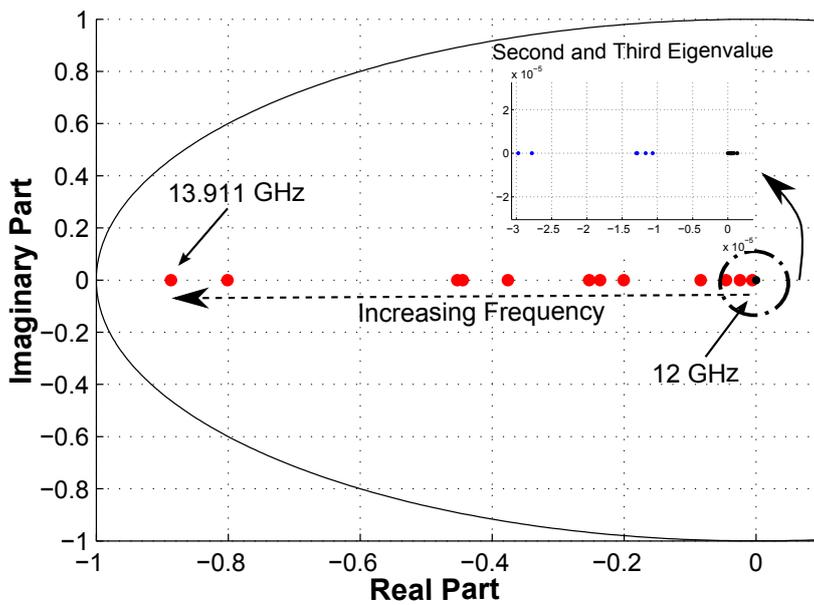


Figure 35: Period-2 eigenvalues progression as the input frequency is increased from 12GHz and approaches the critical value which leads to the bifurcation.

discontinuities of the modelling approach are taken care of by the Filippov method that guarantees the soundness of the results. The qualitative nature of the results expected from this type of analysis allows adequate space for a trade-off between modelling accuracy and implementation complexity. Finally, the proposed algorithm is realised using Matlab scripts.

4

STATE SPACE CHARACTERISATION IN CMOS OSCILLATORS

4.1 INTRODUCTION

Oscillators are critical building blocks in digital and analog systems, as they are indispensable for tasks such as clock generation, frequency synthesis and clock recovery. In general, a ring oscillator consists of a series of cascaded delay elements in a closed loop configuration. The frequency of operation depends on the number of stages and the delay of each stage. This structure is commonly enhanced with additional circuitry that allows the control of certain oscillator properties.

AMS and SOC designs incorporate many different subsystems performing diverse tasks. Similarly, the oscillating elements of these designs are implemented based on a wide range of specifications that guarantee specific operating characteristics. One of the most important features of oscillators is their speed which is defined by the frequency of oscillation. High speed is directly related to a smaller number of delay elements in the ring, which translates to power consumption savings and less area for implementation. Unfortunately, the cost to be paid is the reduced capacity for the generation of multiphase outputs, which are necessary among others in signal processing circuits. Additionally, noise immunity deteriorates and the generated outputs deviate from the ideal periodic behaviour. If the oscillator design allows tuning, a trade-off among the above specifications can be achieved. The detailed control of the trade-off depends on the resolution and the length of the tuning range.

Evidently, there cannot exist an one-size-fits-all oscillator to perform ideally under any of the aforementioned specifications. To effectively answer the miscellaneous questions related to each design problem, a variety of circuit structures can be found in the literature. Most of them originate from the traditional odd-stage inverter ring oscillator but others incorporate highly unconventional structures. Two of these designs can be seen in Figure 36. In A, an even-stage ring oscillator [1] used for the generation of four-phase signals is presented. In B, a variant of A, called Origami oscillator [73], which can achieve better oscillation frequency is shown. Additional designs such as the five-stage negative skewed delay ring oscillator [74] and the multi-feedback ring oscillator based on single ended delay stages [75] offer alternative implementations, which achieve high speed along with multiphase outputs.

The complexity of newly reported oscillator designs along with the reduced ability for the verification of their operation after fab-

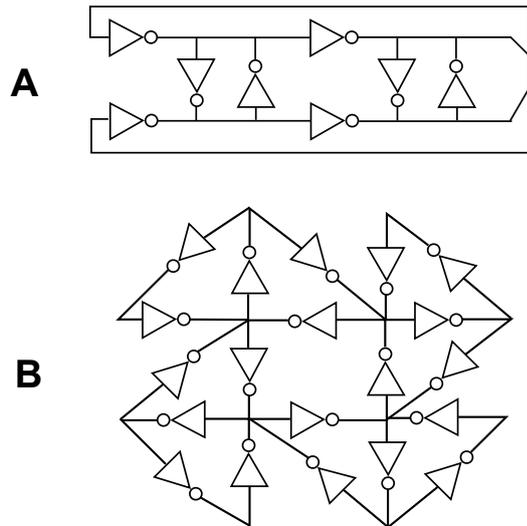


Figure 36: A: Quadrature oscillator. B: Origami oscillator.

rication requires the detailed characterisation during simulation in order to achieve a correct by design circuit. Additionally, the dependence of the oscillator operation on global variable design parameters such as the supply voltage or local properties such as the tuning parameters transforms the verification process to a multidimensional problem.

The structural properties of the state space in a simple odd-stage inverter ring oscillator are well-known. The state space consists of an unstable EP and a limit cycle which attracts the periodic solutions. This basic structure can no longer be considered the norm and traditional PSS simulation alone does not provide a complete verification solution. Unconventional designs such as the quadrature oscillator in Figure 36.A may contain bistable elements that can alter the structure of the state space. Furthermore, considering the parameter variations in the system, it is clear that there is a fertile ground for the appearance of bifurcations which can cause operating failures and other undesired phenomena.

In this chapter, a novel automated flow for the characterisation of the state space in oscillating circuits is presented. Complete verification of an oscillator under parameter variations should include both an exhaustive detection and characterisation in terms of stability of all EP in the state space and a proof of existence or non-existence of periodic orbits. Each of these tasks is performed in a separate modular and automated flow combining existing verification tools with smart application of basic dynamical system theory using any SPICE-like circuit simulator. The verification flow is implemented using the Python programming language. Besides verifying the desired behaviour of an oscillator, the identification of bifurcations with the presented methodology can lead to novel applications for existing circuits. A voltage sensing technique based on this analysis is presented in Chapter

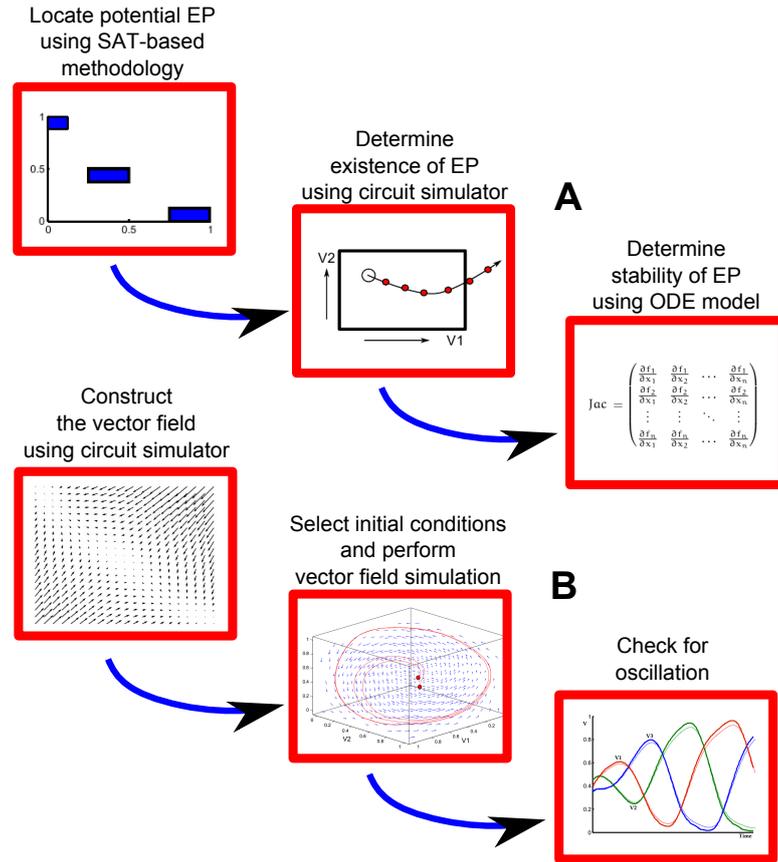


Figure 37: A: Flow for the exhaustive detection and stability characterisation of EP in the state space. B: Flow for the proof of existence or non-existence of limit cycles in the state space.

Figure 37.A graphically presents the steps taken for the state space characterisation in terms of detection and stability of EP in complex circuit blocks with oscillating behaviour. Initially, a SAT-based verification methodology [30] is applied and potential stable and unstable EP are located in the state space. Given the conservative modelling approach in the previous step, a filtering mechanism based on a circuit simulator is provided and all valid EP are identified. In the final step of the analysis, the stability of each EP is determined using basic properties of dynamical systems. The outcome of this analysis is a set of EP in the state space. If all EP are unstable, it can be concluded that an oscillation will be sustained for the current operating conditions. If one or more EP are stable and a periodic orbit exists, then the potentially hazardous situation of *lock-up* can occur in the circuit. In this case, depending on the initial conditions, the circuit may not start oscillating or even start oscillating and eventually settle to a stable EP, thus undermining the desired operation according to the specifications.

Figure 37.B shows the automated flow for determining the existence of periodic orbits in the state space. The first step of the process is the construction of the vector field for the circuit under verification. This is achieved by calculating the derivatives of the

state variables in the state space using a circuit simulator. In the next step, a set of initial conditions is selected and vector field simulations are initiated from different areas in the state space. Finally, the check for periodic behaviour can be performed on the results of the vector field simulation. If every simulation run initiated from different areas of the state space settle to an EP, it can be determined that periodic behaviour does not exist for the given operating conditions.

The remainder of the chapter is structured as follows. In Section 4.2, the three-step flow for the exhaustive detection and characterisation of equilibria in the state space is presented. A brief introduction to Boolean satisfiability paves the way to how the EP detection can be transformed to a SAT-based problem. The proof of existence and the stability properties of the EP using basic dynamical system theory on any circuit simulator are discussed next. Section 4.3 completes the chapter with the presentation of a methodology for the construction of a vector field model of a circuit and with the verification of existence of oscillatory behaviour using vector field simulations.

4.2 EXHAUSTIVE DETECTION AND CHARACTERISATION OF EQUILIBRIA

4.2.1 *Locating potential equilibria using SAT-based methodology*

Boolean satisfiability

Boolean satisfiability is the problem of determining the existence of a variable assignment that yields an evaluation to TRUE in a propositional logic formula $F(X_1, X_2, X_3, X_4, \dots)$. If such an assignment exists, the function F expressed by the formula is satisfiable. Otherwise, when all possible variable assignments yield an evaluation to FALSE, the function F is unsatisfiable. The Boolean expression under evaluation consists of only Boolean variables, operators (AND, OR, NOT) and parentheses. Based on a set of well developed algorithms, SAT solvers are used to tackle the satisfiability problem. The most common representation of a boolean expression in a SAT solver is the conjunctive normal form (CNF). For instance, the formula " $(X_1 \text{ AND } X_2) \text{ AND } (X_3 \text{ OR } X_4)$ " is satisfiable, among other assignments, for $X_1, X_2, X_3 = \text{TRUE}$ and $X_4 = \text{FALSE}$. Recent advances have given existing SAT solvers the capacity to successfully handle problems with millions of clauses and variables. This has been an important factor in their establishment as an invaluable automated analysis tool (Section 2.2).

The addition of background theories to the existing SAT solving techniques has led to the extension of the decision problem from only the binary domain to a generalised space defined by these theories. This space is called SMT and it is a superclass of the traditional boolean SAT theory. Additional theories include equality reasoning, real and integer arithmetic, theory of arrays and lists, and others. In plain words, an SMT solver has

```

;; Definitions
(define X1::real)
(define X2::real)

;; Assertions
;; Section 1 - Set variable intervals
(assert ( and (>= X1 0) (<= X1 10) ) )
(assert ( and (>= X2 5) (<= X2 8) ) )
;; Section 2 - Set expressions
(assert ( = X1 (+ X2 1) ) )

;; Commands
(check)

```

Figure 38: Yices input example.

the ability to prove or disprove the satisfiability of combinations of boolean expressions based not only on boolean variables. For instance, given the expressions $X_1 + X_2 \leq 2$ and $X_1 - X_2 \geq 0$, with $X_1, X_2, X_3, X_4 \in \mathbb{R}$, an SMT solver can provide a variable assignment in \mathbb{R} which satisfies both expressions.

The SAT solving method for the location of potential DC operating points in a circuit is based on Yices [76]. Yices is a powerful SMT solver that decides the satisfiability of arbitrary formulas containing uninterpreted function symbols with equality, linear real and integer arithmetic, scalar types and other theories. In this work, the solver is used for the linear inequalities based on real number arithmetic capability.

Yices is a command line executable with a self-descriptive input language which resembles Scheme and Lisp. The input file template can be conceptually split into three discrete sections: definitions, assertions and commands. Figure 38 shows an example of a simple Yices input file. Initially, all the variables used in the expressions need to be defined in the definitions section of the file. The assertions section can be further divided into two parts. In the first part, minimum and maximum values for the defined variables can be given so that each variable is restricted in a real interval. It is worth noting that the aforementioned step is not necessary in a general Yices input. In the second part, the expressions that need to be checked for satisfiability are listed. An arbitrary number of expressions containing both equalities and inequalities can be set. All assertions in this section are assumed to be connected with AND operators. Finally, the last section contains commands that control the operation and the internal solution process of the solver. In the example presented in Figure 38, two real variables X_1, X_2 are defined on two intervals $X_1 \in [0, 10]$ and $X_2 \in [5, 8]$ and the assertion to be checked is $X_1 = X_2 + 1$. In case of expression satisfiability, Yices constructs

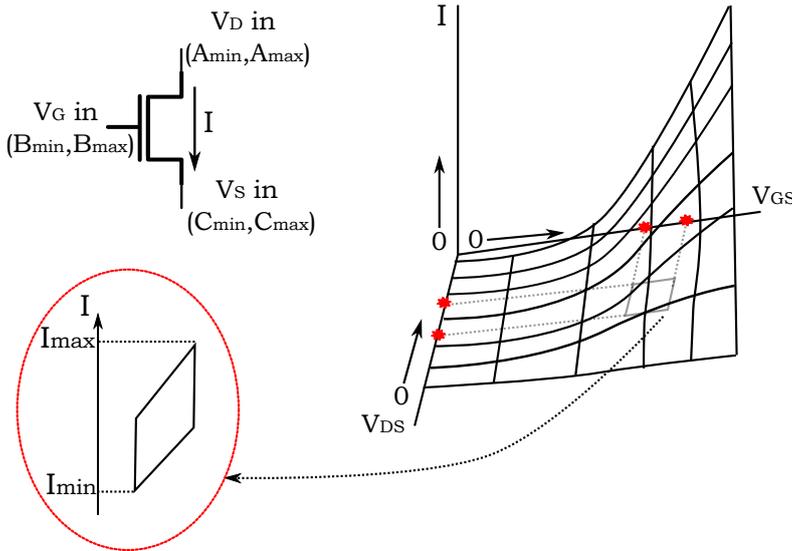


Figure 39: Finding the minimum and the maximum transistor current using the monotonicity property when the transistor pin voltages are represented by real intervals.

evidence by providing a "model" with variable values that satisfy the expression.

Formulation of DC operating point analysis as SAT problem

The formulation of the DC operating point analysis as a SAT problem is based on the basic principles of traditional DC analysis. The relationships among the circuit elements and the fundamental KCL are needed in order to capture the actual behaviour of the circuit. The major difference between the two analyses is the expression of the I-V relationship in nonlinear devices. In the SAT based methodology, this is expressed in terms of real intervals for the voltage and current variables instead of single real values. The representation is beneficial as it allows "multiple simulations" on a single run.

Each circuit state variable in Yices is represented by a set of real intervals. The minimum and maximum values for all variables can be selected in a straightforward way based on the physical constraints of the circuit operation. For instance, a node voltage can initially take any value in an interval $I = [0, V_{DD}]$ between the ground and the power supply. Depending on the solution stage, all the possible values of a state variable may be represented by more than one interval e.g. $V_x \in [0.25, 0.3]$ or $V_x \in [0.55, 0.6]$. In order to account for unexpected phenomena and to keep the conservative nature of the results, the upper and lower limit can be expanded to $I = (0 - \Delta V, V_{DD} + \Delta V)$ without compromising the correctness of the analysis.

The I-V relationship of a transistor using real intervals can be implemented in Yices (and other SAT solvers) using the implication " \Rightarrow " operator. Consider the isolated transistor of Fig-

ure 39 and assume that pin voltages are connected to nodes with values in the following intervals: $I_A = [A_{\min}, A_{\max}]$, $I_B = [B_{\min}, B_{\max}]$, $I_C = [C_{\min}, C_{\max}]$. An expression connecting the pin voltages and the current flowing through the transistor based on the interval representation must be constructed. For this reason, it is noted that in current CMOS technologies, physical properties of the devices force the current to be positive monotonic in V_{GS} and V_{DS} . This means that the minimum and maximum possible values of the transistor current lie on the corners of the surface generated by the intersection of the current surface and the rectangular prism defined by the voltage intervals extended in the positive current direction. Given the above modelling approach, the nonlinearities of the I-V relationship in a transistor can be captured by a set of equations of the form:

$$(V_1 < V_{GS} < V_2) \wedge (V_3 < V_{DS} < V_4) \Rightarrow (I_1 < I_{DS} < I_2)$$

In this work, the computation of the minimum and maximum current values for each set of intervals in the above equation is done with on the fly calls to the circuit simulator during the SAT simulation.

Additional constraints capturing the connection of the devices must be provided to the SAT solver for the correct DC operating point analysis. At an EP, there is no variation of node voltages in the circuit. This means that the current flowing through each node capacitor is equal to zero. KCL is applied on each node of the circuit assuming positive sign for the currents flowing in the node and negative sign for the currents flowing out of the node. The nodal KCL equations are then provided in the SAT solver as constraints of the form:

$$I_n + \dots - I_m - \dots = 0$$

where I_i is the current of a device connected to the node.

Implementation of the SAT-based methodology using the Yices solver

The implementation of the SAT-based methodology was realised using Python scripts. The flowchart of Figure 40 presents a detailed view of the steps taken during the verification process. Initially, a SPICE netlist and a settings file are passed as an input to the script (#1). Recalling the analysis in the previous section, Yices output is given in terms of state variable intervals. For instance, in a circuit with three nodes $\{N_1, N_2, N_3\}$, an output with a potential solution will be of the form:

$$I = \{(N1_a, N1_b), (N2_a, N2_b), (N3_a, N3_b)\}$$

During the algorithm execution, three structures are used for storing the results: FINAL for the final results and tempA, tempB for temporary results between stages.

In the first step of the analysis, temporary solution intervals for each node are generated and added on tempA based on the

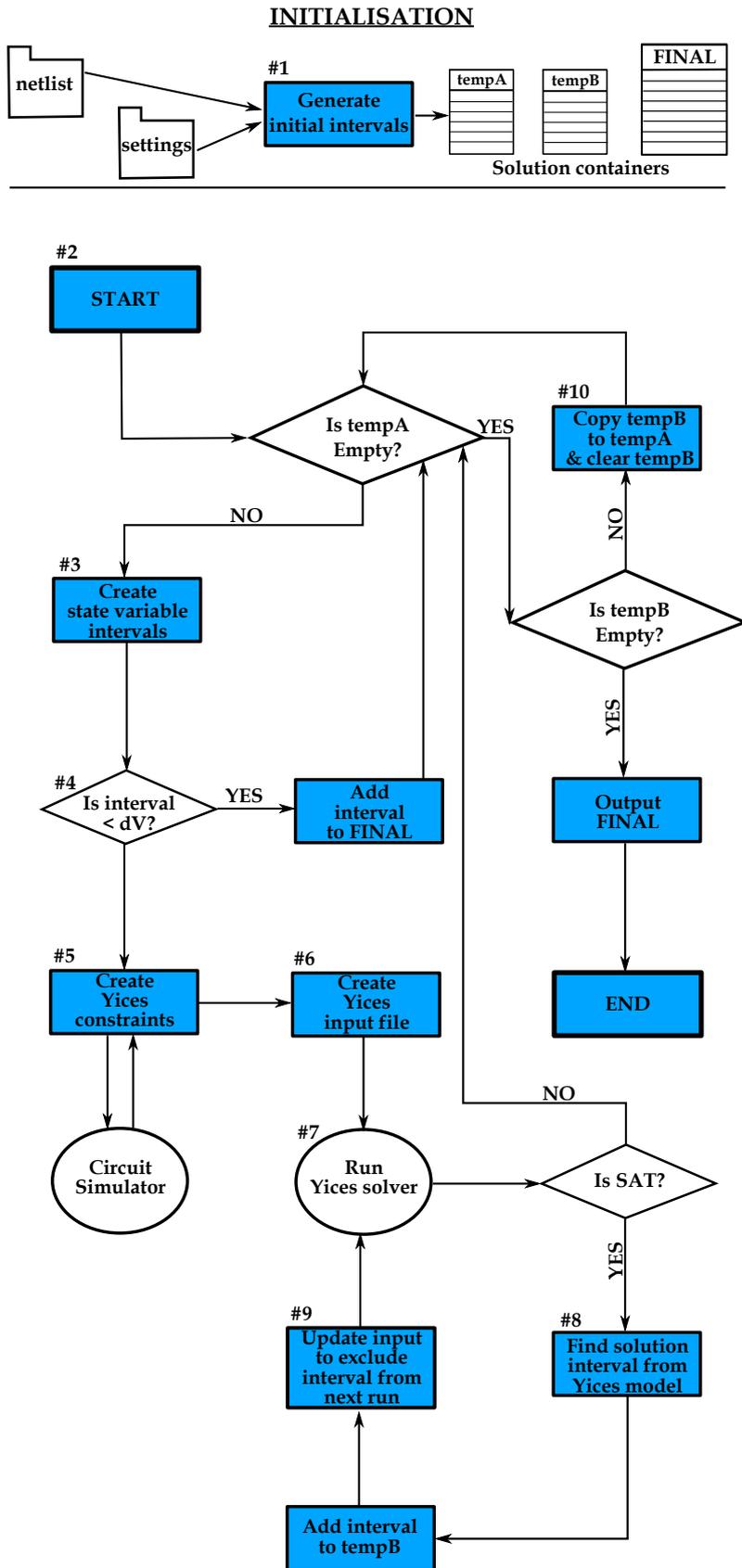


Figure 40: Flowchart with the implementation of the SAT-based verification methodology.

minimum and maximum values of the state variables. In the next step (#3), the state space is partitioned in many different areas by equally splitting the initial interval of each variable into k number of intervals defined in the settings file. The length of each of the new intervals is then compared (#4) to a value dV which defines the minimum length threshold of the solution interval for which a solution is considered final. A typical value for dV can be 10mV but generally it depends on the desired accuracy. On the one hand, if a variable interval is less than dV , the solution is saved in the structure with the final solutions and it is not processed further. On the other hand, if none of the intervals is less than dV , the algorithm proceeds with the generation of the appropriate Yices constraints (#5). These include both the KCL equations for the circuit and the determination of the minimum and maximum currents for each set of intervals for the nonlinear devices. The latter is achieved by direct calls to the circuit simulator for batch DC operating point analysis on each nonlinear device.

Based on the initial netlist and the generated constraints, an input file in Yices format is created (#6) and fed into the Yices solver for simulation (#7). If Yices can prove the satisfiability of the expressions, a model with actual values for the node voltages is returned. Using that model, the corresponding set of solution intervals is found (#8) and added to the temporary solution structure `tempB`. Given that we are interested in an exhaustive search for potential solutions, the Yices input file is updated with a formula that excludes the latest solution. This procedure is run until Yices cannot find any other solution and returns *UNSAT*.

The temporary solutions in the intermediate steps of the analysis are stored in two structures. This can reduce the amount of simulations because at (#10), before copying the results of `tempB` to `tempA`, an attempt to merge neighbouring potential solution intervals of `tempB` is made. The algorithm ends when both temporary structures contain no solution intervals for further analysis.

In Figure 41, the actual process is presented in six steps during the analysis of a pair of cross-coupled inverters under supply voltage equal to 1V. In the beginning, each state variable is split into two intervals $I_1 = [0, 0.5]$ and $I_2 = [0.5, 1]$ and the solver searches for areas in the state space that the model does not have any solutions. As the number of runs is increased and the state variables are refined further, the solver successfully returns a final set of intervals, the length of which can be controlled by the dV parameter of the settings file.

4.2.2 Existence of equilibrium point

The modelling approach during the formulation of the DC operating point analysis as a SAT problem guarantees the formal nature of the final results. Given the conservative construction

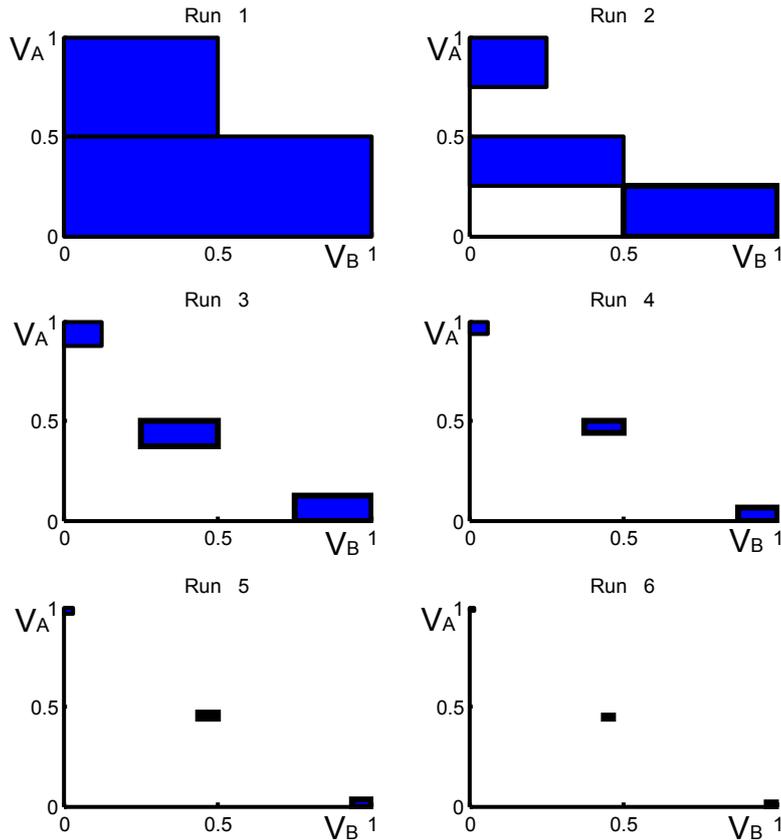


Figure 41: Gradual reduction of the areas in the state space that may contain an EP in a bistable element using Yices. The two stable and one metastable point in Run 6 are enclosed in a rectangle with dimensions of a few mV.

of the $I - V$ transistor expressions, the output of the SAT solver includes all the potential EP of the circuit. Although this means that a solution is not possible to be excluded from the final results, it also means that some listed solutions may not actually be EP of the circuit. For this reason, a checking mechanism must be implemented after the SAT process in order to filter out the false solutions.

This mechanism can be easily implemented by taking advantage of the *nodeset* option in the DC analysis of the circuit simulator. Nodesets are used both in DC operating point and during the initialisation of the transient simulation. They can be supplied in the simulator and force specific nodes to certain values which are used as an initial guess of the final solution. The Newton-Raphson method discussed in Section 2.2.2 starts using an initial guess. If nodesets are not given, the simulation will choose the initial values based on the operating point regions of the nonlinear devices. Nodesets are an important tool in two major cases. Firstly, when a circuit has multiple DC solutions, they are used to guide the simulator towards the desired solution. This case is similar to the way used for the proof of existence in

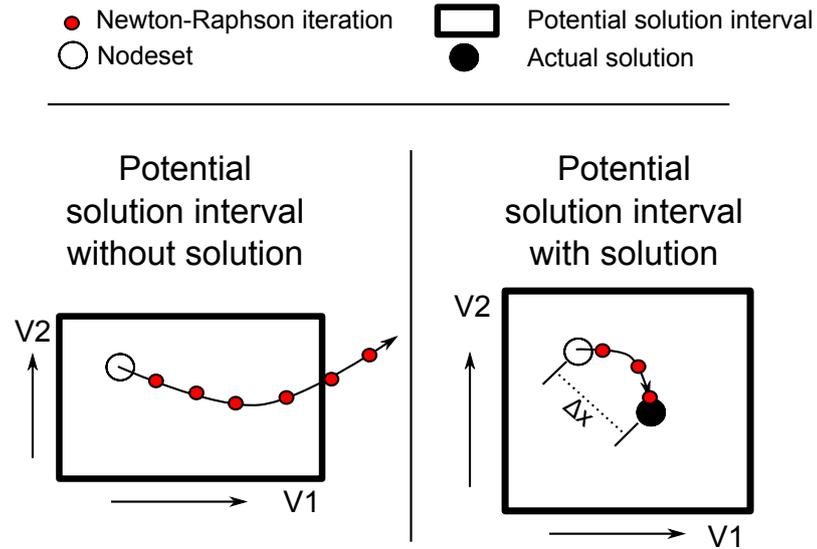


Figure 42: Graphical representation of the check for the existence of EP using the circuit simulator *nodeset* option.

the presented flow. Secondly, when they provide a close approximation of the real solution, nodesets can eliminate convergence problems and speed up the DC operating point analysis.

Algorithm 1 Checking existence of DC equilibria

```

{*** P: list of intervals with potential EP from SAT solver}
{*** EQ: list with verified equilibria}
EQ = ()
for all p ∈ P do
  nodeset = Random(p)
  op = RunSpice(nodeset)
  if op ∈ p then
    EQ = Add(p)
  end if
end for
Return(EQ)

```

Algorithm 1 presents the verification steps and Figure 42 graphically elucidates the determination process of potential EP existence. Assuming a two-dimensional case with two state variables $V1$ and $V2$, the SAT solver returns N sets of intervals for $V1$ and $V2$ which may contain EP. A random point $r = (V1r, V2r)$ is selected for each set of the N intervals and is used as an initial guess for the DC analysis using the *nodeset* option in the simulator. On the left, it is clear that after five Newton-Raphson iterations the simulator is driving the circuit solution out of the initial rectangle defined by SAT solver output. The circuit settles on an EP in a different area of the state space and it can be determined that this potential solution interval does not contain a solution. On the right, the simulator after three Newton-Raphson iterations locates an EP in the potential solution interval, Δx far

from the initial guess. It is important to note that an appropriate value for the maximum length of the intervals of V1 and V2 should be chosen during the formulation of the SAT model.

4.2.3 Stability of equilibrium point

The final part of the analysis for this section is the evaluation of the stability of all EP. It is particularly important during the oscillatory behaviour of the circuit. By proving that all EP are unstable, we can exclude the possibility of a lock-up and guarantee that a circuit sustains an oscillation.

To determine the stability properties of a circuit, a local linearisation of the system at each operating point must be performed. This can be achieved using the Jacobian (Section 2.1). Assuming a general ODE model $\dot{V} = f(V(t))$, the linearised equivalent in the neighbourhood of an EP is $\dot{V} = \text{Jac.}(V(t) - V_{EP})$, where V_{EP} is the EP and Jac is the Jacobian evaluated on V_{EP} . The solution of this ODE is $V(t) = V_{EP} + e^{t \cdot \text{Jac.}} \cdot (V - V_{EP})$. The sign of the eigenvalues of the Jacobian matrix decides the stability of an EP. If the real part of every eigenvalue is negative, the exponential term will approach zero as time approaches infinity and thus the EP will be stable. Otherwise, it will be unstable.

The expression of the Jacobian for an analytic ODE model can take a symbolic form based on state variables, time and other parameters. The calculation of such an expression is trivial. However, an analytic expression is not possible to be obtained for CMOS circuits described by complicated models. For this reason, an approximation of the Jacobian must be performed. Traditionally, a forward difference is used for the first order derivatives. The partial derivatives are calculated using the EP $(a_1, a_2, \dots, a_i, \dots, a_N)$ and a slightly perturbed point:

$$\frac{\partial f}{\partial V_i} = \frac{f(a_1, a_2, \dots, a_i + h, \dots, a_N) - f(a_1, a_2, \dots, a_i, \dots, a_N)}{h}$$

In the second case, the EP is not used in the calculations but the final result is computed using two slightly perturbed values:

The calculation of the Jacobian requires an ODE circuit model. For this reason, the approach presented in Section 3.2.2 is adopted using Equation 2:

$$\dot{V} = C^{-1} \cdot M \cdot I_{DS}(V, t)$$

A positive fixed value capacitance from each node to the ground is assumed. The node capacitance for each operating point can be calculated by enabling the simulator's *captab* parameter which outputs a capacitance matrix for the circuit. Recalling that the terms of the Jacobian are of the form $\text{Jac}(i, j) = \partial V_i / \partial V_j$ and assuming that the node capacitance remains constant for small node voltage perturbations, the calculation of the partial derivatives of the transistor currents $I_{DS}(V, t)$ with respect to the node voltages is the quantity of interest.

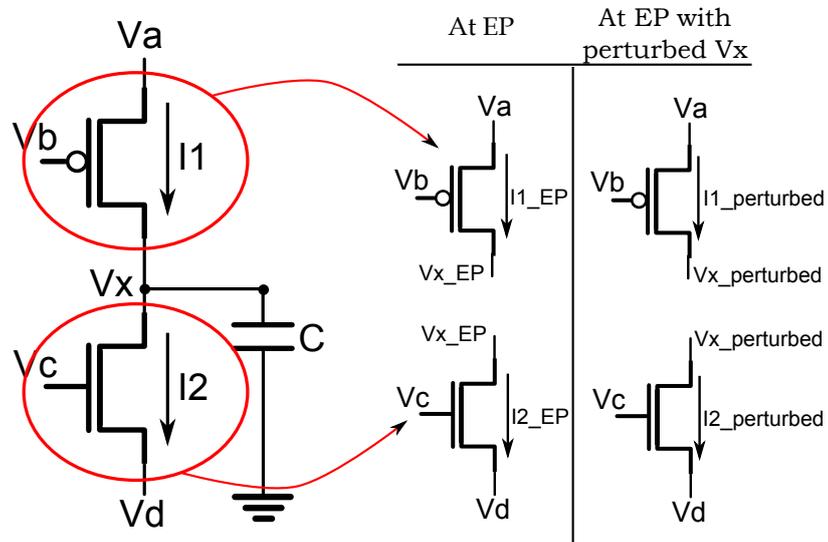


Figure 43: Isolation of transistors connected to the node of interest in a first order example in order to determine the currents for the calculation of the Jacobian.

Algorithm 2 Checking stability of DC equilibria

```

{** EQ: list with verified equilibria}
{** EQ_stable: list with stable equilibria}
EQ_stable = ()
for all eq ∈ EQ do
  jac = Jacobian(eq)
  eig = Eigenvalues(jac)
  if max(Re(eig)) < 0 then
    EQ_stable = Add(eq)
  end if
end for
Return(EQ_stable)

```

The implementation in this work proceeds as described in Algorithm 2 and as presented in Figure 43. In this first order example, the ODE on the node V_X is $\dot{V}_X = C.(I_1 - I_2)$. The Jacobian is:

$$\text{Jac}_{V_x} = C.(\frac{\partial I_1}{\partial V_x} - \frac{\partial I_2}{\partial V_x})$$

For the calculation of the Jacobian, each transistor connected to the node of interest is isolated. Then, two DC operating point simulations are run using the node voltages on the equilibrium point $(V_a, V_b, V_{x_EP}, V_c, V_d)$ and on slightly perturbed operating point $(V_a, V_b, V_{x_EP} + \Delta V, V_c, V_d)$ in order to determine the transistor current in both cases. Calculating the Jacobian from this point is straightforward.

4.3 DETECTION OF PERIODIC ATTRACTORS USING VECTOR FIELD SIMULATION

Formal proof of the non-existence of stable periodic orbits in a N-dimensional dynamical system is hard to achieve. Although it is possible to resort to analytical techniques, their applicability is restricted mainly to autonomous planar vector fields [77]. Numerical integration is a standard method for the solution of an ODE system. Stable periodic orbits can be detected as the integration time t , if a system's initial condition V_0 at time t_0 belongs to the attracting region of the orbit.

In this analysis, we need to show the non-existence of oscillating modes in the circuit for an interval $IV = [X_{min}, X_{max}]$ of a parameter X . Formal verification for the continuous interval IV could be attempted using reachability analysis of uncertain non-linear systems. To keep the problem tractable, a set of equidistant discrete values of X is generated from IV . The analysis will be performed for each value of X . If the difference between consecutive values is small enough, the results can be generalised for the whole interval. However, they still remain not formal in nature.

Running multiple transient SPICE simulations from different initial points in the state space for adequate time in order to observe oscillation is computationally expensive. Instead, the search for periodic orbits is based on the construction of the vector field of the ODE system. A similar technique is presented in [78] and is also used in [79].

Algorithm 3 presents the two-step process for the verification of the non-existence of periodic solutions in a circuit block. Assuming that a circuit is described by a generic continuous ODE model $\dot{V} = f(V(t), t)$, the first step of the process requires the construction of a discrete vector field D for the continuous state space defined by the node voltages V . For this reason, an m -point uniform sampling is applied for each of the N state variables, leading to a set $S = \{s_1, s_2, \dots, s_{N^m}\}$ of N^m sampling points. Increasing m will improve the accuracy of the discrete model but the vector field computation time will also increase exponen-

Algorithm 3 Vector field generation and simulation

```

{** t0: transient simulation time}
{** S: sampled state space points}
{** dV: derivatives at sampled state space points}
dV = ()
for all s ∈ S do
    ic = s
    s+ = RunSpice(ic,t0)
    dV = Add( $\frac{s_+ - s}{t_0}$ )
end for
{** tVF: total vector field simulation time}
{** R: random initial conditions in the state space}
{** sol: solution vector}
for all r ∈ R do
    solj = Add(r)
    while t < tVF do
        s = DetectNearest(solj.Last,S)
        solj = Add(solj.Last+dV(s).Δt)
        Update(t)
    end while
    j = j+1
end for

```

tially. Non-uniform sampling based on the homogeneity of the continuous vector field can provide a trade-off between the two.

The calculation of the vector field at each sampling point s_i can be performed using a circuit simulator. A transient analysis starting from an initial condition equal to s_i is set up for each point. The initial condition ic can be easily defined by instructing the simulator to bypass the DC operating point analysis and to use the user provided values. The simulation is run for a minimum time t_0 , sufficiently long to avoid integration errors from the simulator. State of the art simulators use adaptive techniques to control the simulation time step in order to meet the criteria that guarantee the correctness of the results. Thus, a specific value is not possible to be explicitly selected. For the proposed flow, a value of $t_0 = 0.5\text{ps}$, which is large enough to produce a meaningful result and small enough not to calculate many intermediate steps, was selected. The result of the transient simulation is a final solution s_{i+} at time t_0 . The vector dV that defines the direction and the rate of change of the solution at each sampling point can be approximated by:

$$dV_{s_i} = \frac{s_{i+} - s_i}{t_0}$$

A discrete vector field $D = \{dV(s_i) : \forall s_i \in S\}$ for the complete state space is generated by applying this method. The behaviour of the state variables and therefore the structural properties of the state space is captured within D .

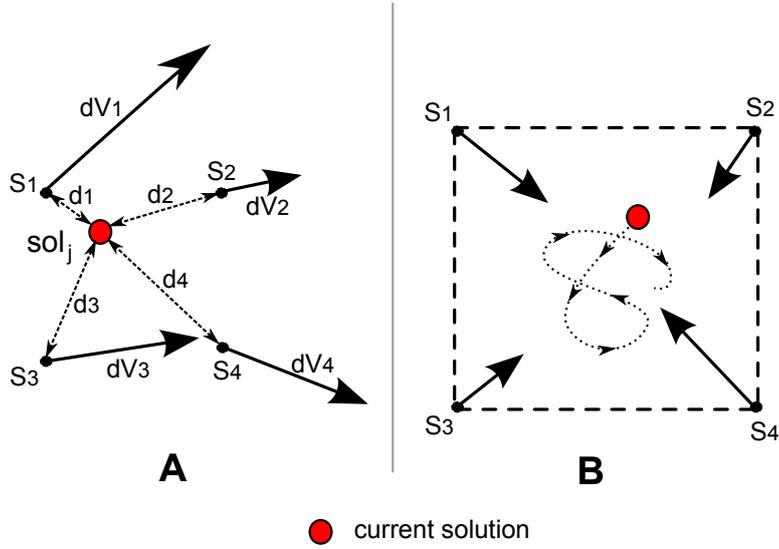


Figure 44: A: Distance d_i of neighbouring sampling points s_i from current solution sol_j in a two-dimensional vector field. B: Solution settling to an area with a stable EP in a two-dimensional vector field.

The second step of the process involves running multiple vector field simulations starting from a random set $R = \{r_1, r_2, \dots, r_i\}$ of initial conditions. Vector field simulations provide a faster alternative to traditional SPICE simulations by using the data generated in the first step of the process in order to produce solutions with initial conditions covering most part of the state space. An appropriate simulation time t_{VF} and a set of initial conditions R are selected. In most cases, an approximate period of potential oscillation for the circuit under verification is known in advance and t_{VF} can be set accordingly.

Vector field simulation depends on two major components: time step selection and solution update. Although different time step selection methods were tested, a fixed time step of $\Delta t = 1ps$ was used for the simulations in this work. Time step selection is directly related to the time constants of the circuit and the fixed time step should be at least one order of magnitude less than the time constant of the fastest node of the circuit in order for the results to be acceptable. Optimal selection can be performed by controlling the maximum node voltage change using a variable time step which depends on the node voltage derivatives.

Given the discrete nature of the generated vector field, the solution update method is based on approximating the value of the vector field at the current solution point sol_j with the vector field at the nearest sampling point:

$$dV(sol_j) = dV(\min\{|s_i - sol_j| : \forall s_i \in S\})$$

Figure 44.A shows that process in a two-dimensional vector field. Using this approximation, the solution updates are calculated using the following equation:

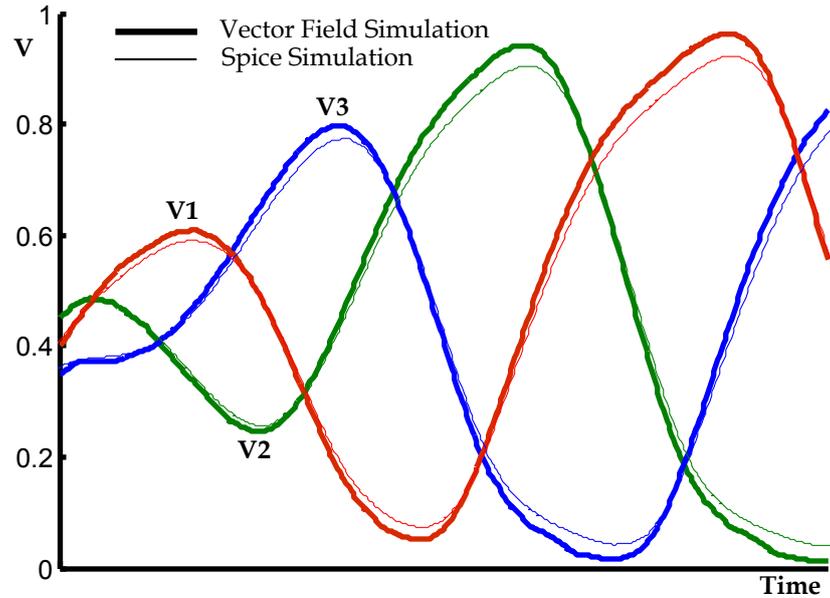


Figure 45: Comparison of node voltages over time on a three-stage ring oscillator between vector field simulation and traditional SPICE simulation starting from the same initial condition. Uniform state space sampling with 20 points (50mV) per node voltage was used.

$$\text{sol}_j(t + \Delta t) = \text{sol}_j(t) + \Delta t \cdot dV(\text{sol}_j(t))$$

Oscillatory behaviour can then be checked either visually or by sampling the solution of the vector field simulation at periodic intervals. In figure 45, the three node voltages V_1, V_2, V_3 of a three-stage ring oscillator over time are plotted for both a vector field and a traditional SPICE transient simulation. Both simulations start from the same initial condition and uniform sampling with 50mV difference between consecutive sampling points is performed. In a two-dimensional example involving a stationary solution, Figure 44.B shows a close view of a solution settling on a location in the state space with a stable EP. Finally, the three-dimensional example in Figure 46 shows the vector field of a three-stage ring oscillator and the simulation results of two runs starting from random points in the state space. Both solutions follow the flow and eventually converge to the periodic attractor.

4.4 SUMMARY AND CONCLUSIONS

Proliferation of AMS and SOC designs has led to the diversification of the specifications in oscillating circuits. Naturally, the variety and the complexity of oscillators have surged in order to meet the particular design goals. Despite the fact that traditional transient and PSS simulations are needed for the verification of these designs, increased challenges demand the complement of existing methods with additional techniques for the fabrication of correct by design circuit blocks.

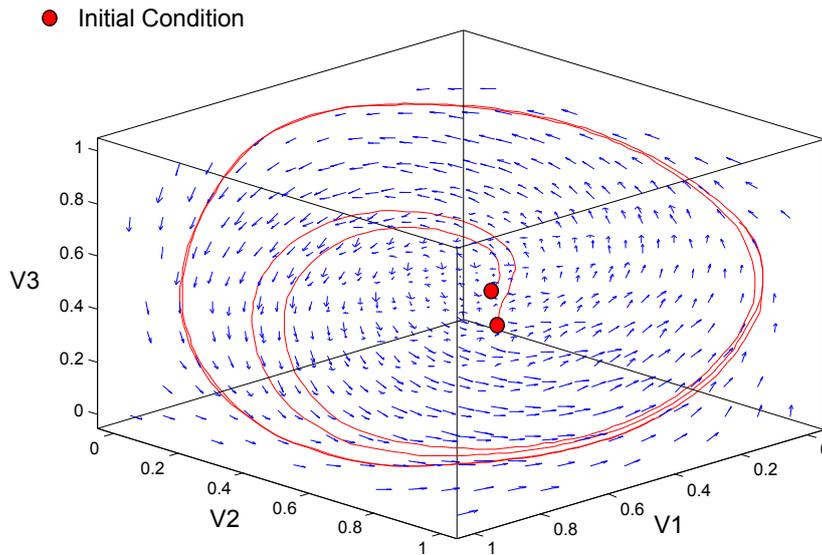


Figure 46: Vector field of a three-stage ring oscillator and two vector field simulations starting from random initial conditions with the solutions converging to the periodic attractor. Uniform state space sampling with 20 points (50mV) per node voltage was used.

This chapter presented a novel automated flow for the characterisation of the structural properties of the state space in complex and unconventional oscillating circuits under parameter variations. The flow is separated in two different branches. The first branch is based on a SAT based methodology and on basic dynamical system theory. It deals with the exhaustive detection and stability analysis of EP in the state space and allows the generation of a formal proof for a lock-up free oscillatory behaviour. The second branch is concerned with the proof of existence or non-existence of periodic orbits in the state space under certain operating conditions using vector field modelling and simulations. The combination of the two branches provides a complete map of the state space and can be used not only for the verification of the correct circuit operation but also for the exploration of novel applications of existing structures.

5

VOLTAGE SENSING BASED ON TRANSIENT MODE SWITCHING

5.1 INTRODUCTION

The proliferation of SoC designs with the integration of AMS components on the same platform has led to the presence of many different voltage levels on the same chip. In addition to high performance applications, power supply variations are also an intrinsic characteristic of energy harvesting designs used, for instance, in wireless sensor networks and biomedical applications, based on non-deterministic energy sources.

Power supply voltage and internal subsystem voltages can no longer be considered static parameters in a system. Traditionally, flash A2D converters are used for the conversion of an analog signal to a digital code in high frequency applications [80]. A wide range of methods have also been used in energy harvesting systems. In [81], a process invariant sensor consisting of a bandgap reference, a comparator, a resistor divider and a CMOS output driver is presented. Curty et al [48] propose a simple sensor named POR that consists of a pair of cross coupled inverters and a capacitor. Kocer et al [49] present a sensing circuit named Mode Selector. This design consists of a differential stage and two resistor ladders that are replaced by active loads in a subsequently improved version [50]. Using a different concept, Shang et al [53] present a reference free voltage sensor that produces a thermometer code by comparing the latency of two different circuits powered by the V_{DD} to be sensed.

This chapter proposes a novel voltage sensing technique. and investigates how the change of operating modes in a circuit can be used for the identification of a voltage threshold crossing. In particular, the properties of an autonomous even stage ring oscillator with inherent sensitivity to the supply voltage are studied and its ability to either oscillate or latch depending on the value of V_{DD} is analysed. The proposed approach has two main advantages over existing methods. First, the compact implementation with only digital components simplifies the integration in prevalent digital design flows. The removal of analog components (resistors, capacitors) also allows for a greatly reduced circuit area. Second, the inherent, and tunable, properties of the circuit define the switching voltage threshold and thus an external voltage reference is not necessary.

The remainder of the chapter is organised as follows. In section 5.2, the theoretical basis behind the proposed voltage sensing technique is developed. Section 5.3 contains the actual realisation of the technique on an even stage ring oscillator with

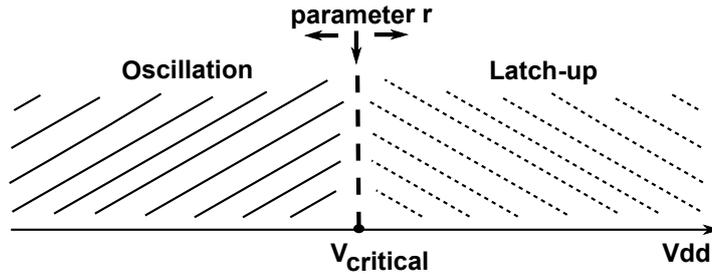


Figure 47: Using r to control $V_{critical}$ which describes the boundary between the stationary and oscillatory modes.

detailed analysis and verification based on both dynamical systems theory and SPICE simulations. Finally, summary and conclusions complete the chapter.

5.2 PROPOSED VOLTAGE SENSING METHOD

The idea behind the proposed voltage sensing technique stems from the wealth of phenomena in dynamical systems. As discussed in previous chapters, varying a parameter in a system can result in not only a quantitative but also a qualitative change. In most cases, extreme changes which completely alter the behaviour of a system are undesirable because they usually lead to the violation of the initial specifications. Nevertheless, thorough characterisation and understanding of these occurrences can also lead to their utilisation in novel applications.

The ODE system that represents the theoretical model of the proposed voltage sensor is

$$\dot{V} = f(V(t), r, V_{DD})$$

with r and V_{DD} being system parameters. The transition from a stationary state to a motion as described by a bifurcation involving equilibrium points and periodic solutions can be used for the detection of a predefined voltage threshold crossing. Figure 47 graphically presents this idea. The power supply V_{DD} can freely fluctuate in a wide interval and parameter r is appropriately fixed in order to control the critical bifurcation point at which the transition from the static to the oscillatory mode occurs.

Figure 48 shows a schematic of a potential circuit implementation. A simple configuration with a 3 bit counter connected to an internal node of the circuit is set to 000. The number of bits in the counter depends on the specifications (rate of V_{DD} change, sensor response time etc). The counter waits for the oscillating signal which acts as the clock for the counting and the most significant bit of the counter serves as the ENABLE signal that informs the rest of the circuit about the change in the V_{DD} level. Additionally, the ENABLE signal can also be used to stop the oscillation by either disconnecting the power supply from the circuit or by changing its configuration.

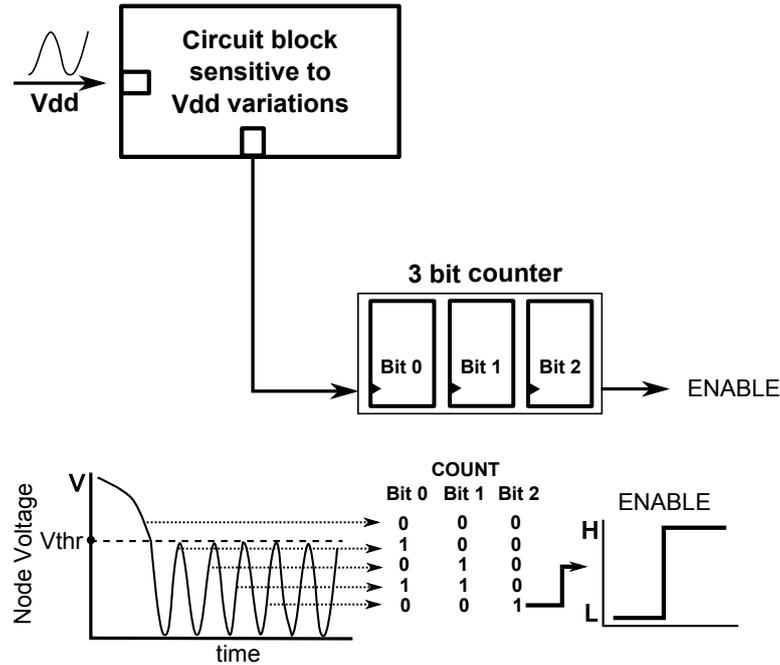


Figure 48: Configuration for the detection of the onset of oscillation.

As V_{DD} decreases, the onset of oscillation at specific V_{DD} threshold points for each value of r is observed. The direct relation of r to the V_{DD} levels and the change of the stationary latching mode of the RO to an active oscillatory mode can be used to detect fixed predefined V_{DD} levels in a circuit.

5.3 REFERENCE-FREE AND TUNABLE VOLTAGE THRESHOLD DETECTOR

The requirements set by the theoretical model described in the previous section can be met by an unconventional even stage ring oscillator (Figure 49). A detailed analysis based on theoretical findings and SPICE simulations follows.

5.3.1 Description of an even-stage ring oscillator

Two equivalent representations of an even stage ring oscillator are shown in Figure 49. Each stage is enclosed in a dashed rectangle in Figure 49.B and it consists of two forward inverters (labelled F) and a set of cross-coupled inverters (labelled CC). The behaviour of the two-stage ring oscillator under nominal supply voltage can be elucidated by studying the two equivalent representations.

In Figure 49.A, the closed loop consisting of four inverters is highlighted. Assuming that the cross-coupled inverter pairs do not exist, a simple four-stage ring oscillator alone cannot sustain an oscillation due to the insufficient phase shift around the loop.

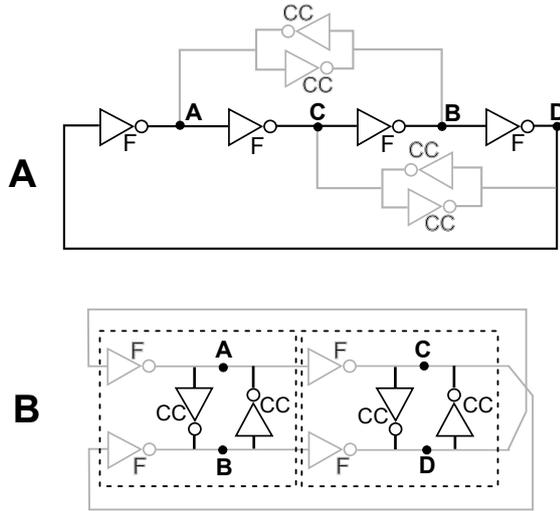


Figure 49: Two equivalent representations of an even-stage ring oscillator. The closed loop is in bold type in A and the cross-coupled inverters in B.

The only possible stable solution for the circuit is the *latch-up* or *lock-up* mode under which the values for the node voltages ABCD can be either HLHL or LHLH, where H is the logic high and L is the logic low. It should be noted that the unstable equilibrium at around half the supply voltage for each node can also be a solution of the system, although it will eventually converge to one of the two stable EP.

The alternate representation of Figure 49.B provides a visual explanation about the significance of the cross-coupled inverters in the circuit. They are used as a connecting element between the nodes of same value in the four-stage inverter ring under the locking mode, namely (A, C) and (B, D). As discussed in Chapter 2, under nominal supply voltage, a cross-coupled pair of inverters has three EP, two of which are stable and one is unstable. Assuming the node voltages are labelled (M, N), the two stable EP settle in either HL or LH. However, the inherent desire of the cross-coupled pair to reach one of these stable EP is in complete contrast with the dynamics of the inverter ring. The battle between the two is the reason behind the onset and the sustainment of the oscillation.

The winner of this battle depends on the strength of the forward and the cross-coupled inverters. Assuming that the width W of the nMOS is half that of the pMOS for each inverter, a quantifiable measure of relative strength can be given by:

$$r = \frac{\text{width of CC}}{\text{width of F}} \quad (15)$$

, where the widths refer to the nMOS transistor of the inverters.

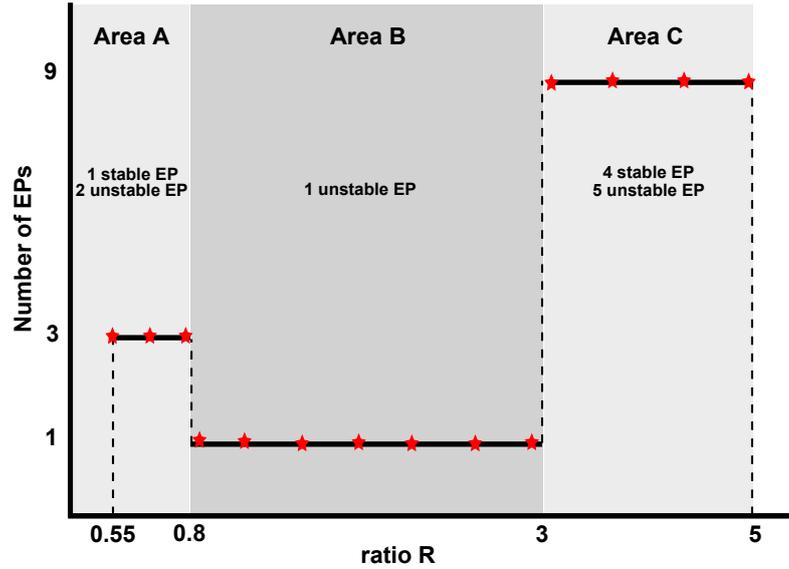


Figure 50: Number of EP versus ratio r .

5.3.2 Behaviour under variable ratio r

Selecting a proper value for r is critical in order to achieve the desired oscillating behaviour. In a recent example [1], researchers from Rambus issued a verification challenge for this design when some oscillators failed to oscillate after fabrication. The dependence of the circuit behaviour to the ratio r may lead to either a permanent lock-up mode or to a coexistence of periodic solutions and stable equilibria in the state space. In the second case, the initial conditions of the system determine the final behaviour of the circuit.

The sensitivity of the even-stage ring oscillator to the ratio r under a nominal power supply has been extensively studied. In [33], the authors use a pen and pencil approach to provide an analysis that leads to an interval for r , in which the circuit always oscillates. Tiwary et al [30] use the circuit as an example for their DC operating point searching method, while in [79] a multiparticle simulation is employed to visualise the areas that lead to latching and oscillatory behaviour.

The work in this section complements previous studies. As the appearance of equilibrium points is the reason behind the lock-up, all EP for a wide range of the ratio r are located and classified according to their stability using the automated flow presented in Chapter 4. This analysis provides an initial basis for the understanding of the state space dynamics, which is valuable for the subsequent usage of the circuit as a voltage sensor.

In this investigation, the width of the CC inverters is set equal to $W_{CC} = 600n$ and the width of the F inverters is varied from the minimum value of $W_{Fmin} = 120n$ to $W_{Fmax} = 1080n$ in order to create a range $R = [0.55, 5]$ for the ratio r . Figure 50 presents the number of calculated EP versus the value of ratio r . Three different areas A, B and C can be observed. Area B corre-

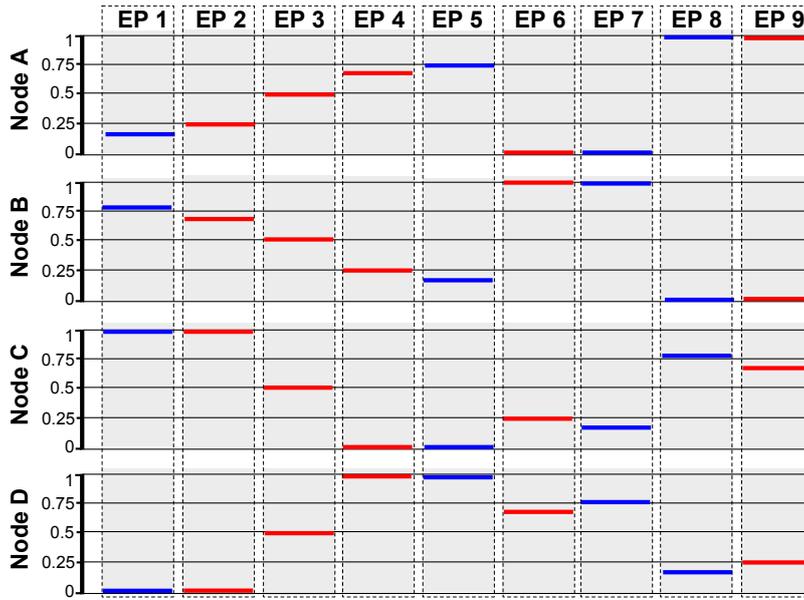


Figure 51: Node voltage levels of each EP under nominal power supply for ratio $r = 3$. Blue levels are stable EP and red levels are unstable EP.

sponds to the interval $B = [0.65, 3[$ for r in which the circuit has only one unstable EP. For this range of values for r , the oscillatory behaviour of the circuit can be guaranteed.

As r increases above 3 in Area C, the relative strength of the CC inverters crosses a critical point and bifurcations occur in the system. The structural properties of the state space are altered and eight new EP appear. The characterisation of the new EP in terms of stability shows that all have real eigenvalues with four being stable nodes and four being saddles, which are always unstable. Because of the high dimensionality of the system, a comprehensive plot with all the structures in the state space cannot be easily generated. However, a visual inspection of the node voltage levels corresponding to each EP for a ratio $r = 3$ can be done in Figure 51, where the blue levels are stable EP and the red levels are unstable EP. Because of symmetry in the circuit, excluding EP₃ which corresponds to the metastable point of the closed loop inverter ring, the combination of node voltage levels for the remaining EP have obvious similarities.

As the ratio r decreases below 1 and the F inverters overpower the CC inverters, there is another critical value at $r = 0.8$ which results in bifurcations in the circuit. Area A in Figure 50 shows that one stable and one unstable EP are created in the state space. It was shown in [79] that for values of r in this area, the circuit can either oscillate or lock-up depending on the initial conditions. This is a potentially dangerous situation for the designer and that is the reason all unconventional oscillating structures must be fully verified (with flows in Chapter 4) before fabrication.

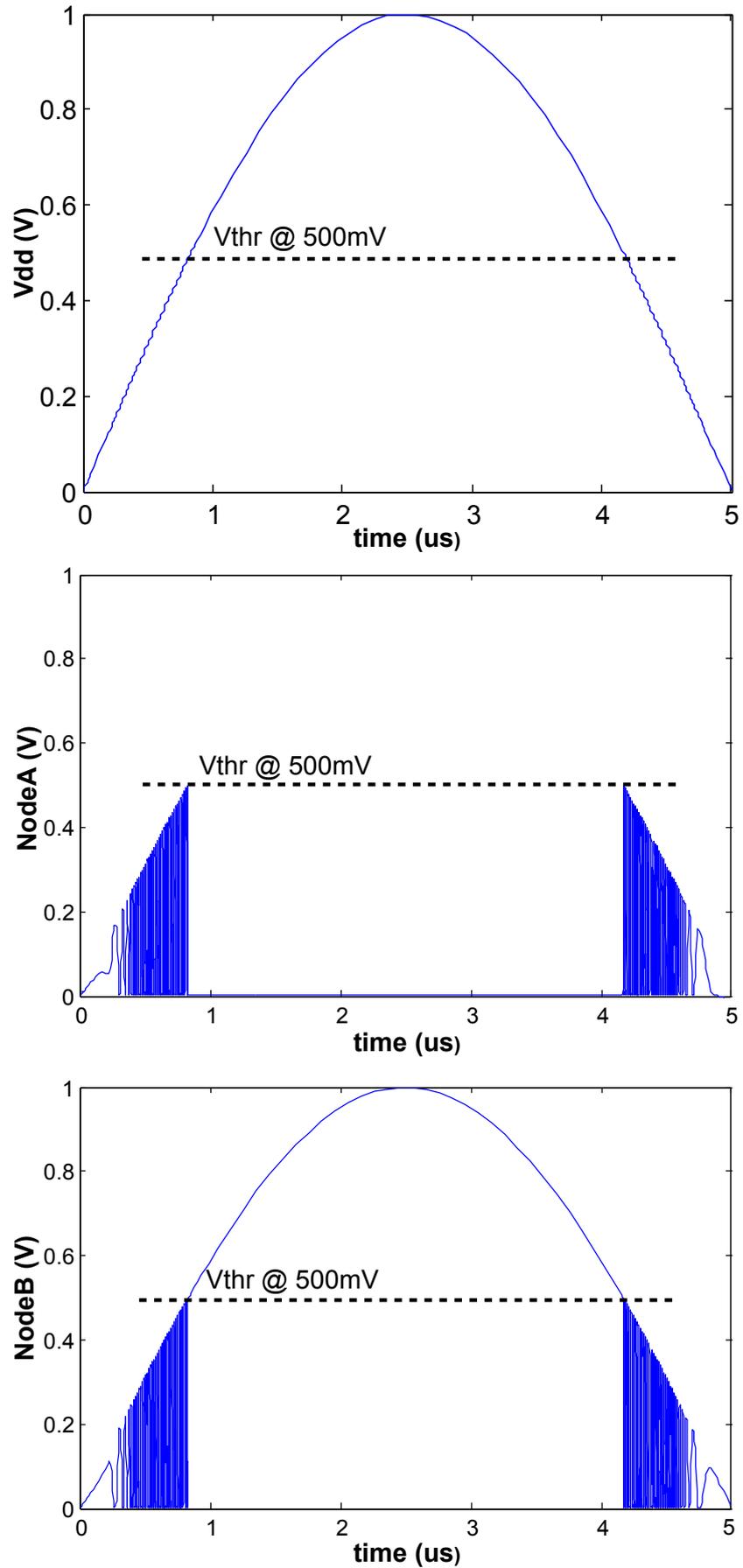


Figure 52: Simulation results showing the voltage waveforms for nodes A and B under sinusoidal supply voltage of amplitude 1V and frequency 100k for a ratio $r = 5$.

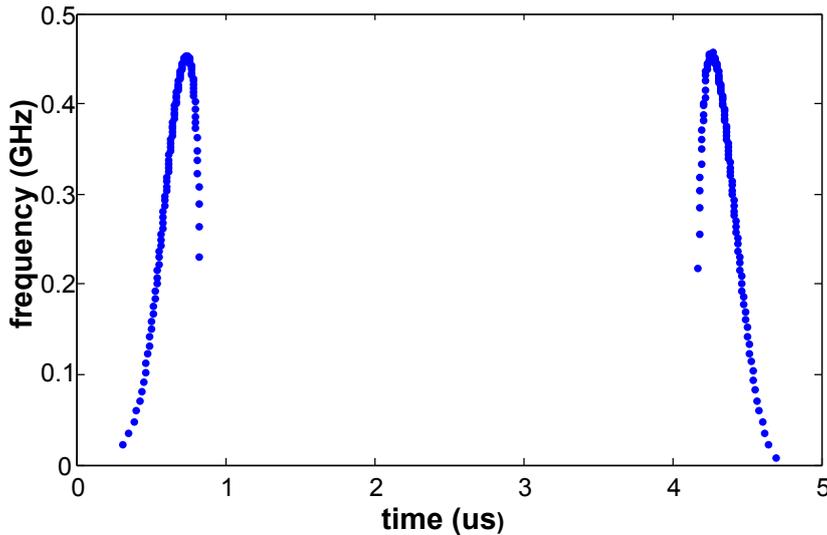


Figure 53: Frequency of oscillation for a ratio $r = 5$.

5.3.3 Behaviour under variable supply voltage

In this section, an investigation of the circuit behaviour under variable supply voltage is presented. Given a ratio r in Area C (Figure 50) where the latch-up occurs, it is interesting to study how the relative strength of the F and the CC inverters is altered as V_{DD} drops from its nominal value. For this reason, the ring oscillator with ratio $r=5$ is simulated under sinusoidal supply voltage of amplitude 1V and frequency 100k. The two node voltages and the supply voltage over time are presented in Figure 52. As V_{DD} drops below 500mV, the dynamics are altered in the state space of the circuit and a bifurcation results in an oscillation with the behaviour of the circuit effectively resembling the behaviour in Area B under nominal power supply. The onset of the oscillation signals a specific and predefined voltage threshold crossing allowing the ring oscillator to operate as a voltage threshold detector.

An important detail about the circuit behaviour is shown in Figure 53. As V_{DD} drops below the critical value of 500mV, the circuit initially oscillates with an increasing frequency despite the fact that V_{DD} decreases and then this counterintuitive phenomenon terminates at a secondary power supply level.

Figure 54 presents the connecting relation between the ratio r and the critical power supply level signalling the onset of the oscillatory behaviour. The relation between the two is nonlinear and the accuracy of the sensor can be controlled more easily at voltage levels less than 0.7V.

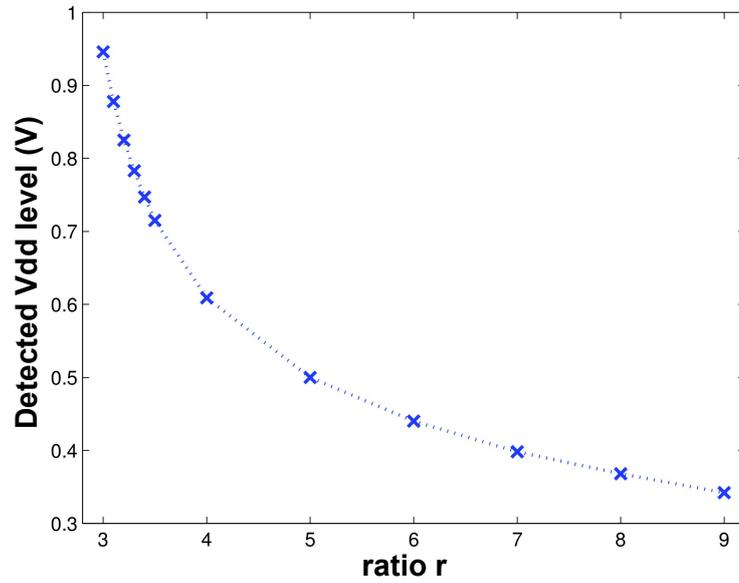


Figure 54: Connecting relation between ratio r and detected voltage level for F inverters of minimum width.

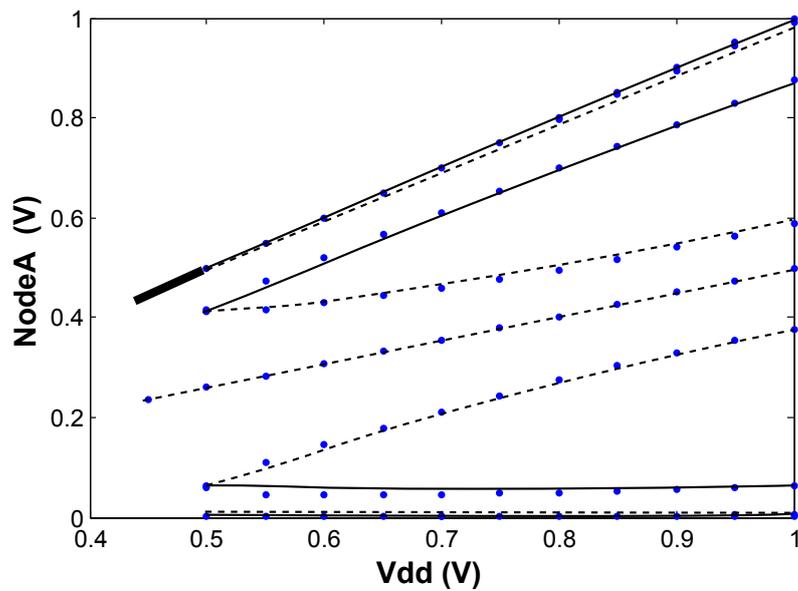


Figure 55: Bifurcation diagram for ratio $r=5$ created by sweeping V_{DD} from 450mV to 1V using the flow presented in Chapter 4.

5.3.4 *Verification of the correct operation*

The verification of the correct operation of the even stage ring oscillator as a voltage sensing device under variable supply voltage is twofold. Assume that a ratio r sets the boundary between the two regions in Figure 48 at V_{critical} . First, it must be proved that for V_{DD} less than V_{critical} , the circuit never enters the latching mode before the generation of the ENABLE signal. Depending on the rate at which the supply voltage changes, it is usually adequate to prove exclusive oscillating behaviour for a few tenths of mV in this region. Second, it must be proved that for V_{DD} more than V_{critical} , the circuit remains in the latching mode and never oscillates. Otherwise, the ENABLE signal would be generated and the correct operation of the sensor would be compromised.

The verification of the sensor is based on the two automated flows of Chapter 4. Figure 55 shows the bifurcation diagram for ratio $r=5$ with V_{DD} sampled at 50mV intervals. For V_{DD} less than 500mV the oscillatory behaviour is guaranteed as the state space apart from the periodic attractor contains only an unstable EP. As V_{DD} crosses 500mV, four new stable and four new unstable branches are generated. The existence of stable EP in the state space does not guarantee the latching behaviour of the circuit as some initial conditions in a potential limit cycle's basin of attraction may lead to oscillatory behaviour. For this reason, the vector field model of the circuit is constructed and the non-existence of periodic solutions is verified with vector field simulations for the whole range of V_{DD} more than 500mV.

5.3.5 *Disappearance of periodic orbit*

The characterisation of the dynamics behind the disappearance of the periodic orbit as V_{DD} crosses a critical threshold is of major significance for the understanding of the circuit behaviour and besides theoretical value, it can also provide additional information leading to a better circuit design.

In this section, the two-stage ring oscillator is modelled as a dynamical system and the stability properties of the periodic attractor as the power supply approaches the critical value are investigated using the method in Chapter 3. Figure 56 shows the periodic orbits in a three-dimensional plot for static V_{DD} levels ranging from 450mV to 490mV. It should be noted that because of the simple transistor model and the modelling assumptions, the latch-up at 500mV occurs for a slightly different ratio r compared to SPICE simulations. However, as the main interest is the qualitative analysis of the phenomenon, the validity of the results is not affected.

The stability of the periodic orbits for the various V_{DD} levels is studied by calculating the values of the Floquet multipliers of the Monodromy matrix. In each case, one of the eigenvalues is equal

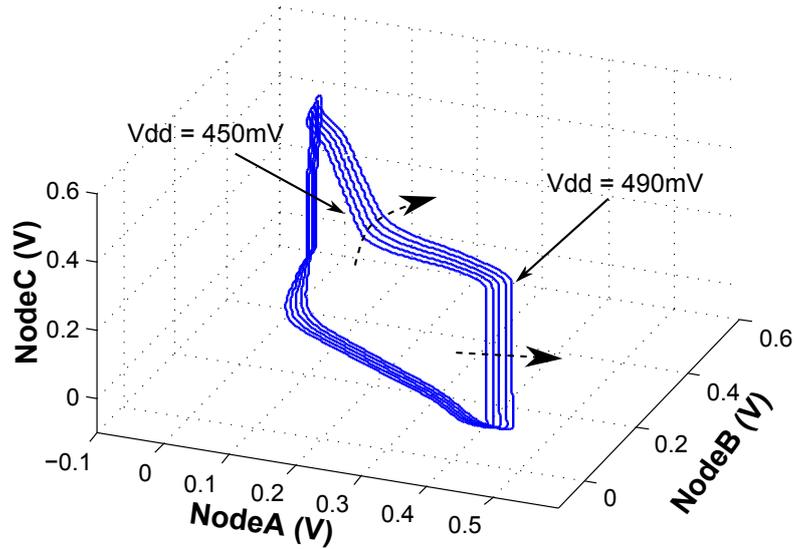


Figure 56: Periodic attractors for constant power supply, as V_{DD} level approaches the critical value of 500mV and the lock-up occurs.

to 1 due to the absence of external stimulus and the remaining three eigenvalues have values less than 10^{-15} . Thus, the analysis does not provide any evidence that the stability of the orbit is lost as a result of an eigenvalue crossing the unit circle.

In order to further explore the dynamics during the critical V_{DD} crossing, a set of three transient simulations is run using SPICE with the purpose of understanding how different solutions behave around the bifurcation point. Firstly, the V_{DD} is set to 490mV and periodic behaviour is observed. Secondly, the V_{DD} is perturbed to 500mV and two simulations are run with explicit initial conditions selected on the periodic orbit of the initial simulation. Figure 57 presents the superimposed results of the three simulation runs for the node voltages of the circuit. Dashed blue and red solutions correspond to simulation runs at 500mV, which lead to lock-up. It is interesting to observe how the solutions are attracted to the periodic attractor before they suddenly settle into a stationary state.

The results of the stability analysis along with the visual inspection of the SPICE simulation runs provide adequate information for the characterisation of the bifurcation as a saddle-node on an invariant curve. An illustration of the phenomenon in two dimensions is shown in Figure 58, where a stable periodic orbit transforms into a homoclinic loop of a saddle-node equilibrium state as the bifurcation parameter λ obtains a positive value. In plain words, the limit cycle in the state space of the circuit is always an invariant set but for V_{DD} larger than a critical value, it contains equilibria. Additionally, the non-monotonic behaviour of the oscillation frequency in Figure 53 is appropriately justified as in such bifurcations the period of the orbit increases before it becomes a homoclinic loop [82].

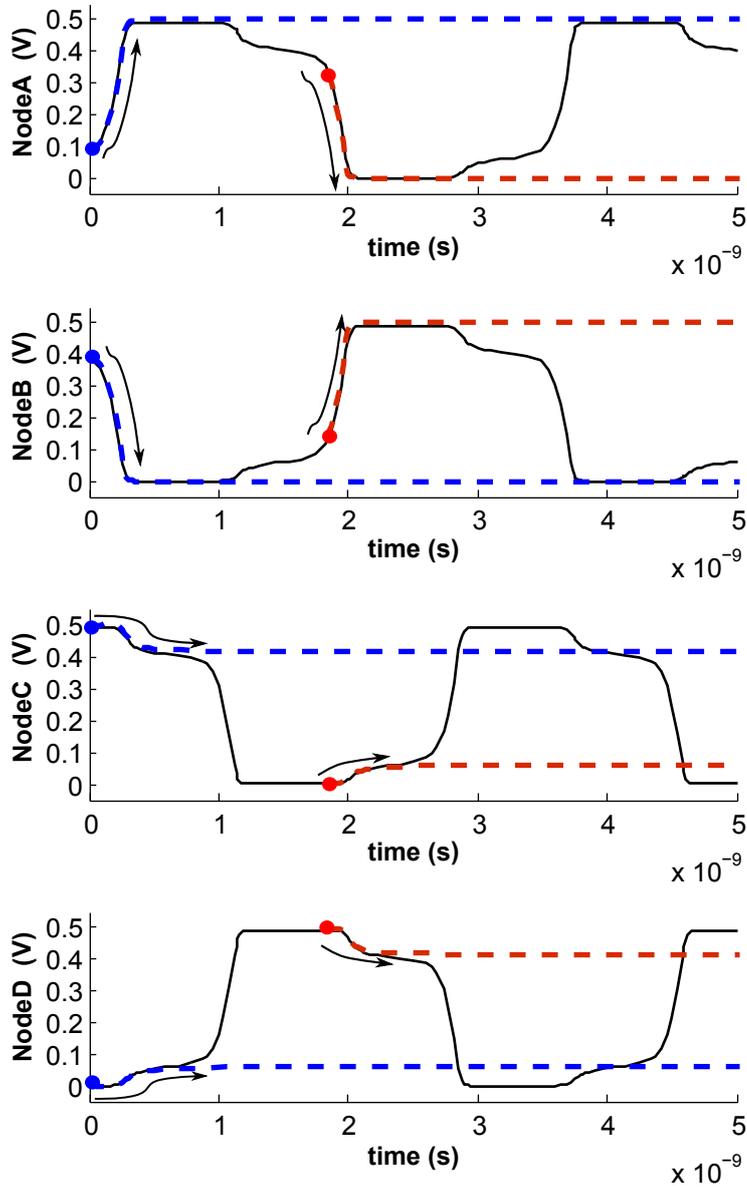


Figure 57: Superimposed SPICE simulation runs for $V_{DD} = 490\text{mV}$ (solid black) and $V_{DD} = 500\text{mV}$ (dashed blue and red) showing the attraction of the solutions to the periodic attractor before the latch-up occurs.

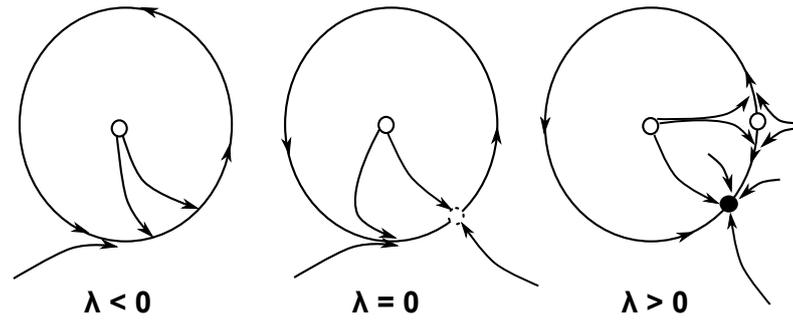


Figure 58: Two-dimensional illustration of how a stable periodic orbit ($\lambda < 0$) becomes a homoclinic loop of a saddle-node equilibrium state as the parameter λ crosses a critical value.

5.3.6 Control of detected voltage threshold during operation

The ability to selectively alter the predefined sensing threshold according to the specific requirements during operation is a feature which allows greater degree of flexibility in the integration of the sensor to monitoring solutions. Due to the transparent circuit design, this tuning capability can be easily implemented with minimum area overhead to the proposed sensor.

Figure 59 presents an alternate configuration for the detection of two different voltage levels. Each CC inverter in the circuit is connected in parallel to an additional tristate inverter and the operation of the extra inverter is controlled by an external signal E . When E is low, the tristate inverter is deactivated and the detected voltage level depends on the initial CC inverter. When E is high, the tristate inverter is active and can alter the detected voltage level. Effectively, by activating the tristate inverter, the ratio r can be manipulated as the strength of each CC block is increased.

The proposed configuration is verified by simulation. In Figure 60, two node voltages and the E control signal are plotted for operation under sinusoidal V_{DD} and ratio $r=5$. Initially, E is low and the tristate inverters are deactivated. The bifurcation that defines voltage threshold A occurs at 600mV. During latch-up, the E signal goes to high, thus changing the ratio r , and at the falling edge of V_{DD} the bifurcation that defines voltage threshold B occurs at 480mV.

The connection of extra transistors at the input and the output of the CC inverters adds additional capacitance to each node and alters the circuit dynamics even when the tristate inverters are deactivated. For this reason, despite the fact that the ratio $r=5$ yields a detected voltage level of 500mV without the additional inverters, the bifurcation point moves to 600mV when the tuning capability is added.

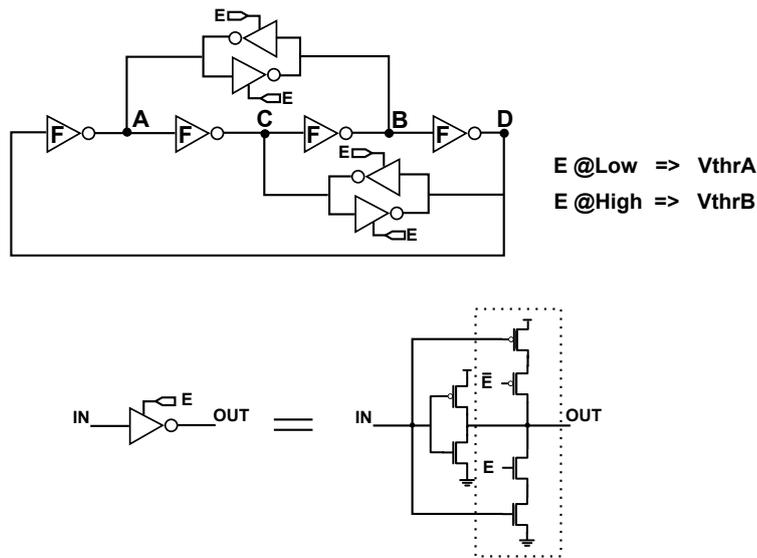


Figure 59: Alternative configuration with additional tristate inverters for the detection of two different voltage thresholds controlled by the E signal.

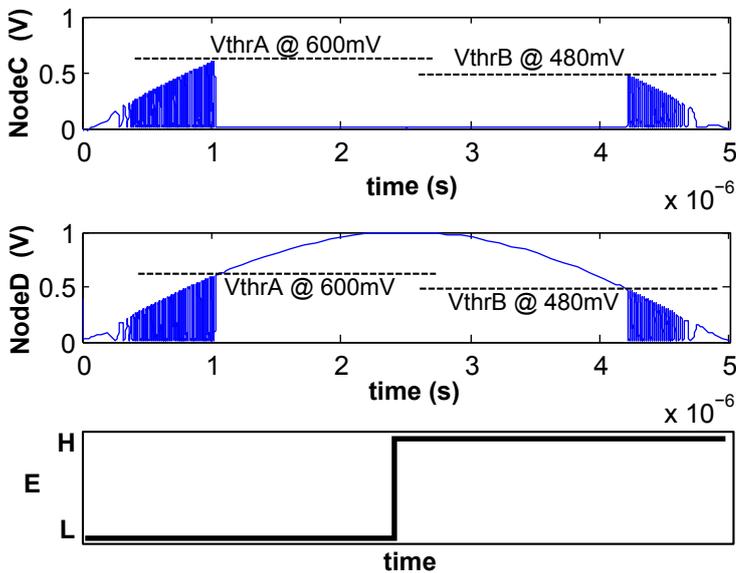


Figure 60: Simulation results showing the detected threshold levels A and B under sinusoidal supply voltage, with additional tristate inverters connected in parallel to each CC inverter. The tristate inverters are activated during latch-up and alter the detected voltage level at the falling edge of the supply voltage.

5.3.7 Process and temperature variations

The effect of process and temperature variations on the proposed sensor (with $r=5$) are investigated with a series of simulations across different corners and temperature values. Figure 61 shows the voltage of Node A under sinusoidal supply voltage for corners SS, FF, FN_{SP} and SN_{FP}. The maximum deviation from the detected voltage level of 500mV on the typical corner is 60mV for the FN_{SP} corner. The bottom plot of Figure 61 shows the dependence of the detected voltage level on the temperature for the nominal process parameters. The maximum deviation is 50mV for 75C.

Despite the fact that the reference voltage is not necessary and thus the detected voltage level is more prone to variability factors, these results show that the proposed sensor is a viable solution if the tolerance of a few tenths of mV is acceptable. Depending on the specific monitoring solution and calibration options, accurate digital tuning can be achieved by using a configuration similar to Figure 59 with appropriately sized tristate inverters digitally controlled by external activation signals.

5.4 SUMMARY AND CONCLUSIONS

In this chapter, a novel voltage sensing technique based on the ability of the ring oscillator to change operating modes under variable V_{DD} was developed. By sensing the onset of the oscillatory mode from a stationary latching behaviour and taking advantage of the inherent properties of the circuit, a reference-free preset threshold voltage detector was developed. Detailed analysis and verification using dynamical systems theory and SPICE simulations, along with an additional configuration for the control of the detected voltage during operation make the proposed sensor a viable solution for the integration in an on-chip voltage monitoring system.

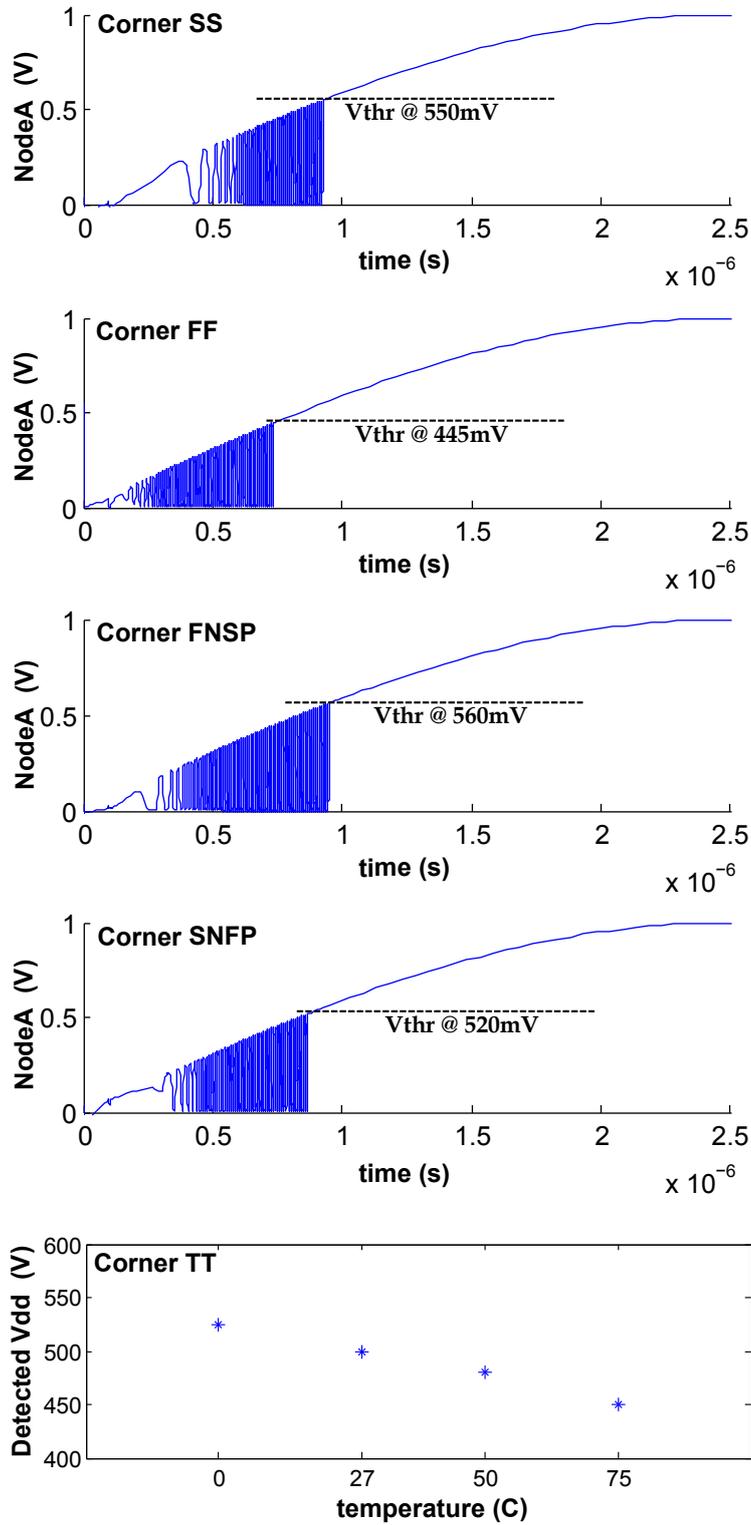


Figure 61: Corner and temperature simulations of proposed sensor for ratio r=5.

Recent advances in mixed signal integration considerably narrowed the gap between the formerly separate worlds of analog and digital design. Despite the major benefits gained by this co-existence, many new challenges have also emerged. Technology scaling to advanced process nodes imposed additional predicaments to the integration of analog components and to the design of mixed signal blocks in general. Existing verification techniques are highly inefficient in dealing with the increasing amount of design considerations and a novel verification framework consisting of straightforward flows, efficient methods and smart tools has to be developed for the analysis and verification of AMS designs.

This thesis investigated the potential benefits of a dynamical systems approach to the verification and analysis of CMOS circuits. The development of realistic dynamical models and the study of their behaviour using tools from dynamical systems theory served as the basis for this endeavour.

The remainder of this chapter recalls the main contributions of this thesis and presents open questions and directions for future research. An overall statement about the study concludes the thesis.

6.1 MAIN CONTRIBUTIONS

In Chapter 3, the construction of an ODE model of a circuit using KCL and a piecewise short channel transistor model is demonstrated. A method based on Floquet theory and Filippov solutions for the exploration of the stability properties of periodic attractors as a model parameter approaches a critical value is also developed using Matlab. The proposed method is applied to a toggle element with a variable input frequency and it successfully describes the period doubling bifurcation, commonly known as pulse swallowing in frequency dividers.

In Chapter 4, a flow for the automated characterisation of the structural properties of the state space in unconventional oscillators complements the set of proposed tools. The verification flow involves the exhaustive detection of EP using a SMT based method and a smart implementation of dynamical systems principles with any SPICE simulator. Additionally, the existence of periodic attractors is investigated on a vector field model of the state space using vector field simulations. The verification toolbox provides a solution to the complete mapping of the state space which can be used not only for the verification of the cor-

rect circuit operation but also for the exploration of novel applications of existing structures.

In Chapter 5, a voltage sensing technique based on the sensing of the onset of an oscillatory mode from stationary latching behaviour on a circuit which can change operating modes under variable supply voltage is developed. A circuit realisation of a reference-free and tunable threshold voltage detector is introduced using an autonomous even stage ring oscillator with inherent sensitivity to the power supply.

6.2 DIRECTIONS FOR FUTURE RESEARCH

The work presented in this thesis has exploited the benefits of treating CMOS circuits with a dynamical systems mindset. However, many questions are in need of further investigation and many opportunities for new studies have also emerged.

In Chapter 3, the algorithm for the stability analysis of periodic orbits can be optimised and used in the generation of a parameter space diagram for the evaluation of the stability region under parameter variations. This diagram may serve as an initial reference for the designer for the selection of parameter values within bounds not violating the predefined specifications. In addition, a number of caveats need to be noted regarding the verification flow of Chapter 4. The presented methodology is intended to be applied on circuit blocks with low number of nodes. Despite the straightforward implementation, the vector field generation method does not scale well with the node count. Although an adaptive state space sampling technique may provide increased capacity, formal analog verification methods such as reachability analysis [40] may be considered as an alternative option.

The implementation of the proposed sensing method in Chapter 5 is based on a specific even stage ring oscillator design. However, a wide variety of oscillators from the literature [83, 84, 85] may be analysed and a detailed comparison can elucidate the advantages of each design. In addition, although the dependence of the detected power supply threshold on the ratio r was demonstrated with simulations, an analytical model based on small signal parameters could also be developed. Moreover, the compact size of the proposed sensor facilitates the design of a built-in self-test without excessive area cost for better immunity to process and temperature variations. The study of potential implementations and the fabrication of a chip demonstrator would also be very valuable. Finally, further research may investigate in more depth the relation between the bifurcation phenomena in low dimension ODE models and the corresponding CMOS structures that can implement these functions, leading to a dynamical system based circuit synthesis approach [86].

6.3 CONCLUSION

Despite the establishment of AMS designs as a principal driver of the semiconductor industry, many open challenges in the AMS verification process need to be addressed. Traditional simulation techniques have evolved into a major bottleneck and alternative verification frameworks must be developed to effectively solve existing problems. This thesis has manifested the potential of dynamical systems theory as an active participant in the paradigm shift in CMOS circuit verification.

SIMULATION PARAMETER VALUES

A.1 CHAPTER 3

The parameter values for the simulations in Chapter 3 were chosen according to the BSIM4 transistor model for the 90nm technology node from UMC. This allowed for a comparison between the simulation results using each of the models. The channel length modulation effect λ which determines the angle of the saturation region for the simplified transistor model was selected using basic fitting. Additionally, the capacitors connected to each node were approximated in order to determine the actual time constants of the simulated circuits.

A.1.1 *Three-stage ring oscillator*

Common values for both pMOS and nMOS devices:

$$L = 80e-09m, W = 300e-09m, C_{OX} = 0.9e-02F/m^2, v_{sat} = 24e06m/s, \lambda = 0.4$$

For pMOS devices:

$$V_T = -0.35V, E_c = 24e6V/m, \mu_e = 70e-04m/Vs$$

For nMOS devices:

$$V_T = 0.35V, E_c = 6e6V/m, \mu_e = 270e-04m/Vs$$

Node capacitances:

$$C1, C2, C3 = 1e-15F$$

A.1.2 *Yuan and Svensson toggle element with variable input frequency*

Common values for both pMOS and nMOS devices:

$$L = 80e-09m, C_{OX} = 0.9e-02F/m^2, v_{sat} = 24e06m/s, \lambda = 0.4$$

For pMOS devices:

$$V_T = -0.35V, E_c = 24e6V/m, \mu_e = 70e-04m/Vs$$

For nMOS devices:

$$V_T = 0.35V, E_c = 6e6V/m, \mu_e = 270e-04m/Vs$$

Transistor widths and node capacitances:

$$W1, W2, W3 = 600e-09m, W1, W2, W3 = 1200e-09m, \\ C1 = 0.5e-15F, C2 = 2.5e-15F, C3 = 4e-15F, C4 = 1e-15F, \\ C5 = 5.5e-15F, C6 = 1e-15F$$

A.2 CHAPTER 4 AND CHAPTER 5

The 90nm technology node from UMC with the Spectre circuit simulator from Cadence was used for the simulations in chapter 4 and chapter 5. Unless otherwise stated, the transistor length is set to the minimum value (80nm) for this technology.

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