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Analysis and Design of Switched-Capacitor DC-DC Converters with Discrete Event Models

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Acronyms

SCDDC	Switched-Capacitor DC-DC Converter
SC-STG	Switched-Capacitor Signal Transition Graph
STG	Signal Transition Graph
LPN	Labelled Petri Nets
VCR	Voltage Conversion Ratio
LCD	Liquid-crystal Display
DRAM	Dynamic Random Access Memory
SSL	Slow Switching Limits
FSL	Fast Switching Limits
CSC	Complete State Coding
CAD	Compute-Aid Design

Abstract

Switched-capacitor DC-DC converters (SCDDCs) play a critical role in low power integrated systems. The analysis and design processes of an SCDDC impact the performance and power efficiency of the whole system. Conventionally, researchers carry out the analysis and design processes by viewing SCDDCs as analogue circuits. Analogue attributes of an SCDDC, such as the charge flow current or the equivalent output impedance, have been studied in considerable detail for performance enhancement. However, in most existing work, less attention is paid to the analysis of discrete events (e.g. digital signal transitions) and the relationships between discrete events in SCDDCs. These discrete events and the relationships between discrete events also affect the performance of SCDDCs. Certain negative effects of SCDDCs such as leakage current are introduced by unhealthy discrete states. For example, MOS devices in an SCDDC could conduct undesirably under certain combinations of signals, resulting in reversion losses (a type of leakage in SCDDCs). However, existing work only use verbal reasoning and waveform descriptions when studying these discrete events, which may cause confusion and result in an informal design process consisting of intuitive design and backed up merely by validation based on natural language discussions and simulations. There is therefore a need for formalised methods to describe and analyse these discrete events which may facilitate systematic design techniques.

This thesis presents a new method of analysing and designing SCDDCs using discrete event models. Discrete event models such as Petri nets and Signal Transition Graphs (STGs) are commonly used in asynchronous circuits to formally describe and analyse the relationships between discrete transitions. Modelling SCDDCs with discrete event models provides a formal way to describe the relations between discrete transitions in SCDDCs. These discrete event models can be used for analysis, verification and even design guidance for SCDDC design. The rich set of existing analysis methods and tools for discrete event models could be applied to SCDDCs, potentially improving the analysis and design flow for them. Moreover, since Petri nets and STGs are generally used to analyse and design asynchronous circuits, modelling and designing SCDDCs with STG models may additionally facilitate the incorporation of positive features of asynchronous circuits in SCDDCs (e.g. no clock skew).

In this thesis, the relations between discrete events in SCDDCs are formally described with SC-STG (an extended STG targeting multi-voltage systems, to which SCDDCs belong), which avoids the potential confusion due to natural language and waveform descriptions. Then the concurrency and causality relations described in SC-STG model are extended to Petri nets, with which the presence of reversion losses can be formally determined and verified. Finally, based on the STG and Petri net models, a new design method for reversion-loss-free SCDDCs is proposed. In SCDDCs designed with the new method, reversion losses are entirely removed by introducing asynchronous controls, synthesised with the help of a software synthesis toolkit “Workcraft”.

To demonstrate the analysis capabilities of the method, several cross-coupled voltage doublers (a type of SCDDC) are analysed and studied with discrete event models as examples in this thesis. To demonstrate the design capabilities of the method, a new reversion-loss-free cross-coupled voltage doubler is designed. The cross-coupled voltage doubler is widely used in low power integrated systems such as flash memories, LCD drivers and wireless energy harvesting systems. The proposed modelling method is potentially used in both research and industrial area of those applications for a formal and high-efficiency design process.

Acknowledgement

First of all, I would like to express my sincere gratitude to Prof. Alex Yakovlev for his patient guidance and consistent support throughout the duration of my study. His enthusiasm and attitude on research is admirable and has been a resource of inspiration for me.

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Last but not least, my deepest thanks are given to my parents for their unrequited love.

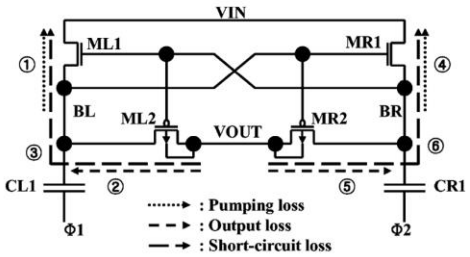
Chapter 1
Introduction

1.1 Motivations and objectives

Over the past few years, portable electronic devices such as smartphones and wearable devices have been proliferating in people's daily lives [1]. Portable devices such as smartphones are increasingly equipped with such components as face recognition modules, wireless charging modules, 5G communication modules, etc. [2]-[4]. As a portable device is typically powered by a battery with a fixed output (e.g. of 3.7V for smartphones) and the functional components are operated with different voltage supplies [5], DC-DC converters are utilised to convert the battery voltage into different supply voltages, ensuring that such components work in optimal modes. DC-DC converters play an essential role in these portable devices, and the performance of DC-DC converters impacts the device's battery life.

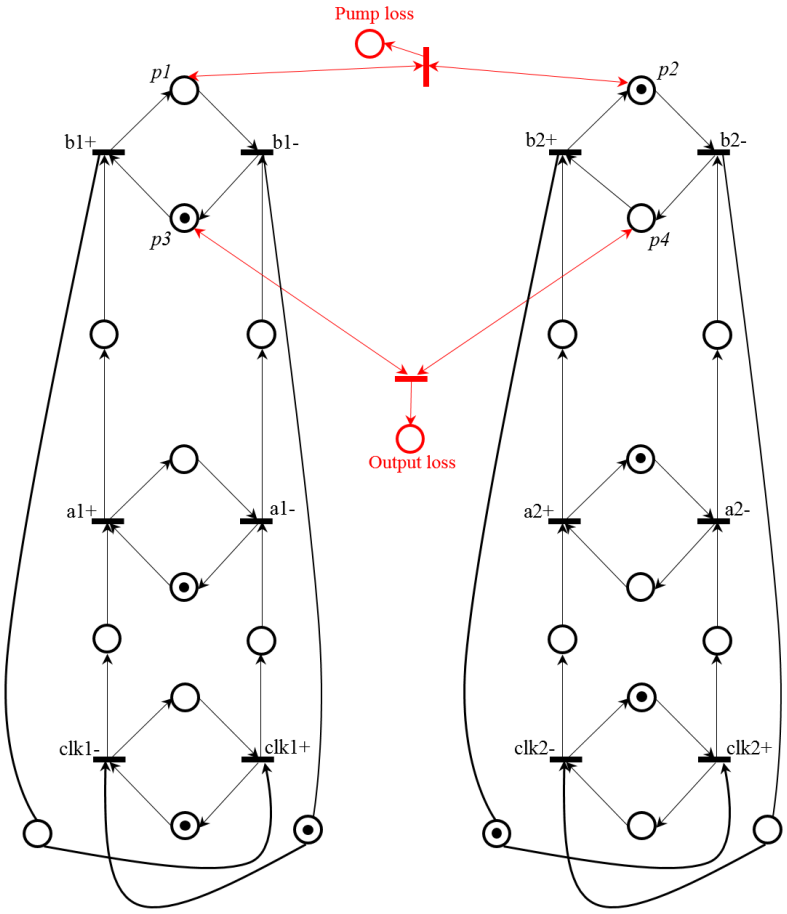
Switched-capacitor DC-DC Converters (SCDDC) are a subset of DC-DC converters, converting a voltage to another voltage with only switches and capacitors employed. Compared with the inductor based switched DC-DC converter, the SCDDC has advantages of small size and high-power density since the capacitor is more compatible with modern CMOS processes [6]. Although efforts have been made [7]-[9] to reduce the inductor size and to integrate the inductor on a chip, these usually require costly extra fabrication steps. The ease of integration has led to the extensive use of SCDDCs in low power technologies. The performance, especially power efficiency, of SCDDCs is therefore an important topic of study for low power integrated technologies [6].

In this charge pump, the timing relationship between Φ1 and Φ2 is very important for minimizing the reversion loss because the loss closely depends on both the relative timing between clock phases and the transition slope of each clock [6]. To investigate this aspect, Fig. 2 shows two possible timing relationships between these control clocks. When Φ1 and Φ2 are matched to each other [see Fig. 2(a)], there is no overlap between clock levels, and only the transition periods are briefly overlapped. In this case, overlapping transition period, $OV\_T_R(OV\_T_F)$, refers to the period in which a rising (falling) transition of Φ1 and a falling (rising) transition of Φ2 are overlapped to each other. When there is a timing mismatch between Φ1 and Φ2 [see Fig. 2(b)], there are intervals in which their high and low levels are overlapped. In this case, overlapping period, $OV\_H(OV\_L)$, refers to the period in which both clock phases are identically high (low) [5]. Under the matched timing condition shown in Fig. 2(a), the charge pump has reversion loss during each transition period. That is, during OV_T_R, the pumping loss occurs since a boosting action on BL starts before ML1 becomes fully OFF [see ① in Fig. 1]. The output loss also occurs because the precharge action on BR starts before MR2 becomes fully OFF (see ⑤). The short-circuit loss happens during the portion of the transition period in which ML1 and ML2 or MR1 and MR2 are simultaneously ON (see ③ and ⑥). The occurrence of reversion loss during OV_T_F is similar to the previous case. Under the mismatched timing condition shown in Fig. 2(b), the conventional charge pump has far larger amount of reversion loss during overlapping periods. During OV_L, BL driven by Φ1 goes low when ML2 is still ON. Then, some of the output charges are transferred to BL through ML2,



resulting in the output loss (see ②). The pull-down of BL also allows MR2 to turn on, resulting in additional output loss (see ⑤). The charge injected into BL and BR by these output losses causes a pull-up of both nodes, which makes ML1 and MR1 turn on. Then, some charges can flow directly through ML1–ML2 or MR1–MR2, resulting in the short-circuit loss (see ③ and ⑥). During OV_H, since BL goes high when ML1 is still ON, some of the charges stored in BL are transferred to the input supply node, resulting in the pumping loss (see ①). During the pull-up of BL, there is a period in which MR1 and MR2 are simultaneously ON, resulting in the short-circuit loss (see ⑥). In addition, since a high level on BL makes MR1 stay ON, the voltage of BR is somewhat lowered, turning ML2 on. Thus, short-circuit loss can happen during the period in which ML1 and ML2 are simultaneously ON (see ③).

(a) Language description of reversion losses



(b) Modelling reversion losses with Petri nets

Figure 1.1: Descriptions of reversion losses in a cross-coupled voltage doubler, (a) is from [40].

Traditionally, SCDDCs in are analysed and designed with modelling methods such as Charge Flow Analysis [10] and Output Impedance Analysis [11]-[13]. Charge Flow Analysis, studies the charges in a converter and can be used to estimate the equivalent output resistance based on the Output Impedance Analysis, with which an optimised working frequency or duty cycle can be obtained to improve the power conversion performance and power efficiency. Other modelling methods have also been proposed to help the analysis and design of SCDDC; [14] proposed a graph theory to predict the required number of capacitors for an SCDDC for any voltage conversion ratio; [15] and [16] modelled SCDDCs' output impedance with topology synthesis and [17] proposed a voltage-domain analysis that balances the trade-off between SCDDCs' properties for performance enhancement. However, these modelling methods focus more on the analogue attributes of SCDDCs and less attention is paid to discrete events (events that occur instantaneously, i.e. in discrete time, on signals that take discrete values, which are usually described using digital methods contrasted to continuous events which happen in continuous time on signals with continuous values and described using analogue methods) and the causality and concurrency relationships between discrete events, leading to the undernoted issues in the analysis and design of SCDDCs.

- There is no formal way to describe the causality and concurrency relations between the discrete events in SCDDCs. Existing literature titles typically describe the causalities of the signals in SCDDCs with natural language assisted by waveforms without any formal notations, researchers or engineers could potentially be confused about these relations in SCDDCs.

- There is no formal way to describe and verify certain negative effects, such as reversion loss, caused by discrete events in SCDDCs. Reversion losses are a type of leakage caused by undesirable conduction in MOS devices under certain combinations of signals. Without a formal method of modelling the discrete events and their relationships, works in the literature can only describe and analyse reversion losses with natural language intuition and waveforms, which also may cause confusion for researchers and engineers.

These problems become severe when an SCDDC gets larger in size and more complex in topology. Figure 1.1(a) shows descriptions of reversion losses that happen in a cross-

coupled voltage doubler [47] with dedicated combinations of internal signals. Although readers can understand what happened in the voltage doubler from the above descriptions, the descriptions are likely to cause confusion and inconvenience in case of the need for further analysis and verification.

At the same time, there are several SCDDC topologies that can achieve the same conversion rate with different charging and discharging principles. Behaviours such as signal transitions and charging/discharging processes in those SCDDCs are different, where the conventional intuitive descriptions for these also may cause a certain degree of confusion.

To formally describe and analyse those discrete events in SCDDCs, new modelling methods for SCDDCs based on discrete event models are proposed in this thesis. In this thesis, the main discrete event models adopted to model SCDDCs are Petri nets [19] and Signal Transition Graphs (STGs) [20]. The Petri net language was first introduced in the early 1960s, which has been used widely in the area of concurrent systems, distributed control systems, manufacturing, etc. [21]-[24]. STG is a particular version of Petri nets, which was initially introduced in [20], [25] to describe and formalise discrete events in asynchronous digital circuits. These discrete event models have been utilised to analyse and design DC-DC converters in some literature titles [26]-[30]. [26]-[28] propose a new design flow for a mixed-signal circuit based on STG and LPN (a type of extended Petri nets) where an example of an inductor based buck converter is designed with STG and LPN. [29] and [30] propose self-timed two-phase and multi-phase SCDDCs based on the STG model.

Based on these existing works, this thesis presents new modelling methods for SCDDCs in low power integrated systems by using discrete event models. With such modelling methods, the causality and concurrency relations between discrete events in SCDDCs can be formally described and reversion losses can be associated with certain events and therefore formally described and verified. Figure 1.1(b) shows the Petri net model that describes reversion losses in a cross-coupled voltage doubler, which is formal, simpler and more straightforward compared with the traditional descriptions in Figure 1.1(a). Most importantly, it can be used for analysis, verification and even design guidance for SCDDC designs such as cross-coupled voltage doublers. Moreover, modelling SCDDCs with discrete models will provide designers with a new perspective for SCDDC's analysis and design. Large sets of analysis methods and tools for discrete models could be applied to

SCDDCs, potentially improving the analysis and design flow for them. The automation tools for discrete event models such as Workcraft [71] may promote design efficiency for SCDDCs, especially for large-sized systems. In addition, since Petri nets and STGs are generally used to analyse and design asynchronous circuits, modelling and designing SCDDCs with STG models may additionally facilitate the incorporation of positive features of asynchronous circuits to SCDDCs. These include no global clock distribution & clock skew problems, low power and high speed. These features for asynchronous circuits will provide SCDDCs with extra benefits for power conversion performance and power efficiency.

1.1 Contributions

This thesis aims to present new modelling and design methods for SCDDCs in low power integrated systems with discrete event models. The following contributions have been made as a result of this research:

- A new modelling method that represents SCDDC with SC-STG (an extended STG) is proposed. With this new modelling method, the causality and concurrency relations between discrete events in SCDDCs can be described formally. A modified definition of multi-value transition enables analogue variation processes such as capacitor charging and discharging processes to be described with SC-STG. This method prevents the potential confusion in describing these relations with natural language and waveforms and facilitates the use of the rich set of tools available for SCDDC design and investigation.

- A new modelling approach that models reversion losses in SCDDCs with Petri nets is proposed. With the appropriate representation of events in SCDDCs with places and transitions, qualitative verification for reversion losses can be obtained by reachability analysis, by means of which all possible states of an SCDDC can be explored and investigated. Consequently, the related control scheme leading to a reversion loss can be detected and healthy controls that do not cause these events can be determined. In addition, the Petri net model also can be utilised to detect the reversion losses because of clock skew and clock jitter.

- A new reversion-loss-free SCDDC design method based on Petri nets and STGs is proposed. In this method, a healthy control scheme that avoids reversion losses can be determined at first based on the reachability analysis of the Petri net model. Then the healthy control scheme is modelled with STGs and the asynchronous control circuit producing such a control scheme can be obtained using tools such as Workcraft [71] and Petrify [72]. In the SCDDCs obtained with this new design method, there will be no reversion losses or clock mismatch problems (correct by the design). In addition, the new method is flexible, so that the obtained circuit synthesised by STG is able to produce control signals that are closed-loop with the target SCDDC.

- As a demonstration case study, a reversion-loss-free cross-coupled voltage doubler is obtained using the new design method. By using a formalised method and less design effort, the design achieves the same level of power efficiency as the best existing designs. This new cross-coupled voltage doubler example is a good demonstration for the validity of using the modelling methods presented in this thesis for SCDDCs.

1.2 Structure of the thesis

This thesis is organised as follows

- Chapter 1: This chapter briefly outlines the motivations and contributions of the thesis.

- Chapter 2: This chapter provides background information on SCDDCs and cross-coupled voltage doublers. It also introduces the basic definitions and properties of the Petri net model and the STG model. In addition, some existing modelling methods for SCDDCs are reviewed.

- Chapter 3: This chapter presents a new modelling method that models SCDDCs with SC-STGs. Examples of two different cross-coupled voltage doubler designs

are analysed with this new method. Subsequently, other SCDDCs with different topologies are also modelled with SC-STG.

- Chapter 4: This chapter presents a new modelling method that captures the reversion losses in SCDDCs with Petri nets. This concurrency and causality relations in Petri nets can be obtained from the SC-STG model. Several examples of existing cross-coupled voltage doubler designs are studied to demonstrate the modelling approach. Healthy control schemes that do not lead to reversion losses for these designs are determined and verified with reachability analysis of the Petri net models. In addition, further analysis of clock mismatch problems of these cross-coupled voltage doublers is also undertaken using the Petri net model.

- Chapter 5: This chapter presents a new design method for SCDDCs with Petri nets and STGs. This design method is extended from the Petri net model for reversion losses. A reversion-loss-free cross-coupled voltage doubler is designed with this new method in which reversion losses and timing mismatch problems are avoided. This new cross-coupled voltage doubler is implemented in UMC 65nm technology, and the analogue simulation results show high power efficiency and high performance.

- Chapter 6: This chapter summarises the modelling and design methods in this thesis. Possible areas for future work also are discussed.

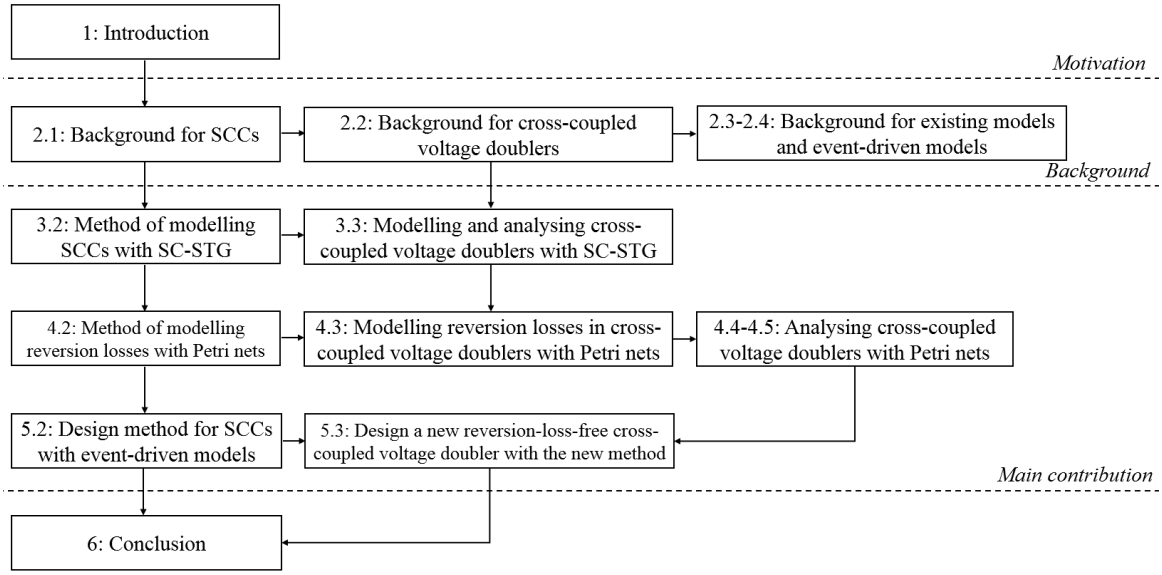


Figure 1.2: Main structure of the thesis.

Figure 1.2 depicts the relationships between the chapters. Apart from the modelling methods proposed, other critical contents of this thesis include analysing different cross-coupled voltage doublers with discrete event models and finally designing a new cross-coupled voltage doubler with discrete event models.

1.3 Publications

The following is a list of publications and paper(s) to be submitted for review as a result of this research work.

- D. Li, D. Shang, F. Xia and A. Yakovlev, "Modelling Switched-Capacitor DC-DC Converters with Signal Transition Graphs," *2018 15th International Conference on Synthesis, Modelling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD)*, Prague.
- D. Li, F. Xia, J. Luo and A. Yakovlev, " Modelling Reversion Loss and Shoot-through Current in Switched-Capacitor DC-DC Converters with Petri Nets," *2019 29th International Workshop on Power and Timing Modelling, Optimisation and Simulation (PATMOS)*, Rhodes.
- D. Li, F. Xia, D. Shang, J. Luo and A. Yakovlev, "Analyse and Design Reversion-loss-free Switched-Capacitor DC-DC Converters with Petri Nets," Journal paper (ready to submit).

Chapter 2
Background

The primary background information for this thesis is introduced in this chapter, which includes:

- SCDDCs
- Cross-coupled voltage doublers
- Existing modelling methods for SCDDCs
- Discrete event models

Basic knowledge of SCDDCs related to this thesis, including definition, topologies and reversion losses, is introduced in Section 2.1. Several cross-coupled voltage doublers, which are a specific type of SCDDCs and which are modelled and analysed with discrete event models in the following chapters, are preliminarily introduced and analysed in Section 2.2. Existing modelling methods for SCDDCs are reviewed in Section 2.3. Finally, an overview of discrete event models including Petri nets and STG, tools for discrete event models and asynchronous circuit design flow with discrete event models is provided in Section 2.4. Sections 2.1 – 2.3 pertain to the baseline of this research and Section 2.4 presents the modelling techniques used in this research.

2.1 Switched-capacitor DC-DC converters

2.1.1 Definition

A DC-DC converter is a power converter with a feature of converting a DC voltage at the input terminal to a different DC voltage at the output terminal [31]. Generally, there are three types of DC-DC converters in low power systems, including inductive, capacitive and inductive-capacitive DC-DC converters [32]. SCDDCs are capacitive DC-DC converters whose voltage-conversion activities rely only on switches and capacitors.

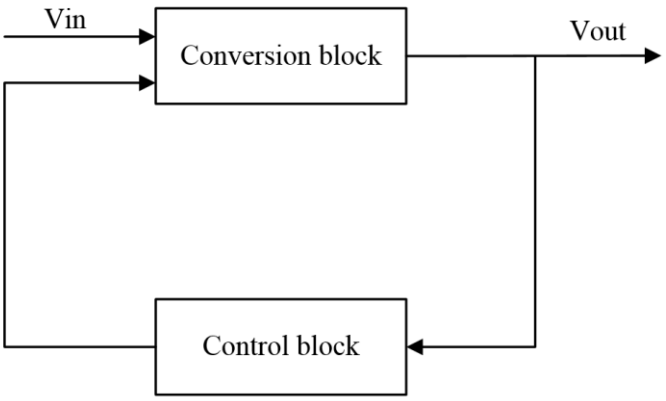
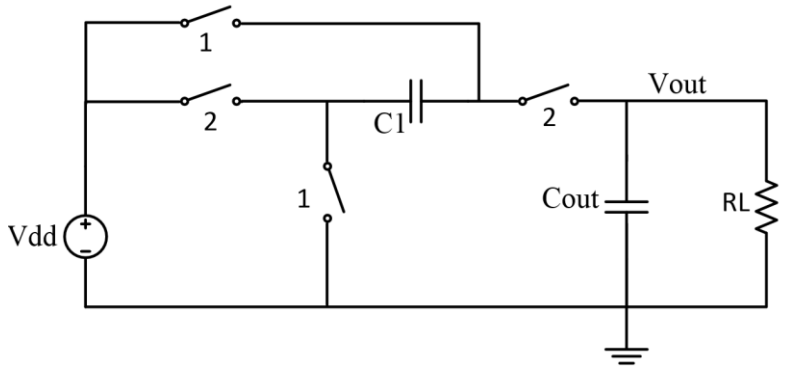


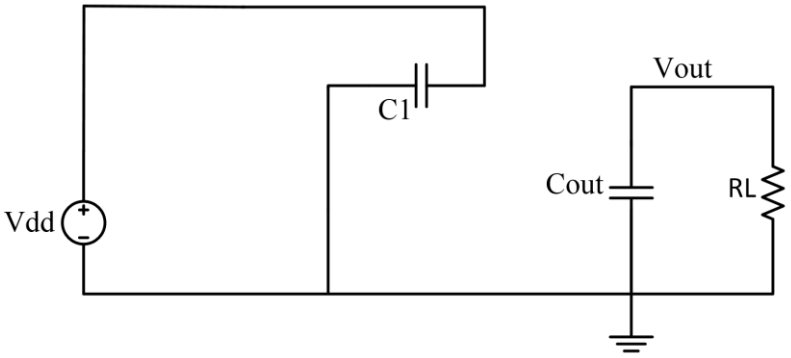
Figure 2.1: General structure for SCDDCs.

As shown in Figure 2.1, an SCDDC circuit includes a conversion block and a control block. The conversion block consists of switches and capacitors that implement the actual voltage conversion, whereas the control block manipulates events in the conversion block such as turning on and turning off switches based on the system requirements. The conversion block includes only switches and capacitors. Generally, control signals are clock signals, which control one or more switches in the conversion blocks. In an integrated SCDDC system, switches are realised by NMOS or PMOS devices. The capacitor employed in the conversion block to transfer the energy is called flying capacitor [32]. The word ‘flying’ denotes that neither of its two terminals is fixed at a specific voltage.

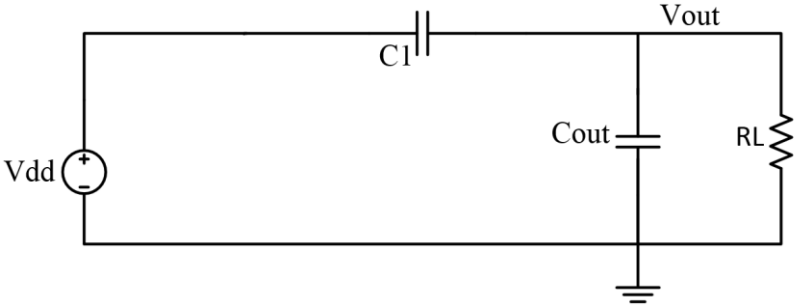
Each switching period of switches may be divided into several phases. With individual switches turned on and off in different phases, the conversion block can be configured into different SCDDC sub-nets. An SCDDC might implement two or more SCDDC sub-nets in different phases. Figure 2.2(a) shows a voltage doubler, which is configured into two different sub-nets during two phases.



(a) Voltage doubler



(b) Sub-net in the first phase



(c) Subnet in the second phase

Figure 2.2: Basic voltage doubler and its sub-nets.

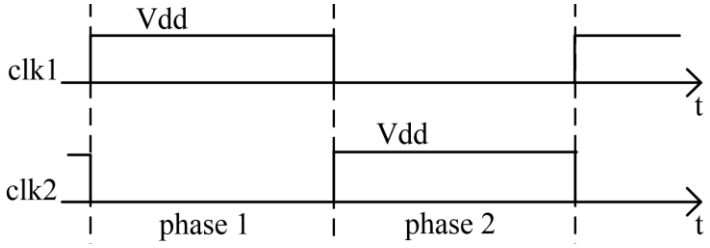


Figure 2.3: Control signals (Clock signals).

This voltage doubler consists of a flying capacitor C1 and four switches. This voltage doubler is controlled by control signals shown in Figure 2.3, Switches marked 1 are controlled by clock signal *clk1*, while switches marked 2 are controlled by *clk2*. The voltage input Vin is connected to a voltage source Vdd (Vin in all example SCDDCs in this thesis is connected to Vdd). This voltage doubler is configured into two sub-nets in two phases. In the first phase, switches marked 1 are turned on and switches marked 2 are turned off. The sub-net of the voltage doubler is shown in Figure 2.2(b). In this phase, capacitor C1 is charged to Vdd. In the second phase, with switches marked 2 turned on and switches marked 1 turned off, the voltage doubler is configured into a sub-net, as shown in Figure 2.2(c). In this phase, as C1 was charged to Vdd in the previous phase, the output voltage gets boosted to 2Vdd. According to [54], two nodes are capacitor coupling if they are connected with a capacitor, where a sudden change of voltage at one will cause a sudden change of voltage at the other. In this thesis, the voltage boost because of a pre-charged capacitor is called *capacitor coupling effect*.

The voltage doubler achieves a voltage output of 2Vdd with an input of Vdd. Therefore, the Voltage Conversion Ratio (VCR) for the voltage doubler is 2. The VCR of an SCDDC is defined as:

$$VCR = \frac{V_{out}}{V_{in}}$$

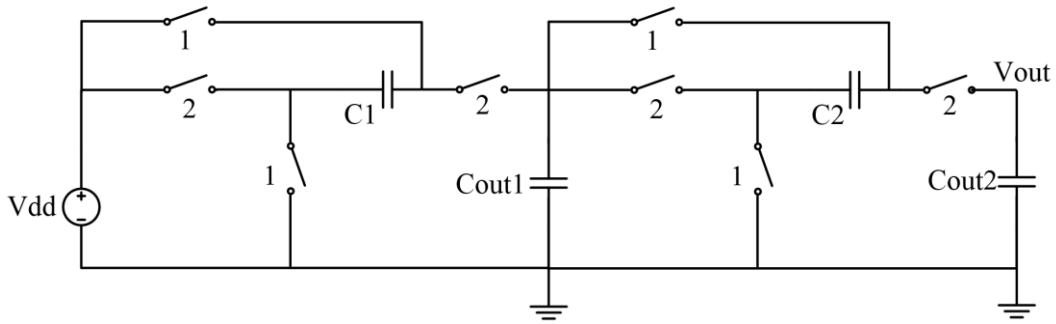
where V_{out} is the output voltage of an SCDDC and V_{in} is the input voltage of an SCDDC.

An SCDDC with VCR larger than 1 is called a step-up converter while the step-down converter has a VCR smaller than 1. Different VCRs can be achieved by different topologies which correspond to different configurations of switches and capacitors. Step-up converters can be implemented by topologies such as Ladder [33], Fibonacci multiplier [34], Parallel-Series Converter [35] and Multi-stage converter [36]. The step-down converter can be implemented by topologies such as Fractional Converter [37], Series-Parallel Converter [38] and Ladder [33].

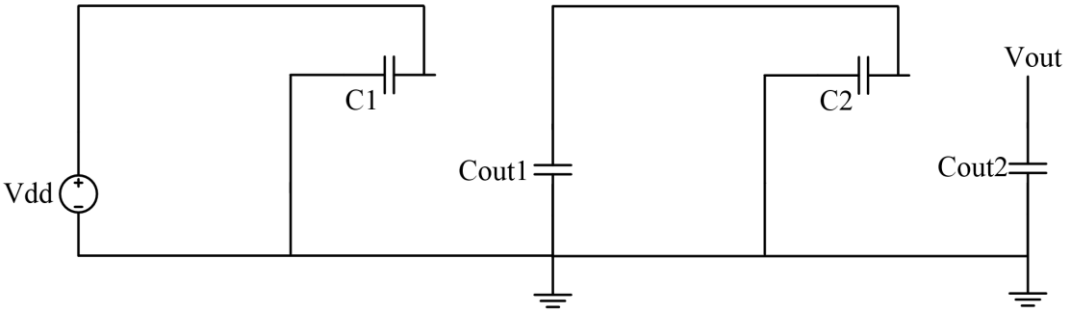
All SCDDC examples analysed in this thesis are step-up converters for low power integrated systems. These SCDDCs are widely used in flash memories [32], LCD panels [33] and wireless energy harvesting systems [52].

2.1.2 Topologies of SCDDCs

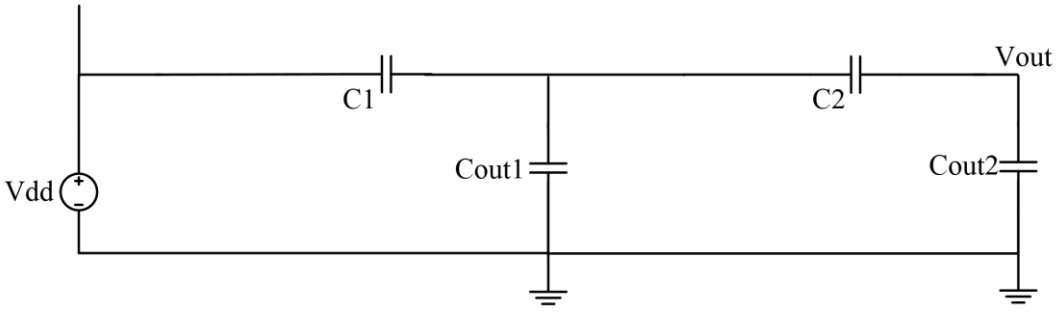
For SCDDCs, different VCRs can be achieved by different topologies. In this subsection, several topologies of step-up converters are introduced, which are then modelled and analysed in Chapter 3. All these SCDDCs are two-phase and controlled by two inverted clock signals, which are similar to the control signals shown in Figure 2.3. At the same time, switches marked 1 are controlled by *clk1* and switches marked 2 are controlled by *clk2*.



(a) Two-stage voltage doubler



(b) Sub-net in the first phase



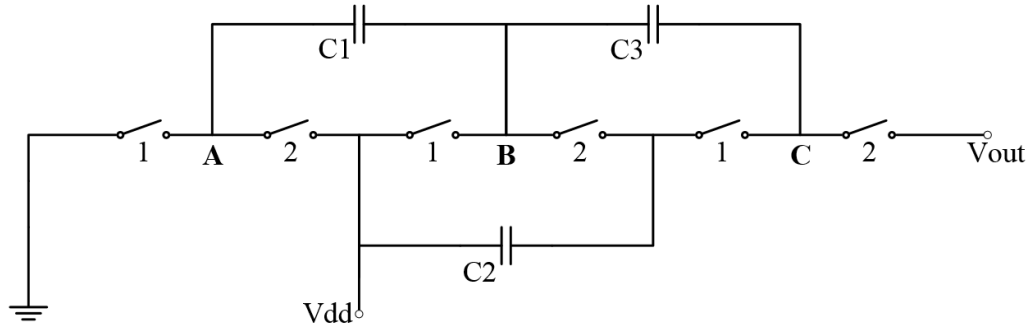
(c) Sub-net in the second phase

Figure 2.4: Two-stage voltage doubler and its sub-nets.

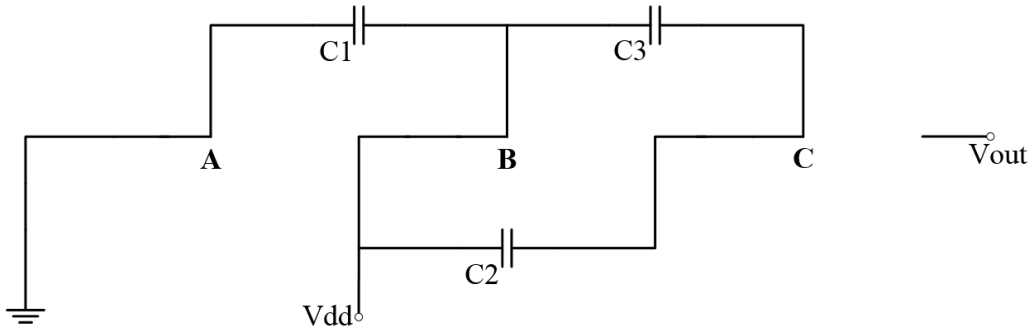
The SCDDC shown in Figure 2.4(a) is a step-up converter. It is a two-stage voltage doubler where the output of the first stage acts as an input for the second stage, achieving a VCR

of 4. The clock signals for this two-stage voltage doubler are shown in Figure 2.3, which are also control signals for other SCDDCs in this subsection.

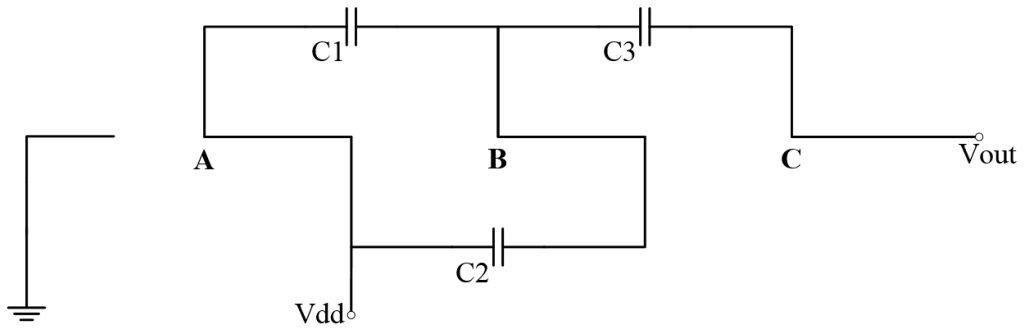
Like the voltage doubler shown in Subsection 2.1.1, the two-stage converter also has two phases. In the first phase, the converter is configured into the sub-net shown in Figure 2.4(b) and in the second phase it is configured into the sub-net shown in Figure 2.4(c). In the first phase, C1 and C2 are charged to Vdd and 2Vdd respectively. Then the output of the converter goes to 4Vdd in the second phase due to a capacitor coupling effect. Obviously, with the number of stages increased, the output voltage increases. For a k-stage doubler-type SCDDC, the VCR can be expressed as 2^k.



(a) Ladder



(b) Sub-net in the first phase



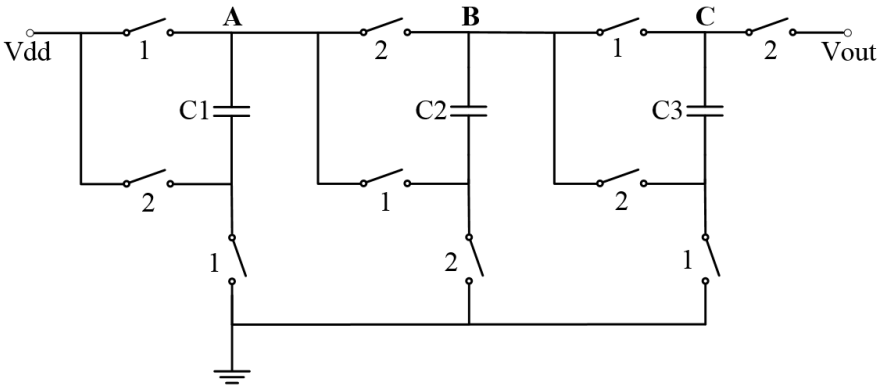
(c) Sub-net in the second phase

Figure 2.5: Ladder and its sub-nets.

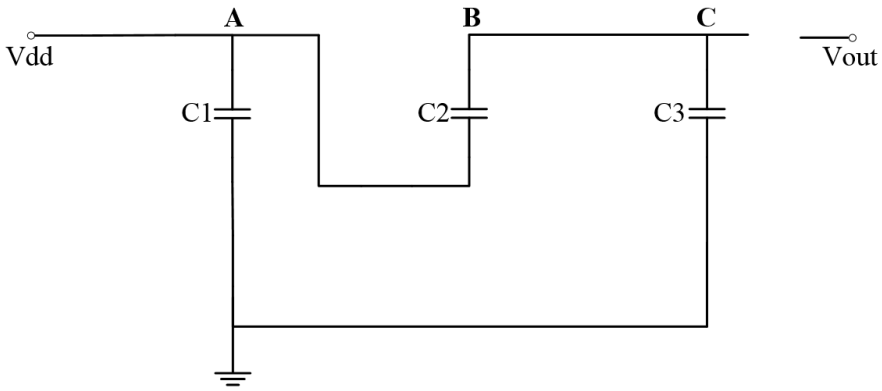
Figure 2.5(a) shows an SCDDC with a Ladder-type topology. This type of SCDDC can implement both step-up and step-down conversion. The ladder shown above is a step-up version, achieving a VCR of 3. For the step-up Ladder, the VCR equals to the number of flying capacitors.

This Ladder is controlled by two clock signals *clk1* and *clk2* as shown in Figure 2.3. In the first phase, switches controlled by *clk1* are turned on and switches controlled by *clk2* are turned off, and the Ladder circuit is configured into a sub-net as shown in Figure 2.5(b). The voltages at nodes *A* and *B* are 0 and Vdd, since they are connected to ground and Vdd respectively. As a result, C1 is charged to Vdd. Since C2 was charged to Vdd previously, the voltage at node *C* is 2Vdd, which charges C3 to Vdd. In the second phase, as switches controlled by *clk1* are turned off and switches controlled by *clk2* are turned on, the Ladder circuit is configured into a sub-net as shown in Figure 2.5(c). As in the previous phase, C1 and C3 were charged to Vdd, the voltages at node *B* and *C* are 2Vdd and 3Vdd respectively. Finally, the output voltage of the Ladder is 3Vdd.

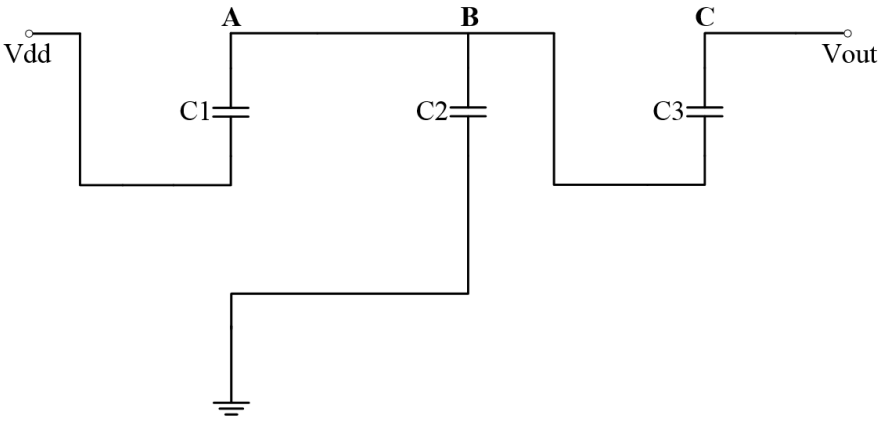
Figure 2.6(a) shows an SCDDC with a Fibonacci topology. A Fibonacci multiplier with n capacitors has a VCR of F_{n+2}, where F_{n+2} represents the $(n+2)^{th}$ Fibonacci number. Fibonacci series is a set of numbers $1, 1, 2, 3, 5, \dots, F_{n-1}, F_n, F_{n+1}$, where $F_{n+1} = F_n + F_{n-1}$ and the value of the next number is the sum of the previous two numbers. Therefore, the three-capacitor Fibonacci multiplier shown above has a VCR of 5. A Fibonacci converter has the highest VCR for a given number of flying capacitors, among all two-phase topologies [11].



(a) Fibonacci multiplier



(b) Sub-net in the first phase



(c) Sub-net in the second phase

Figure 2.6: Fibonacci multiplier and its sub-nets.

This Fibonacci multiplier is also controlled by clock signals *clk1* and *clk2* shown in Figure 2.3. In the first phase, the converter is configured into a sub-net shown in Figure 2.6(b), since switches controlled by *clk1* are on and switches controlled by *clk2* are off. The node *A* is connected to Vdd, charging C1 to Vdd. As C2 was charged to 2Vdd previously, the voltages at node *B* and *C* are both 3Vdd. As a result, C3 is charged to 3Vdd. In the second

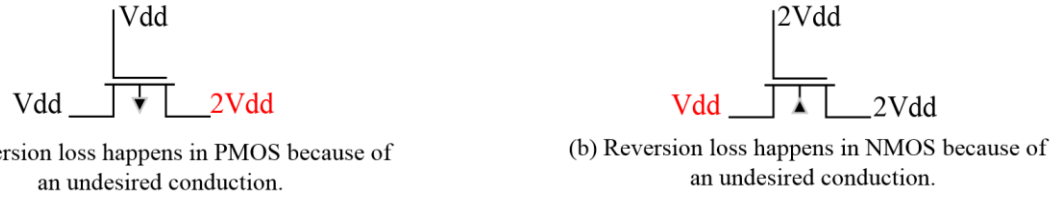
phase, the converter is configured into a sub-net shown in Figure 2.6(c). Because C1 and C3 were charged to Vdd and 3Vdd in the previous phase, the voltages at nodes *A*, *B* and *C* are 2Vdd, 2Vdd and 5Vdd respectively. As a result, the output voltage for this Fibonacci multiplier is 5Vdd.

The two-stage voltage doubler employs two flying capacitors while both the Ladder and Fibonacci multiplier employ three flying capacitors. Their VCRs are different; the Ladder has the lowest VCR of 3, the VCR of the two-stage doubler is 4 and the Fibonacci Multiplier has the highest VCR of 5. Because of the different topology configurations, the charging and discharging events among these converters are different. It is important to study why and how the VCRs of these converters have changed. Modelling these charging and discharging behaviours with discrete event models potentially helps us to do this analysis systematically, while the conventional methods presented here rely on verbal reasoning or other types of description that may cause confusion.

2.1.3 Reversion losses

NMOS or PMOS devices are used as switches in an integrated SCDDC. However, the utilisation of MOS devices may bring about reversion losses in an SCDDC, leading to undesirable power and energy loss.

Reversion loss [39], which is also known as undesired charge loss or undesired charge transfer, is generated in an SCDDC with NMOS or PMOS switches under certain signal combinations. Three types of reversion loss happen on MOS switches, as introduced below.



(a) Reversion loss happens in PMOS because of an undesired conduction.

(b) Reversion loss happens in NMOS because of an undesired conduction.

Figure 2.7: Reversion loss in PMOS and NMOS.

For a PMOS switch as shown in Figure 2.7(a), when the gate and source terminals are connected to Vdd, it is on a turned-off state for a typical circuit whatever the drain terminal is connected to 0 or Vdd. However, in an SCDDC, the drain terminal of the PMOS switch may be connected to a voltage larger than Vdd, e. g. 2Vdd (Vdd > Vth). Consequently, this PMOS switch is conducting undesirably, causing a reversion loss from the output to the source terminal.

For an NMOS switch as shown in Figure 2.7(b), a reversion loss appears when the gate and drain terminals are connected to a voltage larger than Vdd, e.g. 2Vdd (Vdd > Vth), while the source terminal is connected to the voltage source of Vdd.

In an SCDDC, when such undesired conductions happen, undesired charges may flow back from the load to the flying capacitor, or from the flying capacitor to the power supply. In principle, the energy flow through an SCDDC should be from the energy source to the SCDDC, then from the SCDDC to the load. If energy flows in the opposite direction, e.g. from the load back to the SCDDC or directly to the source, or from the SCDDC to the source, a reversion loss event happens. A reversal of the energy flow reduces the efficiency of the SCDDC and causes its output voltage to drop. As a result these types of events are known as energy and power 'losses'. In other words, energy/power that has already been delivered in the forward direction flows backwords and is 'lost' from the point of view of the load or SCDDC.

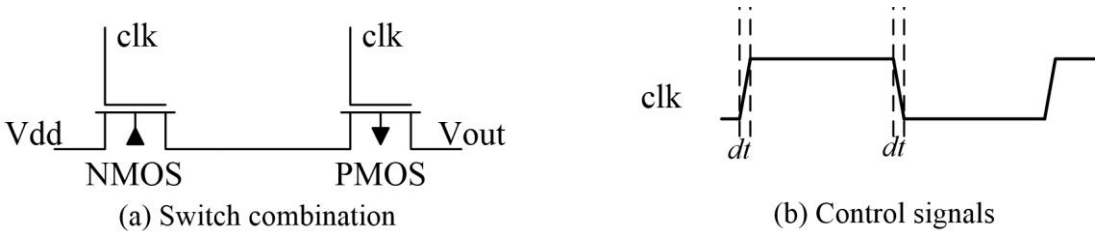


Figure 2.8: Shoot-through current.

Shoot-through current is also conventionally viewed as a type of reversion loss in an SCDDC [40]-[50], even though strictly speaking this is only partially the case. This thesis takes this convention and regards shoot-through current as a type of reversion loss. The effect of shoot-through current is the same as other types of reversion losses, i.e. reduced energy efficiency and output voltage drops.

For example, in the MOS switch combination as shown in Figure 2.8(a) controlled by *clk* shown in Figure 2.8(b), shoot-through currents may happen from the output Vout to the voltage source Vdd if Vout > Vdd. When *clk* is in transition, because this transition does not happen instantaneously and there may be a time interval *dt* when both the NMOS and PMOS switches are conducting simultaneously, causing a charge from Vout to Vdd [45]. Shoot-through current in voltage doubler designs occurs from Vout (2Vdd) to Vdd rather than from Vdd to the ground in conventional circuits such as an inverter. Therefore, one part of the energy loss of shoot-through current is lost due to the reverse charge and the rest is lost locally that is similar as in conventional circuits.

Above all, MOS switches in SCDDCs are all gated by control signals or connected to the internal node in an SCDDC, so that the generation of these reversion losses are corresponding to the control signals and the voltage at the internal nodes. Chapter 4 presents the model and analysis of these reversion losses in SCDDCs with the help of Petri net models.

Since reversion losses are associated with combinations of certain signal combinations in SCDDCs, the usual method of eliminating them is to remove these signal combinations and then test again for the existence of reversion losses.

2.2 Cross-coupled voltage doubler examples

Four cross-coupled voltage doublers are reviewed in this section. These voltage doublers are analysed using discrete event models such as extended STG model and Petri net model in Chapter 3 and Chapter 4. Based on these modelling works with discrete event models, a new design method and a new design of cross-coupled voltage doubler are presented in Chapter 5.

2.2.1 Structure of the cross-coupled voltage doubler

The cross-coupled voltage doubler is a common type of SCDDC, which is also named cross-coupled charge pump [40]. Compared with conventional MOS-device SCDDCs, the cross-coupled voltage doubler has advantages of higher output value and lower output ripple [18]. These features make it widely used in on-chip applications such as mixed-signal integrated systems [18], LCD drivers [41], DRAMs [45], ultrasonic transducer drivers [47] and wireless energy harvesting systems [52]. The schematic of a typical integrated cross-coupled voltage doubler is shown in Figure 2.9, referring as Voltage Doubler 1 in this thesis.

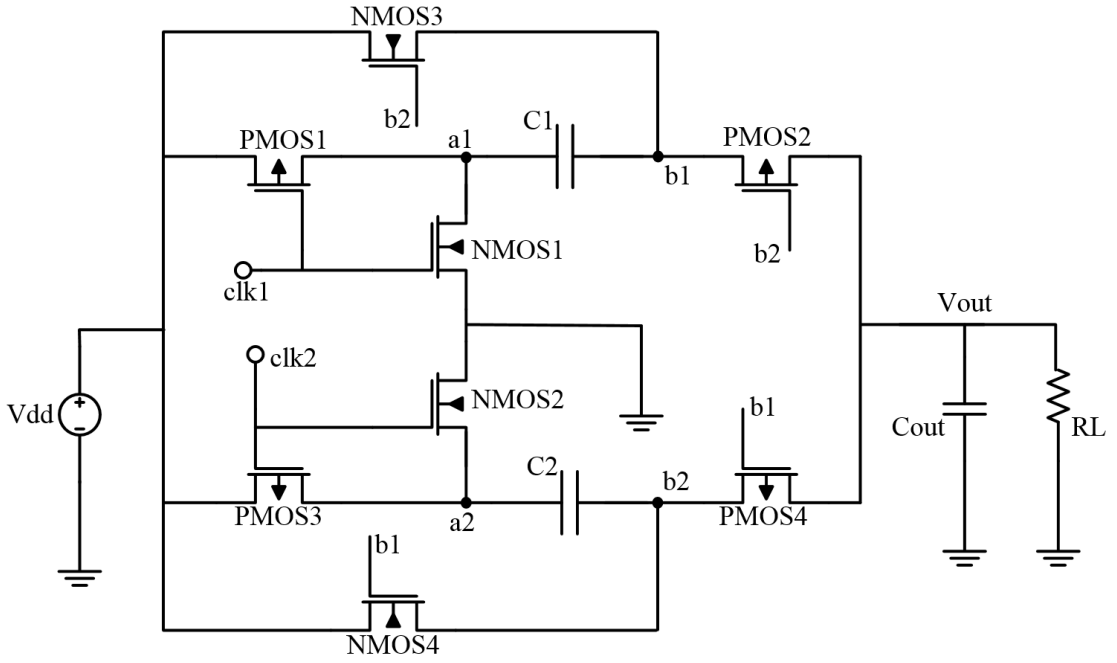


Figure 2.9: Cross-coupled voltage doubler, adapted from [18].

Voltage Doubler 1 includes two MOS-switch versions of the voltage doubler shown in Figure 2.2, with cross-coupled signals and MOS switch devices. Switches PMOS1, PMOS2, NMOS1, NMOS3 and flying capacitor C1 constitute the first voltage doubler while the second consists of PMOS3, PMOS4, NMOS2, NMOS4 and the flying capacitor C2. These two voltage doublers have a common input signal Vdd and output capacitor Cout. The MOS switch pair PMOS2 and PMOS4 is cross-coupled that each one is controlled by an internal signal from the other [53]. Also, NMOS3 is cross-coupled to the NMOS4. A simulated waveform of this voltage doubler is shown in Figure 2.10, where it is controlled by inverted control signals *clk1* and *clk2* (similar to controls shown in Figure 2.3).

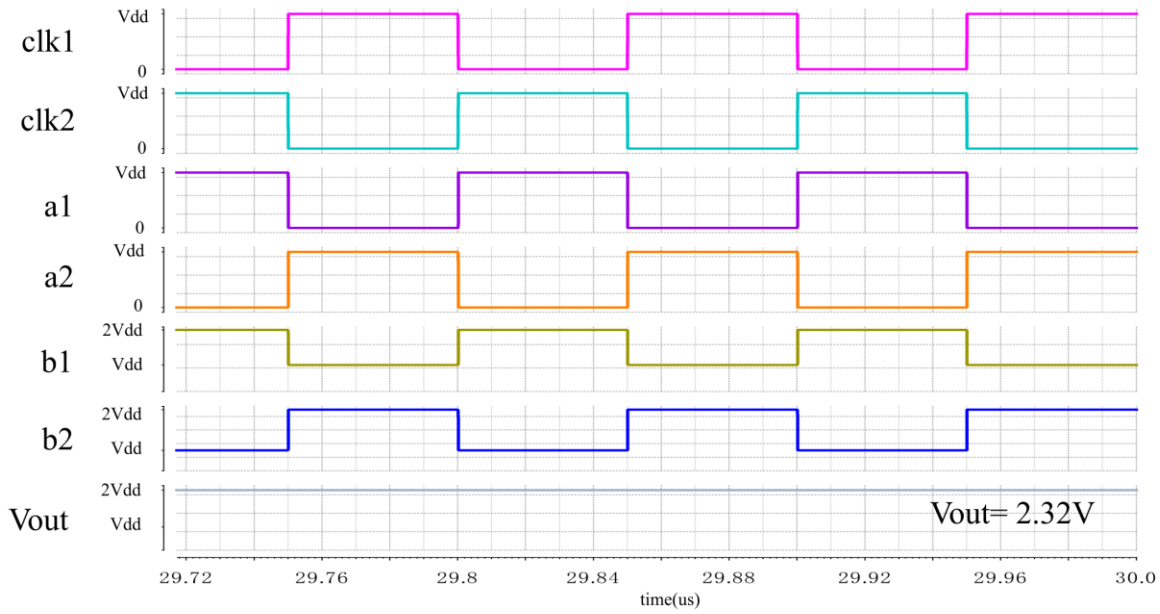


Figure 2.10: Simulation result of Voltage Doubler 1.

In the phase that *clk1*= Vdd, *clk2*= 0, NMOS1 is turned on and PMOS1 is turned off, making the internal node *a1* 0V. Meanwhile, the voltage at the node *a2* is Vdd since switch PMOS3 is on and NMOS2 is off, boosting the voltage at the node *b2* up to 2Vdd due to a capacitor coupling effect, as the flying capacitor C2 was charged to Vdd in the previous phase. Subsequently, switch NMOS3 that was controlled by the *b2* is turned on. As a result, the flying capacitor C1 is charged to Vdd in this phase through NMOS1 and NMOS3, which will bring *b1* up to 2Vdd in the next phase. At the same time, switch PMOS4 is turned on as *b1* is Vdd and *b2* is 2Vdd, charging the output to 2Vdd. In the next phase that *clk1*= 0, *clk2*= Vdd, the flying capacitor C2 is charged to Vdd and the output is charged to 2Vdd in a similar way. In other words, the output Vout is connected to either *b1* or *b2*, whichever is 2Vdd in any particular phase.

Compared with a single voltage doubler shown in Figure 2.2, the charging and discharging period of the flying capacitors is reduced by half, which indeed leads to a decrease of almost half of the output voltage ripple. At the same time, because each cross-coupled MOS switch is controlled by a signal from the other branch instead of its own source terminal, the turn-on voltage drop is reduced to a small drain-to-source voltage that is much smaller than the threshold voltage of Vth. Consequently, the output voltage of Voltage Doubler 1 is higher than the output voltages of other conventional MOS voltage doubler designs. Notably, there are a couple of internal signals including *a1*, *a2*, *b1*, *b2* in Voltage Doubler 1, which affect

the turn-on and turn-off state of MOS switches and the charging and discharging of flying capacitors.

2.2.2 Reversion losses in a cross-coupled voltage doubler

There are reversion-loss problems in cross-coupled voltage doublers. The reversion loss in Voltage Doubler 1 appears due to overlapped clock signals or clock signals with timing mismatches [18]. This subsection describes two types of reversion loss in Voltage Doubler 1 because of overlapped clock signals.

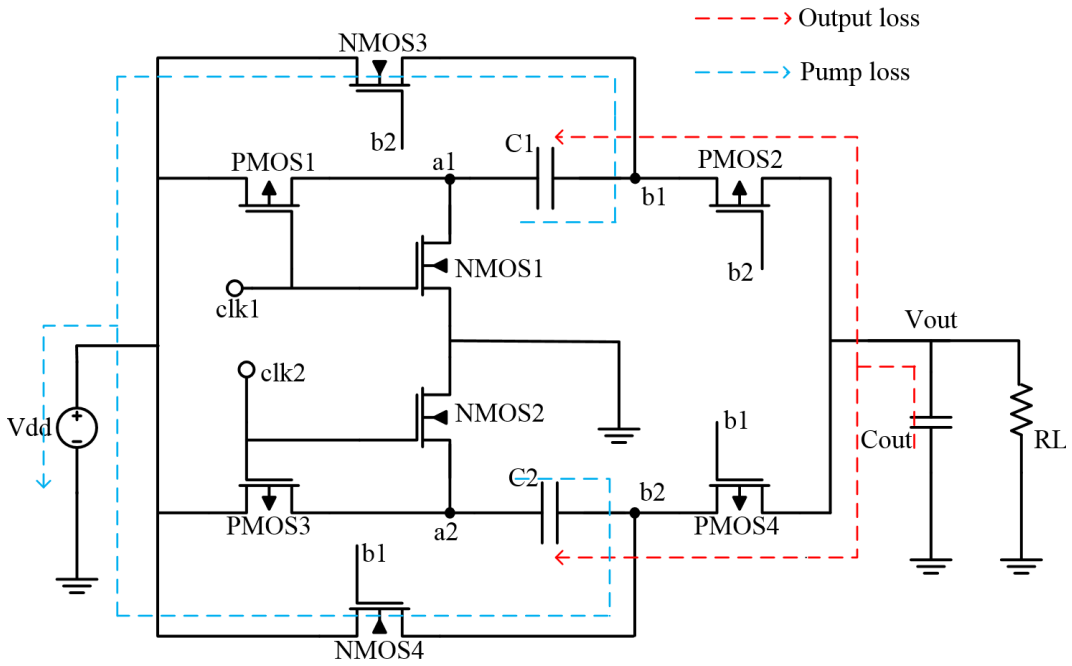
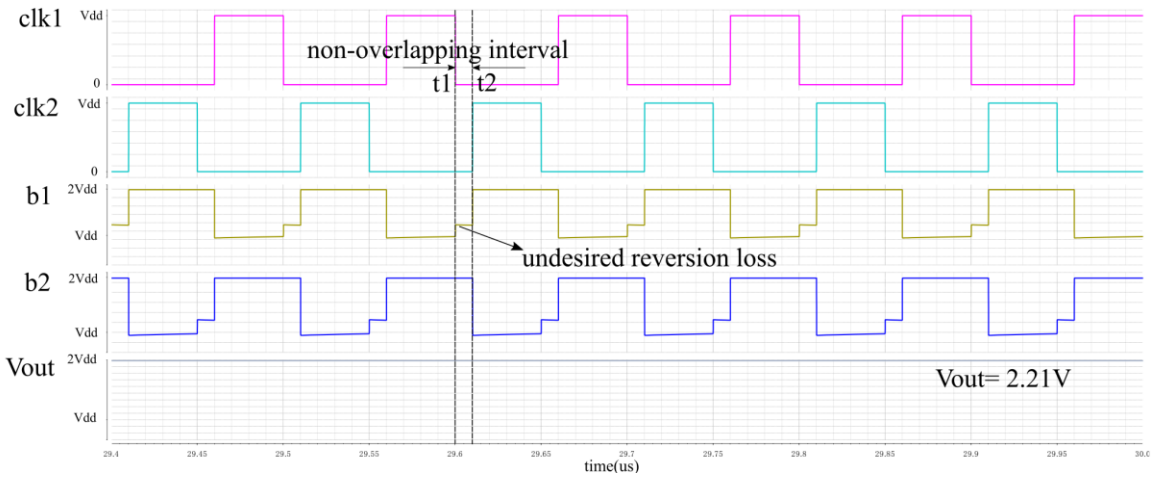
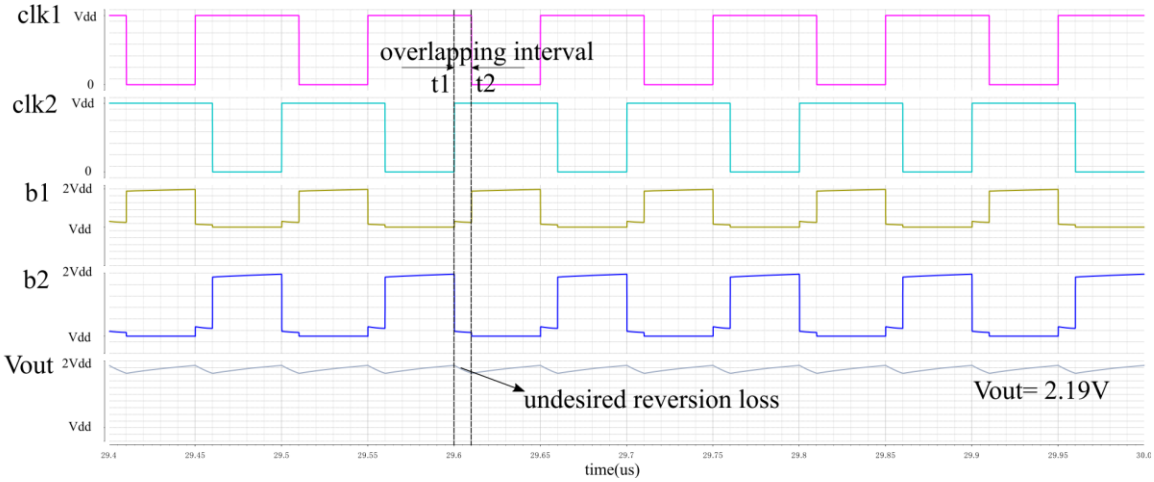


Figure 2.11: Reversion loss paths in Voltage Doubler 1.



(a) Driven with non-overlapping signals



(b) Driven with overlapping signals

Figure 2.12: Waveforms for Voltage Doubler 1 driven with different clock signals.

When Voltage Doubler 1 is driven by non-overlapping clock signals as shown in Figure 2.12(a), reversion losses happen during the non-overlapping interval between *t1* and *t2*. Specifically, since both *clk1* and *clk2* are at the ground during this interval, *a1* and *a2* are both connected to Vdd and thus both *b1* and *b2* are at 2Vdd. In this situation, as switches NMOS3 and NMOS4 are turned on undesirably at the same time, reversion losses may exist. These undesired conductions cause reverse charges from C1 and C2 to Vdd, the paths of which are shown in Figure 2.11. This type of reversion loss from flying capacitors is called pump loss in the literature [40], as flying capacitor in a Charge Pump [32] (a cross-coupled voltage doubler is also called a cross-coupled charge pump) is also called pump capacitor. As shown in the simulation waveform in Figure 2.12(a), there is a clear voltage drop during the time interval when both *clk1* and *clk2* are at 0. The output voltage here

drops compared with the voltage doubler driven with inverted clock signals due to the undesirable reverse charge. The reverse charge leads to additional power loss, thus reducing the power efficiency of the voltage doubler.

When the Voltage Doubler 1 is driven by overlapping signals as shown in Figure 2.12(b), reversion losses happen during the overlapping interval between *t1* and *t2*. During this time interval, as both *clk1* and *clk2* are at Vdd, *a1* and *a2* are connected to ground, making *b1* and *b2* connected to Vdd. In this situation, PMOS2 and PMOS4 are turned on undesirably at the same time. As a result, reversion losses happen. These undesired conductions cause reverse charge from the output to flying capacitors C1 and C2, the paths of which are shown in Figure 2.11. This type of reversion loss from the output to flying capacitors is called output loss in the literature [40]. A noticeable voltage drop can also be seen during the overlapping interval in the waveform. Similarly, the output voltage drops and the power efficiency decreases due to these output losses.

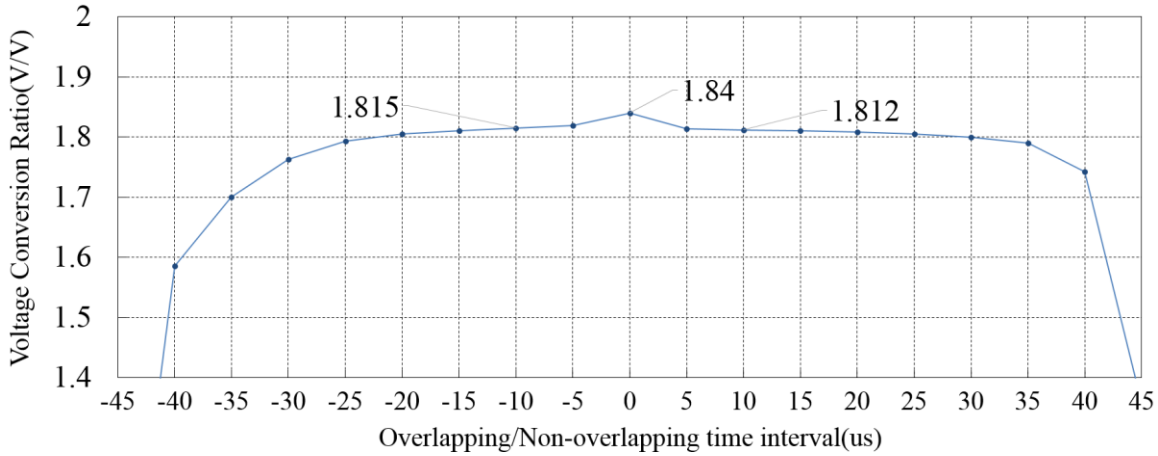


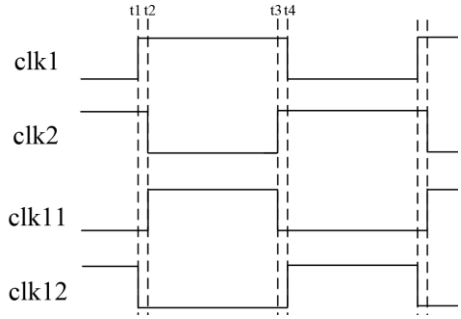
Figure 2.13: VCRs for Voltage doubler 1 with different overlapping and non-overlapping clocks.

The level of the reversion loss is associated with the time of the non-overlapping or overlapping time gap. Figure 2.13 shows VCR of Voltage Doubler 1 is controlled by clocks with different scale of overlapping and non-overlapping time (with 10K loads). The VCR of the Voltage Doubler 1 drops with increase in the overlapping or non-overlapping time from 0 to 30us. When the time gap is over 35us, the reversion loss leads to failure of Voltage Doubler 1 to behave reasonably as a voltage doubler.

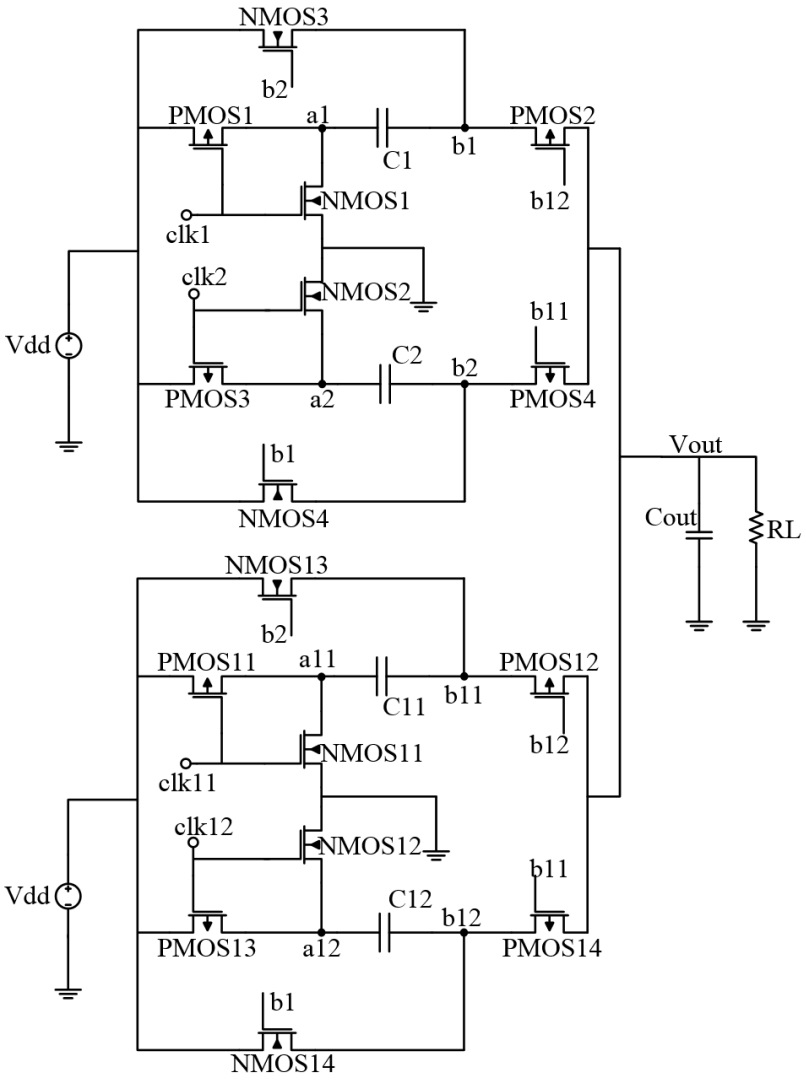
In summary, the nature of the pump losses and output losses are reverse charges due to the undesired conduction of MOS switches. The direct cause of these reversion losses are specific combinations of signals connected to the MOS switches.

2.2.3 Designs that eliminate reversion losses

A new cross-coupled voltage doubler design attempting to eliminate reversion losses is proposed in [18], which is referred to as Voltage Doubler 2 in this thesis. The schematics of Voltage Doubler 2 and its control signals are shown in Figure 2.14.



(a) Control signals



(b) Voltage Doubler 2

Figure 2.14: Voltage Doubler 2 and its control signals, adapted from [18].

As can be seen from the schematic in Figure 2.14(b), it has two copies of the Voltage Doubler 1 shown in Figure 2.9, with a further level of cross-coupled signals. Consequently,

the number of control signals and internal signals are doubled compared to Voltage Doubler 1.

In Voltage Doubler 2, switches PMOS2 and PMOS4 of the upper doubler are controlled by internal signals *b12* and *b11* from the lower doubler instead of *b2* and *b1* from their own block. Similarly, switches NMOS13 and NMOS14 of the lower doubler are controlled by internal signals from the upper one. At the same time, the upper voltage doubler is controlled by overlapping clocks and the lower one is controlled by non-overlapping clocks, where the transitions of these clocks need to be synchronised strictly as shown in the Figure 2.14(a).

In this design, the reversion losses in one copy of the voltage doubler are eliminated by external controls from the other copy. During the time interval *t1* to *t2*, *b1* and *b2* are both connected to Vdd and *b11* and *b12* are both at 2Vdd. For the upper one, there is no output loss from the output Vout to flying capacitors C1 and C2 as PMOS2 and PMOS4 are switched off by signals *b12* and *b11*. Similarly, for the one below, there is no pump loss from C11 and C12 to Vdd since NMOS13 and NMOS14 are turned off by signals *b2* and *b1*. Besides, this cross-coupled voltage doubler design is able to eliminate the shoot-through current compared with Voltage Doubler 1. This aspect is verified in Chapter 4 with Petri net model.

However, in this design, the control signals (clock signals) need to be strictly synchronised. There may be reversion losses when there is any timing mismatch of the control signals. Reversion losses due to timing mismatch of the control signals are also analysed with the Petri net model in Chapter 4.

To eliminate reversion loss problems as well as control signal synchronisation problems, a few newer cross-coupled voltage doubler designs are proposed [40]-[58]. The methods of these reversion-loss-free designs can be divided into two types. The first type of design eliminates the reversion loss by extra blocking transistors that switch off the path of the reversion loss when it happens. The second type of design cancels the reversion loss by introducing extra external control for the MOS switches that have the reversion loss problem. Two classical designs with these two types of techniques are introduced as follows. These designs are further analysed with Petri nets in Chapter 4.

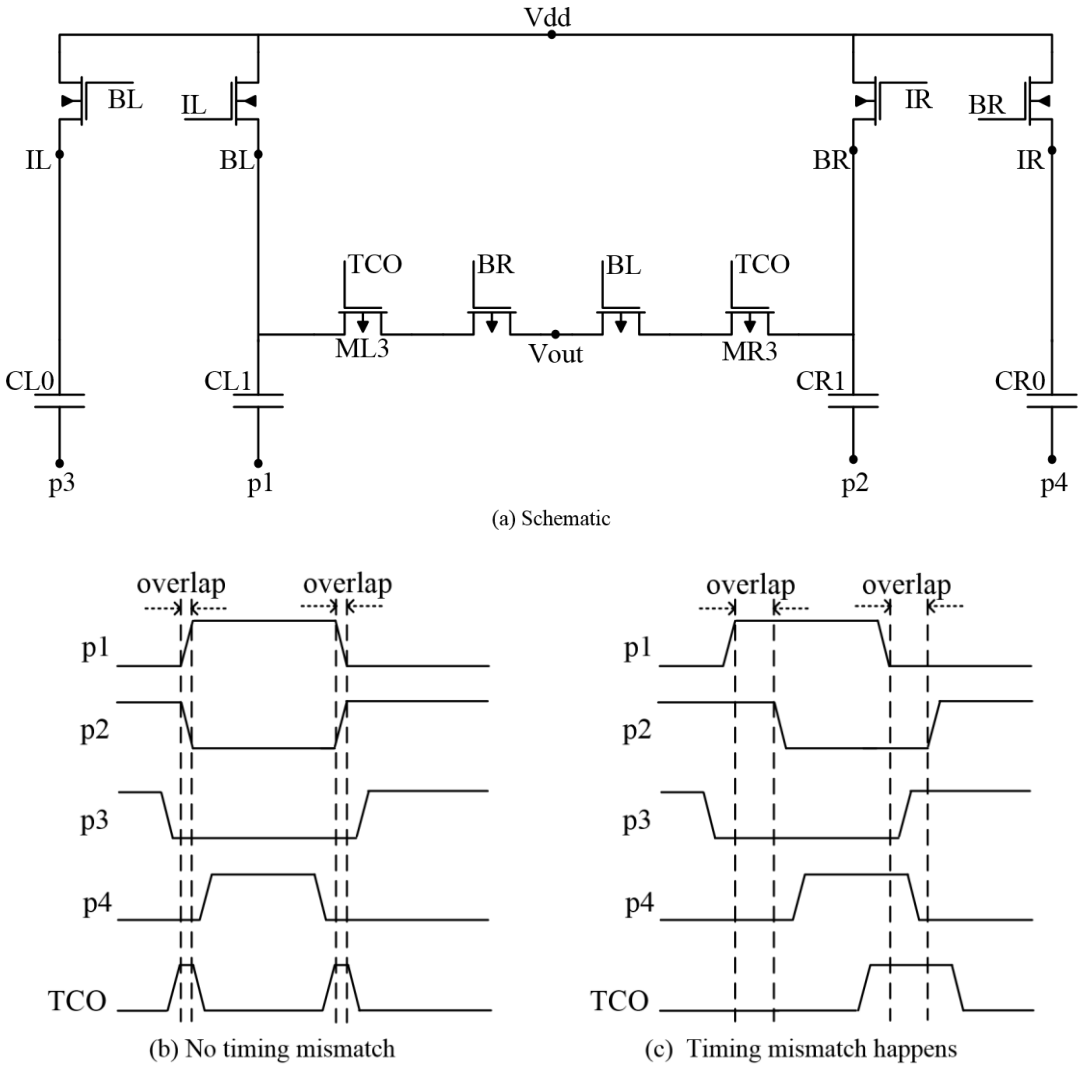
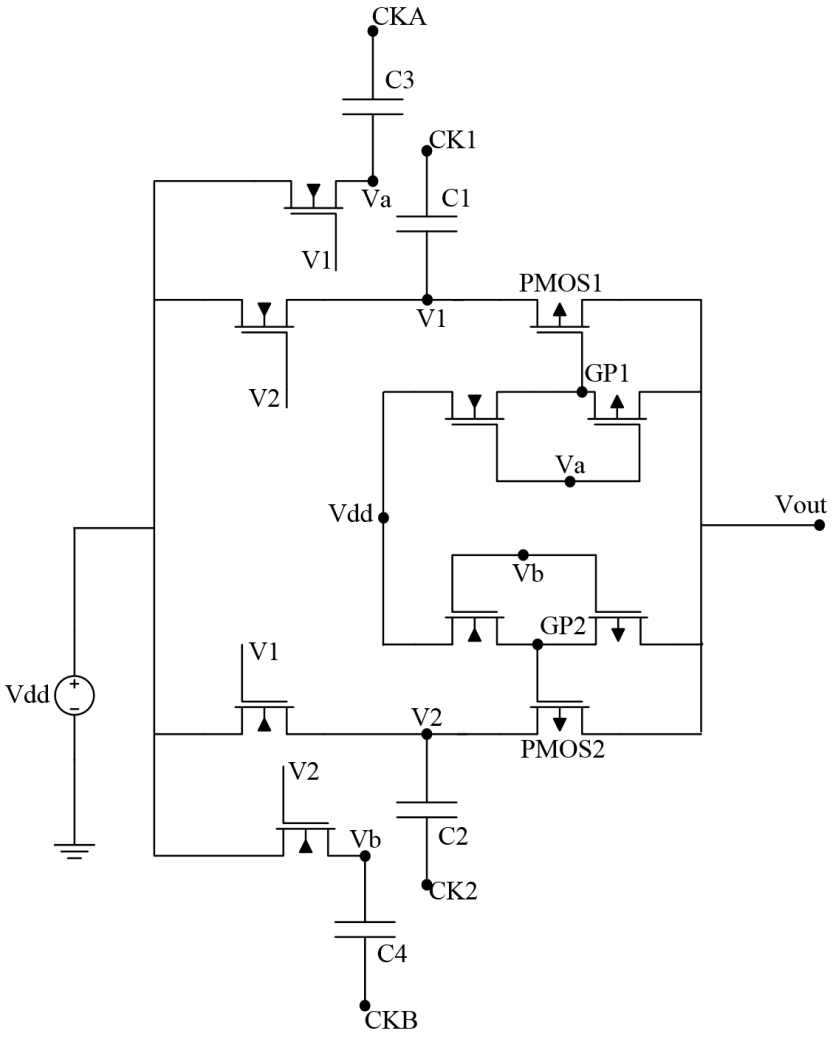


Figure 2.15: Voltage Doubler 3 and its control signals, adapted from [40].

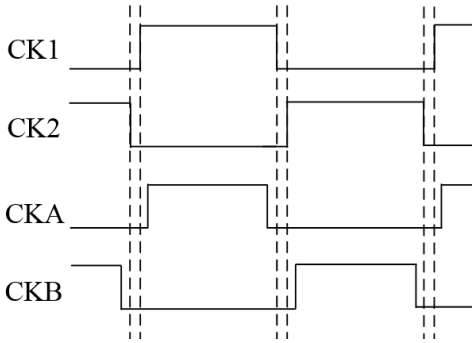
Figure 2.15 shows a classical design [40] with the first type of reversion loss elimination method, referred to as Voltage Doubler 3 in this thesis. Voltage Doubler 3 is controlled by control signals *p1*, *p2*, *p3* and *p4*. Its MOS switches are controlled by internal signals *BL*, *BR*, *IL*, *IR*, which are indeed impacted by control signals *p1*, *p2*, *p3* and *p4* with capacitor coupling effects. There are two extra blocking MOS switches ML3 and ML4 controlled by signal *TCO*. *TCO* is a signal from the overlapping detector (the schematic can be seen in [40]).

In theory, there will be output losses from the output Vout to the flying capacitors during the overlapping interval of the clock pair (*p1*, *p2*). However, output losses in Voltage Doubler 3 have been blocked by extra MOS switches. Two extra MOS switchers ML3 and MR3 controlled by *TCO* are utilised to block the path of the reversion loss. *TCO* signal will be activated by the extra overlapping detector when *p1* and *p2* are both in transition as

shown in Figure 2.15(b) or a timing mismatch happens as shown in Figure 2.15(c). Switches ML3 and MR3 will be turned off when *TCO* is activated, blocking the path of the reversion loss from the output. In addition, clock signal pairs (*p1*, *p3*) and (*p2, p4*) are non-overlapping, so that neither signal pairs (*IL*, *BL*) nor (*IR*, *BR*) will be at 2Vdd at the same time. Consequently, there is no pump loss from flying capacitors to Vdd.



(a) Voltage Doubler 2



(b) Control signals

Figure 2.16: Voltage Doubler 4 and its control signals, adapted from [47].

Compared with Voltage Doubler 2, this type of voltage design has a further capability of eliminating the reversion loss due to the control signal mismatch. However, the trade-off is introducing extra MOS devices and extra overlapping detector circuit. Notably, similar to Voltage Doubler 2, there are also some internal signals introduced in Voltage Doubler 3, including *IL*, *BL*, *IR*, *BR*.

Figure 2.16(a) shows a cross-coupled voltage doubler design [47] which eliminates reversion losses by employing the second type of elimination method, and this is referred to as Voltage Doubler 4 in this thesis. Voltage Doubler 4 also has four control signals *CK1*, *CK2*, *CKA* and *CKB*. The MOS switches are controlled by internal signals *V1*, *V2*, *Va*, *Vb*, which are indeed impacted by control signals *CK1*, *CK2*, *CKA* and *CKB* with capacitor coupling effects. In addition, another two extra signals *GP1* and *GP2* are introduced to control the PMOS1 and PMOS2.

In theory, there will be output losses from the output Vout to the flying capacitors during the overlapping interval of the clock pair (*CK1*, *CK2*) if PMOS1 and PMOS2 are controlled by *V2* and *V1*. However, such reversion losses for PMOS1 and PMOS2 are eliminated by introducing external controls of *GP1* and *GP2*. The value of external controls *GP1* and *GP2* are affected by internal signals *Va* and *Vb* with two extra pairs of MOS switches. *GP1* and *GP2* are indeed controlled by *CKA* and *CKB*, as *CKA* and *CKB* are capacitor coupling with *Va* and *Vb*. Then [47] develops a control scheme that avoids the reversion loss problem based on conventional waveform analysis, which is shown in Figure 2.16(b). During the overlapping interval of (*CK1*, *CK2*), *CKA* and *CKB* are both at 0, *Va* and *Vb* are then both at Vdd because of capacitor coupling effects and *GP1* and *GP2* are both connected to 2Vdd. As a result, *GP1* and *GP2* will turn off PMOS1 and PMOS2 during the overlapping interval so that the output losses are avoided. Meanwhile, it is also claimed that there are no pump losses as *CK1* and *CK2* are non-overlapping that *V1* and *V2* will not be at 2Vdd at the same time.

Compared with the Voltage Doubler 2, transitions of control signals do not need to be synchronised. Compared with the Voltage Doubler 3, this design does not need an extra blocking transistor and overlapping detector. However, the scheme of the control signals that will not lead to a reversion loss for Voltage Doubler 4 or other cross-coupled voltage doublers adopting similar reversion loss eliminating techniques requires careful analysis, as signals in such designs are complicated. As the complexity increases, the conventional

methods of verbal reasoning and waveform analysis become cumbersome and less trustworthy.

A common phenomenon existing in the cross-coupled voltage designs introduced in this subsection is that there are a couple of control signals and internal signals. These signals control the MOS switches directly or indirectly, which may further affect the working principle of these designs. However, the conventional modelling methods for SCDDCs seem to overlook these signals and the relationship between these signals, which may cause confusion for the reader in understanding these designs. At the same time, some states of these signals may also cause a reversion loss problem. These designs propose different techniques to avoid reversion losses, and there is no formal way to describe and analyse the reversion loss that can be used for formal verification. The design methods also depend heavily on intuition, as formal discrete state models for design did not exist until the work reported in this thesis. In addition, the design methods adopted in these designs are not flexible (being dependent on dedicated clock generators), as demonstrated and analysed with Petri nets in Chapter 4.

2.3 Existing modelling methods

In this section, the modelling methods of Charge Flow Analysis and Output Impedance Analysis are introduced. Using these modelling methods for an SCDDC, an optimal value for the flying capacitor and the working frequency of control signals can be selected to achieve a higher power conversion performance and power efficiency.

2.3.1 Charge Flow Analysis

In Charge Flow Analysis [10] for SCDDCs, a set of vectors is defined to describe the topologies and to identify the sub-net configurations in different phases based on the charge flow through switches and capacitors. Charge Flow Analysis quantifies SCDDCs' performance and enables objective comparison of SCDDCs' topologies, playing an essential role in the conventional modelling methods of SCDDCs.

The charge flow through the capacitors is defined as:

$$a_c^{(1)} = \left[q_{out}^{(1)}\ q_1^{(1)} \dots\ q_n^{(1)}\ q_{in}^{(1)}\right] /\ q_{out}$$

$$a_c^{(2)} = \left[q_{out}^{(2)}\ q_1^{(2)} \dots\ q_n^{(2)}\ q_{in}^{(2)}\right] /\ q_{out}$$

…

$$a_c^{(m)} = \left[q_{out}^{(m)}\ q_1^{(m)} \dots\ q_n^{(m)}\ q_{in}^{(m)}\right] /\ q_{out}$$

Where $q_i^{(m)}$ denotes the amount of charge transferred to flying capacitor i during phase m, and q_{out} represents the total amount of charge that is transferred to the output during a switching period T.

The values of each vector element follow the undernoted principles:

- Kirchhoff's current law. The sum of charge flow elements at every circuit node equals to zero.
- For every capacitor, the sum of charge flow elements of all phases equals zero.

For example, the charge flow vectors for the voltage doubler shown in Figure 2.1 are shown in below:

$$a^1 = [0 \quad -1 \quad 1]$$

$$a^2 = [1 \quad 1 \quad 1]$$

As can be seen clearly from the vectors, the vector elements of the flying capacitors in two phases have opposite signs. More details about Charge Flow Analysis can be reviewed in [10] and [32].

Output Impedance Analysis and related calculations introduced in Subsection 2.3.2 are based on Charge Flow Analysis.

2.3.2 Output Impedance Analysis

In the Output Impedance Analysis model, SCDDCs are modelled as a combination of an ideal DC-transformer with a fixed VCR and a finite output resistance [59], which is shown in Figure 2.17.

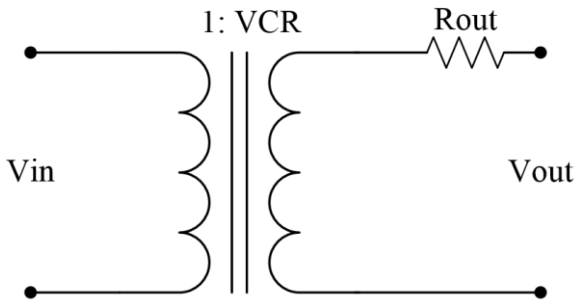


Figure 2.17: Output Impedance Analysis Model for SCDDCs.

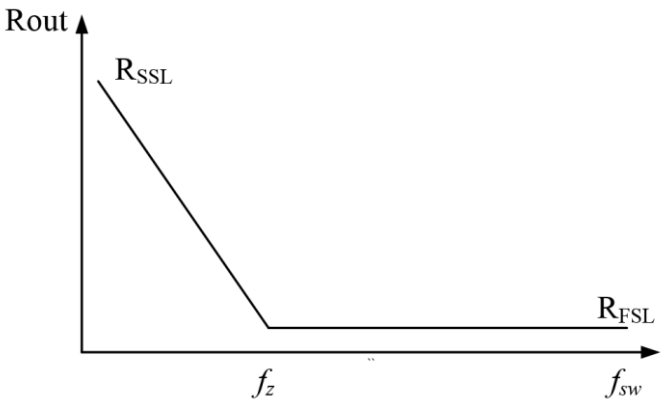


Figure 2.18: SSL and FSL impedance model for SCDDCs.

There are two distinct asymptotic limits to the output impedance: Slow Switching Limits (SSL) and the Fast Switching Limits (FSL). These two impedance models are related to the switching frequency, as shown in Figure 2.18.

Slow Switching Limits (SSL)

SSL is an analysis based on the effect of the switched-capacitor nature of the converter, assuming that the resistances of switches and other interconnects are ideal [57]. The SSL impedance is a function of the switching frequency and the amount of flying capacitance. For an SCDDC with i flying capacitors and m phases, the SSL impedance is described as follows:

$$R_{SSL} = \sum_{cap,i} \sum_{phases,m} \frac{(a_{c,i}^{m})^2}{2 f_{sw} C_i}$$

where $a_{c,i}^{m}$ is the charge flow vector element of the capacitor i in the m^{th} phase.

For a two-phase SCDDC, the SSL impedance is described as:

$$R_{SSL} = \sum_{cap,i} \frac{a_{c,i}^{2}}{f_{sw} C_i}$$

The SSL impedance models the power loss due to the charging and discharging of the flying capacitors, ignoring the parasitic resistance in an SCDDC. This impedance can be obtained by only examining the charge flow in SCDDCs, without complex network analysis or simulations.

Fast Switching Limits (FSL)

FSL is an analysis based on the resistive nature of the converter, assuming capacitors as a fixed voltage source [57]. The FSL impedance is frequency independent. For an SCDDC with n switches and m phases, the FSL impedance is described as follows:

$$R_{FSL} = \sum_{switchers,i} \sum_{phases,m} \frac{(a_{R,i}^{m})^2}{G_i D_m}$$

where $a_{R,i}^{m}$ is the charge flow vector element of the switch i in the m^{th} phase, G_i is the conductance of the switch i and D_j is the duty cycle of the phase m.

For an SCDDC with n switches and m phases with a 50% duty cycle, the FSL impedance is described as follows:

$$R_{FSL} = 2 \sum_{switchers,i} \frac{(a_{R,i})^2}{G_i}$$

Analogous to the SSL impedance, the FSL impedance is determined by the component parameters and charge flow vectors of the switches.

Practical output impedance

Both the SSL and the FSL impedance only model the output impedance of SCDDCs in extreme cases. In practice, an SCDDC is subject to both capacitive and resistive power losses. In [11], the practical output impedance $Rout$ is described as a combination of SSL and FSL impedance, which is expressed as follows.

$$Rout = \sqrt{{R_{SSL}}^2 + {R_{FSL}}^2}$$

The practice output impedance can be used to improve the power efficiency of an SCDDC. Generally, the power efficiency η [32] of an SCDDC is defined as:

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} \times 100\%$$

Where P_{out} is the output power and P_{loss} is the total power loss in an SCDDC. The power loss due to the practical output impedance $Rout$ is a significant part of the total power loss.

Therefore, Output Impedance Analysis gives the designer a simple way to estimate the power loss due to both charging and discharging of the capacitors and the resistance of the switches without complex analysis and simulations. At the same time, the total power loss can be reduced by optimising the parameters of SCDDCs such as switching frequency and flying capacitance, enabling an SCDDC design with higher power efficiency.

In summary, the existing modelling methods overviewed in this section concentrate on the analogue attributes such as charge flow and equivalent output impedance of SCDDCs. Generally, these conventional modelling methods overlook discrete attributes such as signal transition and relations between transitions of SCDDC. They do not, consequently, shed light on the qualitative question of the existence or absence of reversion loss. There are only natural language descriptions with assisted waveform employed to describe these discrete events in the literature, which are not easy to understand and cause confusion.

2.4 Discrete event Models

In this thesis, discrete event models such as Petri nets and Signal Transition Graph (STG) are utilised to model and analyse discrete events and their relationships in SCDDCs. Furthermore, asynchronous control design based on STG for SCDDCs is included in Chapter 5. This section presents the background for these discrete event models and then provides a fundamental review of asynchronous circuit design flow and the related CAD tools.

2.4.1 Petri nets

Petri nets were first introduced in the early 1960s, which are graphical and mathematical representations of distributed systems [60]. Petri nets are widely used to describe and analyse distributed, concurrent and non-deterministic systems. The Petri net model shows possible behaviours of discrete systems using a simple graphical description of the system.

Definitions

A Petri net model PN is a tuple $C = \langle P, T, F, M_0 \rangle$ where

$P = \{p_1, p_2, p_3, \dots, p_n\}$ is a finite non-empty set of places,

$T = \{t_1, t_2, t_3, \dots, t_n\}$ is a finite non-empty set of transitions such that $P \cap T = \phi$,

$F \subseteq P \times T \cup T \times P$ is a flow relation between place P and transition T,

$M_0 \in [P \to N]$ is the initial marking.

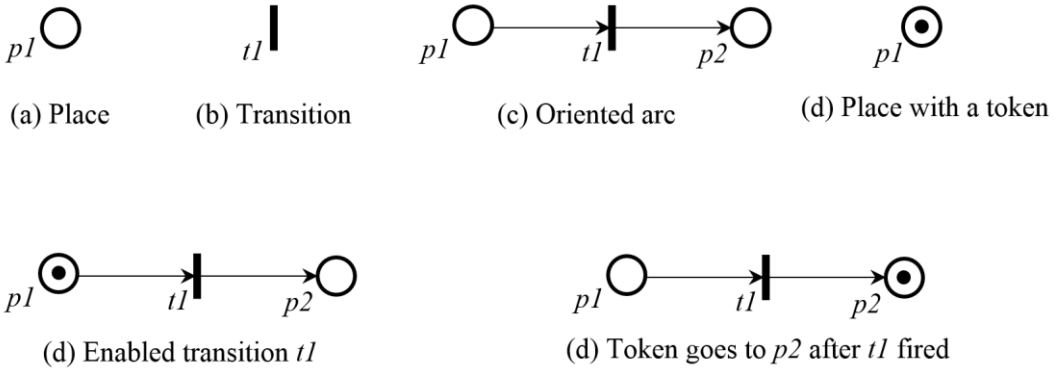


Figure 2.19: Elements of Petri nets.

Figure 2.19 shows some elements of a Petri net graph, where places are represented by circles (Figure 2.19(a)), rectangles represent transitions (Figure 2.19(b)) and oriented arcs indicate flow relations between places and transitions (Figure 2.19(c)). A marking is represented by a set of tokens (solid disks) inside the places of a Petri net (Figure 2.19(d)). The Petri net marking represents its current state. The Petri net state changes with firings of its enabled transitions. A transition is enabled if all of its input places (A place with an arc from itself to a transition is an input place of the transition) have tokens and an enabled transition may fire (Figure 2.19(e)). The firing of a transition decreases the number of tokens in every one of its input places by one and increases the number of tokens in every one of its output places (a place with an arc from a transition to itself is an output place of the transition.) by one (Figure 2.19(f)).

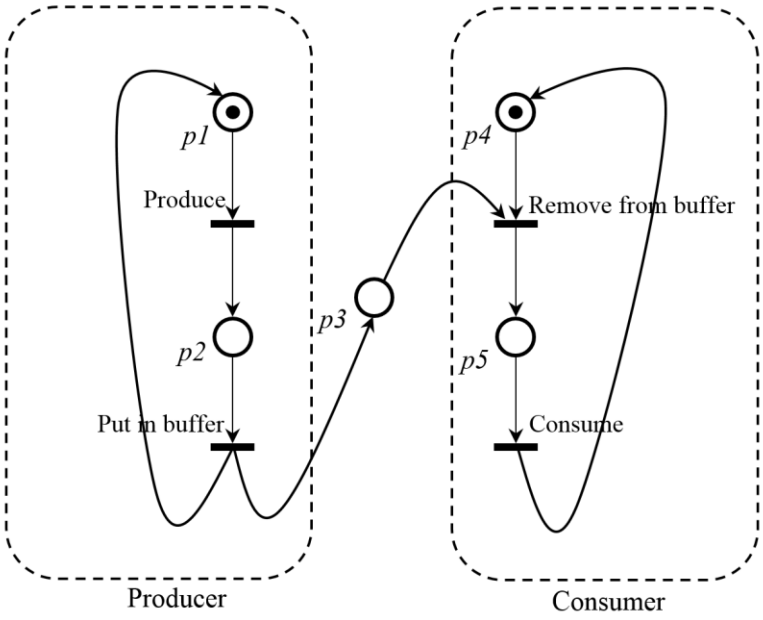


Figure 2.20: Petri net example: Producer and Consumer problem.

Figure 2.20 shows a simple Petri net example of the Producer and Consumer problem. This Petri net model contains five places and four transitions, with places *p1* and *p4* each holding a token, which describes that as long as the producer produces an object and puts it into the buffer, the consumer can remove it from the buffer and consume it.

Reachability analysis

Reachability analysis investigates whether a target state is reachable from a specific initial marking in a Petri net model. It plays a critical role in Petri net theory, since other problems such as liveness analysis and deadlock verification can be reduced to reachability analysis [60]. In actual Petri net applications, it is commonly used to detect fault or hazard problems [61]-[64].

2.4.2 Signal Transition Graphs (STGs)

The Signal Transition Graph (STG) model was first introduced in [20] and [25] to formally model the behaviour of asynchronous circuits and their environments. STG is a domain-specific Petri net for specifying asynchronous circuits. An STG has two types of transitions, positive transition and negative transition, to represent the signal behaviours (rising and falling voltages) in a circuit. With directed arcs indicating the relations between these signal transition behaviours, STG clearly defines the causality and concurrent relationship for a circuit.

Definition

An STG is a tuple $G = \langle PN, I, O, L \rangle$ where

$S \in [I \cup O]$ is a set of all input and output signals,

$L: T \rightarrow S \times \{+, -\}$ is the labelling function,

$S \times \{+, -\}$ is the set of transitions of input and output signals.

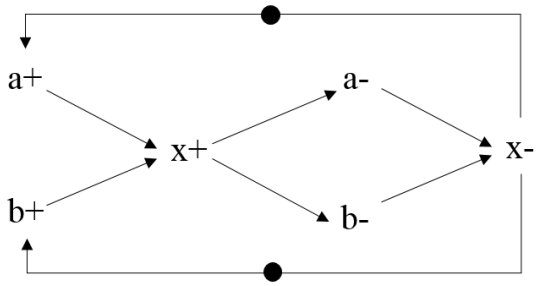


Figure 2.21: Example of an STG modelling a system with featuring concurrency.

As STGs are derived from Petri nets, the graphic representations of STGs are similar to Petri nets. An STG example of a system featuring concurrency is shown in Figure 2.21. In this STG, all places are hidden, which allows transitions to be connected with an arc directly, e.g. on the arc between $a+$ and $X+$, there is assumed to be a place which is removed in the representation. This STG describes the concurrency and causality relationships between signal transitions in this concurrent system. Tokens on the arcs between $X-$ and $a+$ and $b+$ indicate the initial state of this system.

Formal verification methods

STGs provide asynchronous circuits with a convenient theoretical background for specifications and verifications. The property verifications for STGs include:

- Deadlock-freeness: There is no state where all signals are disabled.
- Consistency: In any firing sequences starting from M_0, the positive and negative transitions of every signal must alternate.
- Output-persistence: An enabled transition of an output signal must not be disabled by a transition of any other signal.
- Complete State Coding (CSC): if there are two markings with the same binary code, the output signals enabled at those markings should be the same.

2.4.3 Asynchronous circuits

Asynchronous circuits are fundamentally different from synchronous circuits. Asynchronous circuits utilise a handshaking mechanism between their components to implement the necessary synchronisation and communication, while a global clock is employed in the synchronous circuit to do such necessary actions.

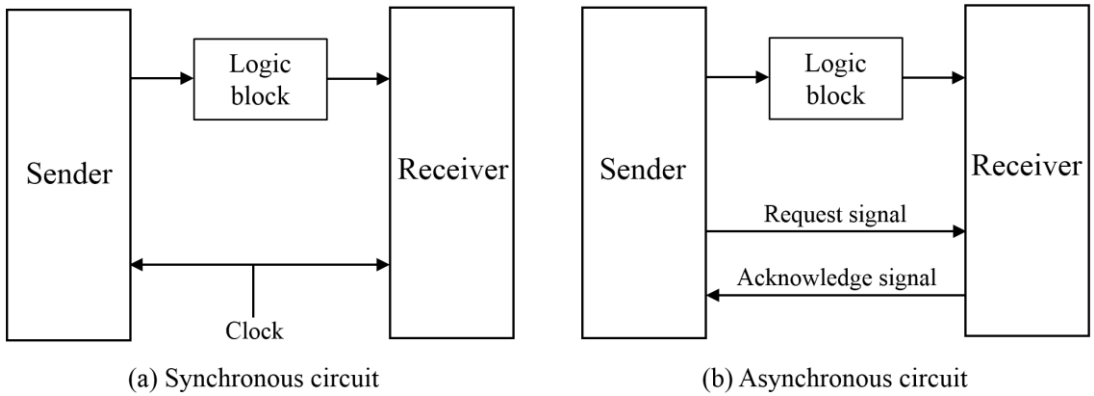


Figure 2.22: Communication methods for synchronous circuit and asynchronous circuit.

Figure 2.22 describes the difference between synchronous communication and asynchronous communication. In the asynchronous communication circuit, the handshaking process is started with which the initial computation unit sends a request signal to the receiver, then the receiver returns an acknowledge signal to confirm the arrival of the related data.

The handshaking mechanism without using global clock gives asynchronous circuits some inherent advantages over synchronous circuits, which mainly include:

- No global clock distribution or clock skew [65].
- Robust to process, voltage and temperature variation [66].
- Lower power consumption [67].
- Average case performance [68].
- Less emission of electromagnetic noise [69].
- Modularity [70].

In an asynchronous circuit design flow, STGs are commonly used for the specifications. After the STG passes the verifications mentioned in Subsection 2.4.2, implementations can be generated automatically by synthesising the STG in tools for discrete event models such as Workcraft, which is introduced in Subsection 2.4.4.

2.4.4 Tools for discrete event models

There are many support tools available for discrete event models such as Workcraft [71], Petrify [70], Mpsat [73], CPN tools [74], EPNK [75], PIPE2 [76], ORIS [77], CLP [78] etc. The tool employed in this work to process the analysis and synthesis of Petri nets and STG is Workcraft. The UI of Workcraft is shown in Figure 2.23.

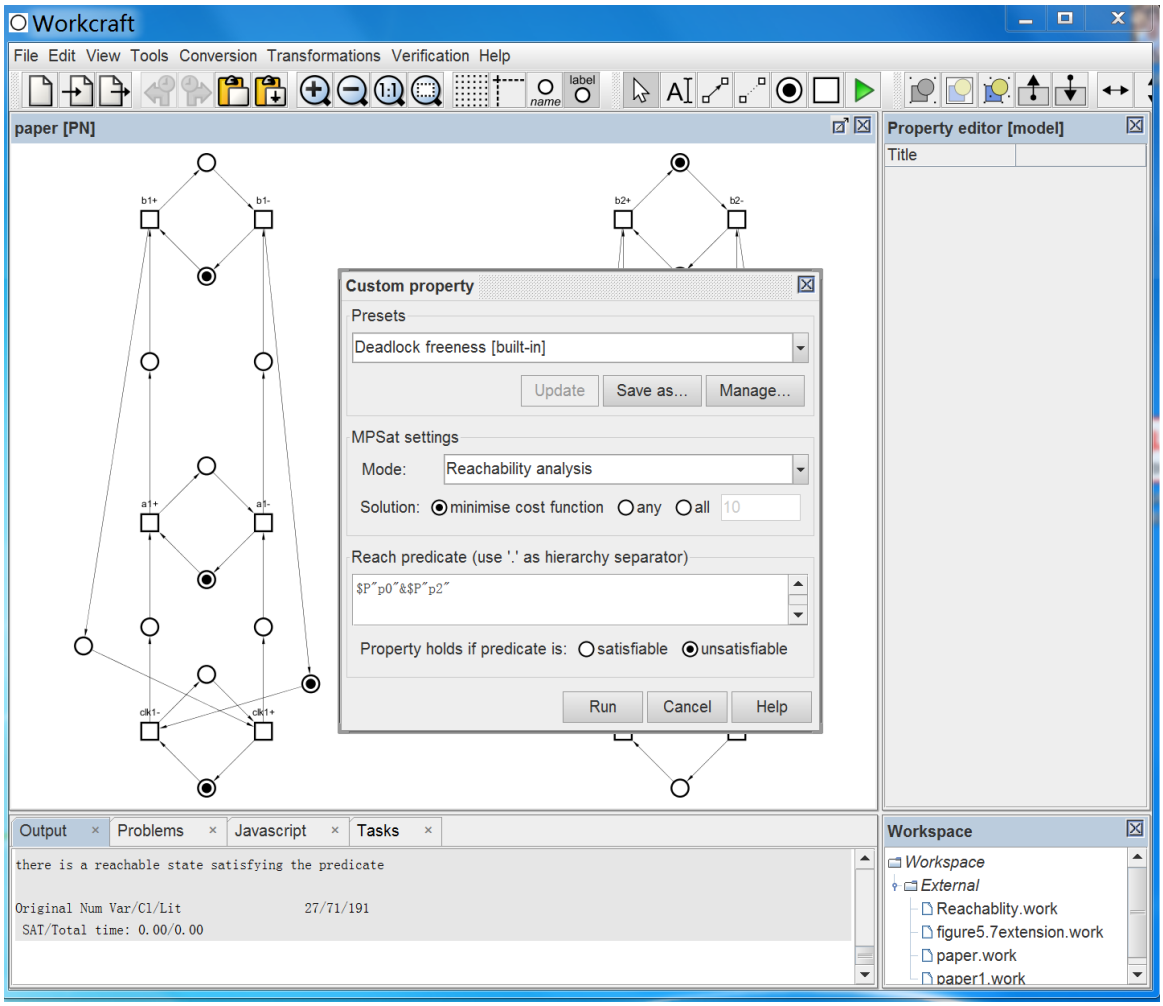


Figure 2.23: UI of Workcraft.

The Workcraft tool was developed at Newcastle University and is freely available for both academic and commercial use. Workcraft provides a flexible common framework for discrete event models, containing visual editing, simulation and analysis, integrating back-end tools such as Petrify and Mpsat. For Petri nets, Workcraft supports not only the deadlock freeness check but also the reachability analysis. For STGs, Workcraft supports formal verifications such as consistency, deadlock freeness, output persistency and CSC check via integrated back-end tools Mpsat. Meanwhile, the asynchronous circuits can be synthesised from STG via back-end tools Mpsat or Petrify. Four synthesis options are

available in Workcraft, including Complex gate, Generalised C-element, Standard C-element and Technology mapping. All of these synthesis options can be carried out by tools Mpsat or Petrify. In Chapter 5, Technology mapping via Mpsat is adopted to synthesis the STG, the synthesised circuit can be imported in tools such as Cadence Virtuoso with hardware description languages. Workcraft also supports the conversion of different discrete event models, such as Petri nets and STG employed in this thesis. More details of Workcraft can be reviewed in [71].

2.5 Summary

In this chapter, background knowledge about SCDDCs, discrete event models, asynchronous circuits and existing modelling methods have been introduced. Some analysis and discussion of SCDDCs with different topologies and cross-coupled voltage doublers are also presented.

As discussed previously, conventional modelling methods for SCDDCs concentrate on the analogue properties for improving SCDDCs' performance, neglecting the discrete events in SCDDCs such as transitions and relations between transitions. For discrete events or energy losses resulting from such events, there is no formal method for modelling and analysing, which may cause confusion. This thesis presents new modelling methods for SCDDCs with discrete event models supporting the analysis of discrete events and their consequences.

In the following chapters, SCDDCs introduced in this chapter are modelled using discrete event models, and then a method for designing reversion-loss-free SCDDCs is proposed based on discrete event models.

Chapter 3
Modelling SCDDCs with Extended Signal Transition Graphs

3.1 Introduction

As reviewed in Chapter 1 and Chapter 2, the conventional SCDDCs' modelling and design methods focus more on their analogue attributes such as charge flow and output impedance. For example, [11] proposed Charge Flow Analysis which describes the charge transfer in SCDDCs' components in different phases with a mathematical matrix. [11], [13], [15] and [16] proposed different output impedance models to estimate the equivalent output impedance that can be used to optimise SCDDCs' performance and power efficiency. However, these modelling methods do not consider discrete events and their relationships in SCDDCs. The existing literature [79]-[93] has only employed natural language descriptions with associated waveforms to describe the behaviour of discrete events such as signal transitions and the relations between signal transitions. As to the causality and concurrency relations between events, these conventional descriptions in the previous work may confuse researchers and engineers, especially when SCDDCs become more complex such as the cross-coupled voltage doublers reviewed in Chapter 2. In addition, confusion also may arise when verbal and waveform descriptions are employed to describe discrete events and their relationships in SCDDCs with different topologies, since the principles of such SCDDCs with different topology types vary considerably.

This chapter presents a new description and analysis method that models SCDDCs with a new extension of STGs (SC-STGs or *switched-capacitor signal transition graphs*). STG is a discrete event modelling language that describes and formalises the behaviour of

asynchronous digital circuits. It has two types of transitions, 0 to 1 (+) and 1 to 0 (-), which denote the rising and falling edges respectively of signals in an asynchronous system. STGs clearly define the causal and concurrency relations between two-state (Boolean logic) signals. The STG model is commonly utilised for the specification of asynchronous digital circuits. It provides necessary verification and implementation synthesis for asynchronous circuits, which are supported by tools such as Workcraft.

Modelling SCDDCs with the SC-STG model is an attempt that modelling and analysing SCDDCs from the perspective of discrete events. With the new extended STG model, the causality and concurrency relations between the discrete events in SCDDCs are described clearly in a formal way. Moreover, the representations of multi-value transitions make the analogue variation processes in capacitors also available to be described with SC-STG, presenting more details that can be used for SCDDC analyses and designs. In addition, with certain extensions, some analytical methods and tools as introduced in Chapter 2 for asynchronous circuits may now be applied to SCDDCs through SC-STG models. This method may potentially provide a new perspective for SCDDC design automation, improving the analysis and design flow for SCDDCs. The method of analysing SCDDCs with SC-STG presented in this chapter can be further extended to new verification and design methods for SCDDCs, as detailed in the following chapters.

Section 3.2 of this chapter contains the definition of SC-STG. Modelling examples for two cross-coupled voltage doublers Voltage Double 1 and Voltage Doubler 2 and the corresponding analyses are presented in Section 3.3. Modelling examples of SCDDCs with other topologies as introduced in Chapter 2 and the related analyses are detailed in Section 3.4.

For the completeness of the modelling work as well as convenience of reading, some schematics of SCDDCs that were reviewed in Chapter 2 are reused in this chapter.

The work presented in this chapter was partly published in [94].

3.2 Modelling Method

The definition of SC-STG is introduced in this section, followed by the modelling approach.

The STG model was initially employed to analyse and design asynchronous circuits, where only Boolean signals existed. Some modifications are required when the STG model is

applied to modelling SCDDCs. For example, SCDDCs also include some analogue signals such as the voltage of the capacitors, which requires specific modification. In addition, the signals in SCDDCs (for instance Voltage Doublers) may have more than two stable values that require extending the STG paradigm beyond Boolean representations. The extended definition for SC-STG and associated modifications are shown below.

Definition

The definition of SC-STG is also based on the Petri net.

An SC-Signal Transition Graph (SC-STG) is a tuple $N = \langle PN, C \cup S, \lambda \rangle$, where

$C \cup S$ is a set of capacitors and signals,

$\lambda: T \rightarrow C^T \cup S^T$ is a labelling function that associates action between T and C^T or S^T,

$C^T \subseteq C \times \Delta C$ are capacitor transitions in SCDDC in which $\Delta C = \{c_1 Vdd, c_2 Vdd, c_3 Vdd, \dots, c_n Vdd\}$,

$S^T \subseteq S \times \Delta S$ are signal transitions in SCDDC in which $\Delta S = \{s_1 Vdd, s_2 Vdd, s_3 Vdd, \dots, s_m Vdd\}$,

($c_1, c_2, c_3, \dots, c_n, s_1, s_2, s_2, \dots, s_m$ are constant values).

Compared the definition of STG, a set of input and output signals $I \cup O$ has been modified to a set of capacitors and signals. Specifically, capacitors represent the voltage value of dedicated capacitors and signals include clock signals and internal signals. Meanwhile, the transitions are not only represented by Boolean representations such as '+' and '-'.

Signals

In an SCDDC, signals normally include clock signals and internal signals, which control the charging and discharging process of the flying capacitors. Thus, signal transitions in SC-STG normally consist of internal signal transitions and clock signal transitions. Notably, internal signals are not included for SC-STGs describing SCDDCs with simple topologies as internal signals may not be used.

As the shifting of phases in some SCDDCs are caused by the synchronous transitions of two or more clock signals, a definition of phase shift transition is made for a simplified description.

$$P_i = S_1^T \cap S_2^T \cap \ldots \cap S_n^T$$

where $S_1, S_2, \ldots, S_n$ are clock signals that will transit synchronously.

Capacitors

In an SCDDC, the energy is transferred by charging and discharging of flying capacitors. However, these charging and discharging processes are analogue variation processes, which cannot be directly described with digital transitions. In this work, to describe the causality and concurrency between events, these processes are modelled as multi-value digital transitions, details of which are shown in the next subsection.

Multi-value transition representations

Since the voltage of the capacitors and signals in SCDDCs can take on multiple sustainable constant values, such as 0, 1/2Vdd, Vdd, 3/2 Vdd, some modifications for the representation of signal transitions are required.

- Transitions ΔC and ΔS are normalised by the voltage of input Vdd such that $\Delta C = \{c_1, c_2, c_3, \ldots, c_n\}$ and $\Delta S = \{s_1, s_2, s_3, \ldots, s_m\}$. In SCDDCs, both flying capacitors and signal levels can take finite numbers of sustainable constant values. These values define the specific c_n and $s_n$terms. For instance, in a voltage doubler, c_1= 0, $c_2 = 1$, $c_3 = 2$, s_1= 0, $s_2 = 1$, $s_3 = 2$. s_n and c_m can also take other values associated to discharge processes caused by the load or resistance.
- Capacitor transition of capacitor C_i is represented as $C_{im}^n \times \{+, -\}$, where the subscript m and the superscript n denote the initial value and final value of the transition and symbol '+' or '−' denotes the polarity of the transition.
- Transition of signal S_i is represented as $S_{im}^n \times \{+, -\}$. Specifically, S_{i0}^1+ or S_{i1}^0- is denoted as S_i+ or S_i-, which corresponds to signal transitions in the conventional STGs.
- For transitions caused by the load or resistance that do not have a specified initial or final value, m or n will be omitted.

Some representation examples are shown in Table 3.1.

Table 3.1: Examples of representations in SC-STG.

Notation	Meaning
$C_m^n +$	Capacitor C charged from *m*Vdd to *n*Vdd
$C_m^n -$	Capacitor C discharged from *m*Vdd to *n*Vdd
$C^n +$	Capacitor C charged to *n*Vdd
$C_m -$	Capacitor C discharged from *m*Vdd (caused by load or resistance)
$S_m^n +$	Signal *S* transited from *m*Vdd *to n*Vdd
$S_m -$	Signal *S* discharged from *m*Vdd (caused by load or resistance)
$S +$	Signal *S* transited from *0* to Vdd
$S -$	Signal *S* transited from Vdd to 0

Relations between signal transitions

Relations between transitions in an SCDDC include concurrency and causality relations, both of which can be described clearly with SC-STGs. SCDDCs have several types of causal relations between signals, a transition will cause another transition because of the conduction of switches, capacitor coupling effects and the charging/discharging of capacitors. All of these causal relations are represented with solid arrows.

Modelling methods

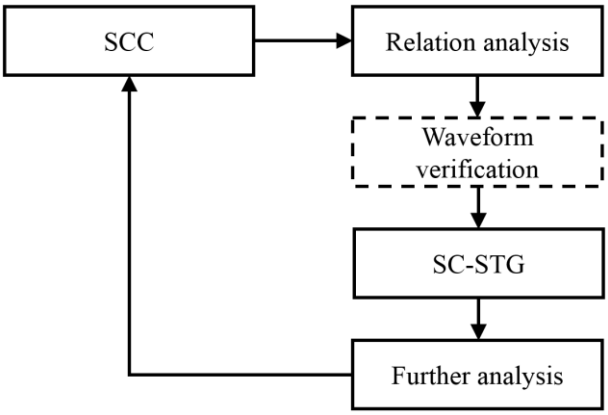


Figure 3.1: Flow chart of modelling SCDDCs with SC-STGs.

The method of modelling SCDDCs with SC-STGs is illustrated in Figure 3.1. The concurrency and causality relations in SC-STG are derived directly from analysing the principle of the SCDDC, which is different from the standard STG generating method where the concurrency and causality relations are often obtained from the simulation waveform. These relations can be first described with a flow chart and then translated to SC-STG. The waveform from a simulation can be utilised to validate those relations

between transitions. Finally, the obtained SC-STG can be utilised for design verification, design tuning, or in larger system analysis. For example, with specified extensions STG verification methods mentioned in Chapter 2 can be applied to SC-STG, which facilitates a further analysis for an SCDDC. In Chapter 4, the concurrency and causality relations described in SC-STG are extended to Petri nets to verify reversion losses in SCDDCs, which can be regarded as a practical application of analysing and verifying SCDDCs with STG. Besides, tools for regular STGs can be potentially adapted for SC-STG use such as Workcraft and other tools mentioned in Subsection 2.4.4.

3.3 Examples

Two example cross-coupled voltage doublers are described and modelled with SC-STG in this section. These two cross-coupled voltage doublers have been introduced in Chapter 2; Voltage Doubler 2 eliminates shoot-through currents with an extra branch of Voltage Doubler 1. The description of shoot-through currents in SC-STG are also discussed.

SC-STG model for the cross-coupled voltage doubler

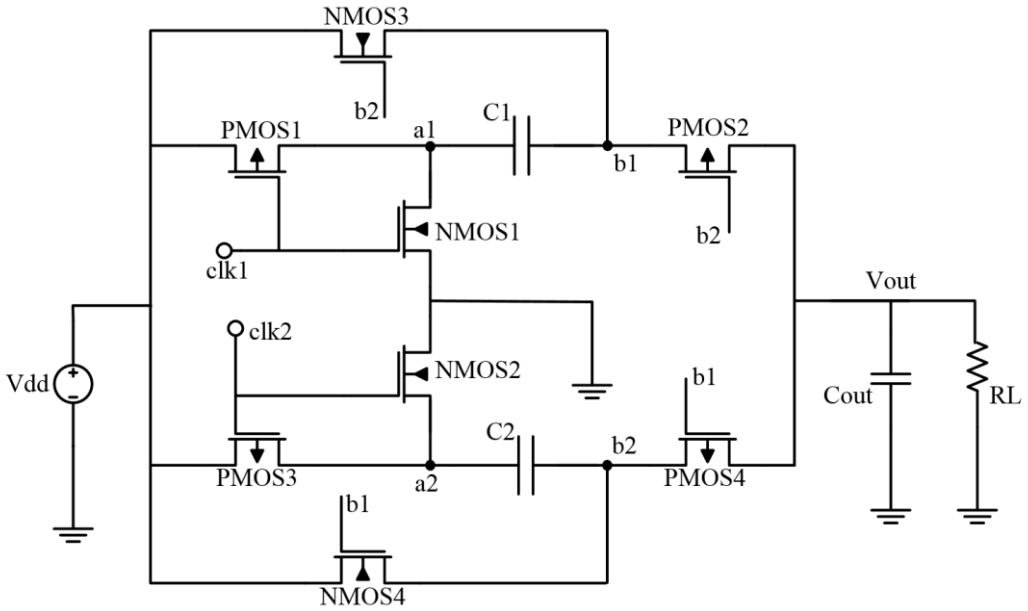


Figure 3.2: Schematic of Voltage Double 1, adapted from [18].

Figure 3.2 shows the cross-coupled voltage doubler (Voltage Doubler 1) that has been introduced in Chapter 2. It has eight MOS switches and four of them are controlled by cross-coupled internal signals *b1, b2*. At the same time, the turned-on or turned-off states of these MOS switches and the charging and discharging processes of the flying capacitors are also affected by the internal signals *a1, a2, b1, b2* and the clock signals *clk1* and *clk2*.

To describe the causality and concurrent relationships among these events in such an SCDDC with complex topology, we model it with SC-STG.

Basically, the voltages at *a1* and *a2* are affected by clock signals *clk1* and *clk2*. Meanwhile, the voltages at *b1* and *b2* are influenced by the voltages at *a1* and *a2* due to capacitor coupling effects. Based on the analysis in Chapter 2, all the detailed causality relationships in this cross-coupled voltage doubler are illustrated in a flow chart shown in Figure 3.3, where the resistances of MOS devices are ignored.

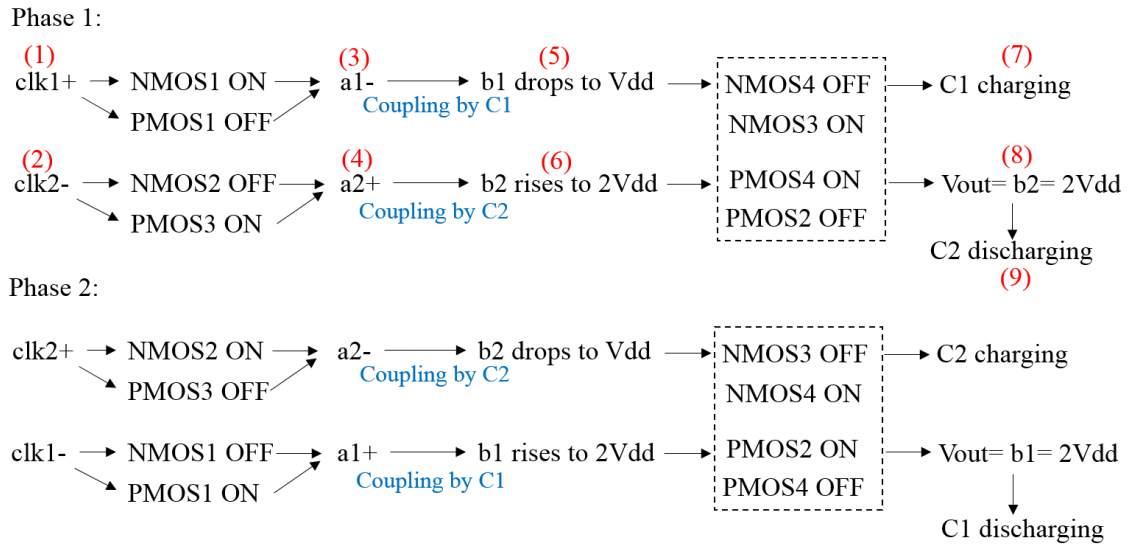


Figure 3.3: Flow chart of events happening in Voltage Doubler 1. (All events in the dashed box are caused by events with an arc to the dashed box)

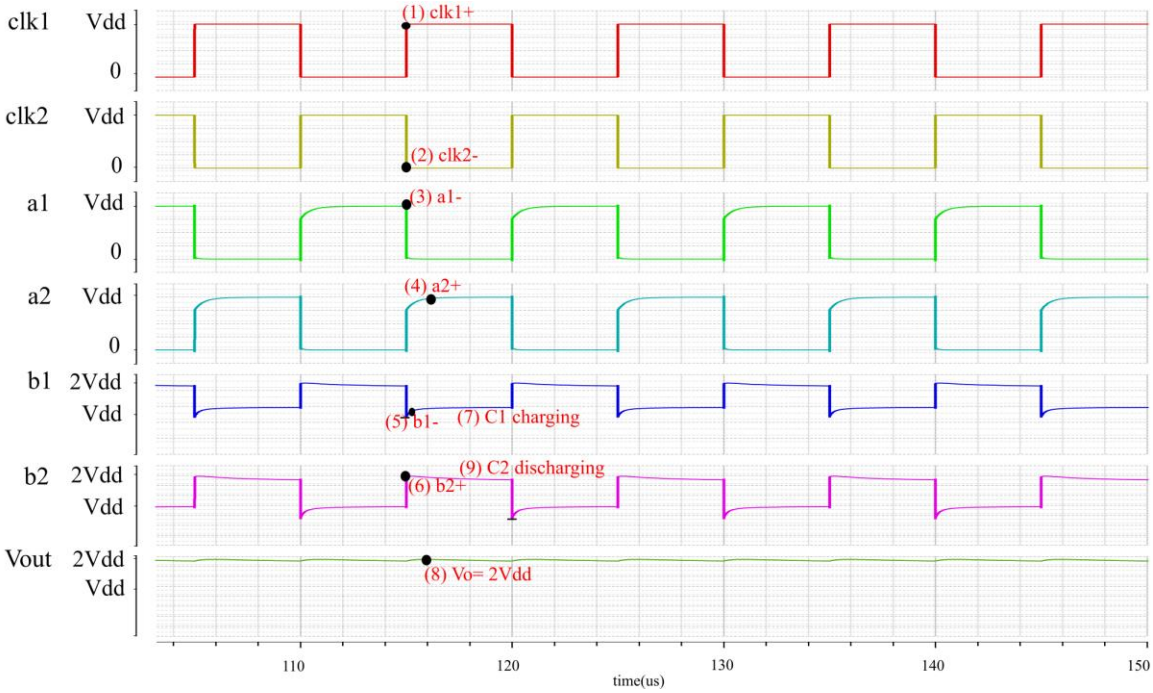


Figure 3.4: Simulation waveform for Voltage Doubler 1 (RL=10K).

As described in the flow chart, when *clk1* is Vdd and *clk2* is 0, NMOS1 is switched on and PMOS1 is switched off, making the voltage at the internal node *a1* 0V. At the same time, the voltage at node *a2* is Vdd as device PMOS3 is on and NMOS2 is off. It brings the voltage at *b2* up to 2Vdd because capacitor C2 was charged to Vdd in the previous half cycle. At the same time, *b1* drops from 2Vdd to Vdd when *a1* falls from Vdd to 0. As a result, device NMOS3 controlled by the node *b2* is turned on and device NMOS4 controlled by the node *b1* is turned off. Consequently, capacitor C1 is charged to Vdd through devices NMOS1 and NMOS3, which will bring *b1* up to 2Vdd in the next half cycle by a capacitor coupling effect. Meanwhile, because *b1* is Vdd and *b2* is 2Vdd, device PMOS4 is turned on and PMOS2 is off, and the output capacitor is charged to 2Vdd. Finally, a discharge process for flying capacitor C2 happens due to the load. In Phase 2 also, there will be an output of 2Vdd in a similar manner.

Based on the modelling method introduced in the previous subsection, the analysis in the flow chart can be verified with the simulated waveforms. Figure 3.4 shows the waveform simulated with Cadence UMC65nm technology (RL=10K). The initial and end values of signal transitions obtained in the flow chart can be firstly verified with the waveform. The concurrency and causality relations between events can be verified by more simulations, e.g. make one or several signals short or open circuit and check the waveforms. These waveforms are not shown here.

Based on the causality and concurrency relations verified with waveform, the SC-STG of Voltage Doubler 1 is shown in Figure 3.5. It assumes Voltage Doubler 1 is working in a stable state where flying capacitors C1 and C2 have been charged to Vdd in the initial marking. Moreover, as Voltage Doubler 1 modelled here is controlled by synchronous clock signals *clk1* and *clk2* as shown in Figure 2.3, for the convenience of description we represent the synchronous signal transitions with phase shift transitions $P1 = clk1+ \cap clk2-$ and $P2 = clk1- \cap clk2+$. Table 3.2 shows representations in this SC-STG.

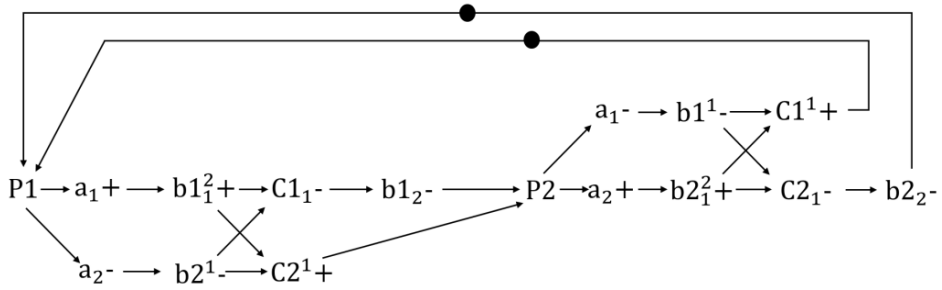


Figure 3.5: SC-STG for Voltage Doubler 1.

Table 3.2: Representations in the SC-STG.

Notation	Meaning
$P1$	Phase transition including *clk1+* and *clk2-*
$P2$	Phase transition including *clk1-* and *clk2+*
$a1+$	Signal *a1* goes up from 0 to Vdd
$a1-$	Signal *a1* goes down from Vdd to 0
$a2+$	Signal *a2* goes up from 0 to Vdd
$a2-$	Signal *a2* goes down from Vdd to 0
$b1_1^2+$	Signal *b1* goes up from Vdd to 2Vdd
$b1_2-$	Signal *b1* goes down from 2Vdd
$b1^1-$	Signal *b1* goes down to Vdd
$b2_1^2+$	Signal *b2* goes up from Vdd to 2Vdd
$b2_2-$	Signal *b2* goes down from 2Vdd
$b2^1-$	Signal *b2* goes down to Vdd
$C1^1+$	Capacitor C1 charging to Vdd
$C1_1-$	Capacitor C1 discharging from Vdd
$C2^1+$	Capacitor C2 charging to Vdd
$C2_1-$	Capacitor C2 discharging from Vdd

With the SC-STG in Figure 3.5, all the causality, concurrency and synchronisation relations among the signals are clearly represented formally. Initially, *P1* is a phase shift transition, which includes *clk1+* and *clk2-*, and *P2* is a phase shift transition which includes *clk2-* and *clk2+*. Phase 1 and phase 2 will start after *P1* or *P2* are fired. Once *P1* fires, *a1-* and *a2+* happen in parallel, and internal signal *b2* rises to 2Vdd due to a capacitor coupling effect from capacitor C2 that was charged to Vdd in the previous half cycle. Meanwhile, internal signal *b1* goes down from 2Vdd to Vdd. In this situation, C1 charges the output and *b1* goes down from 2Vdd due to the load. At the same time, C2 is charged to Vdd, leading to a capacitor coupling effect for *b2* in the next phase. After *P2* fires, C2 charges the output and C1 is charged to Vdd in a similar way.

STG for Voltage Doubler 2

As introduced in Subsection 2.2.3, Voltage Doubler 2 eliminates shoot-through currents. It also can be modelled with our SC-STG model. The SC-STC model can help us to describe and explain the causality and concurrency relations in these designs. Figure 3.6 shows Voltage Doubler 2 and its control signals.

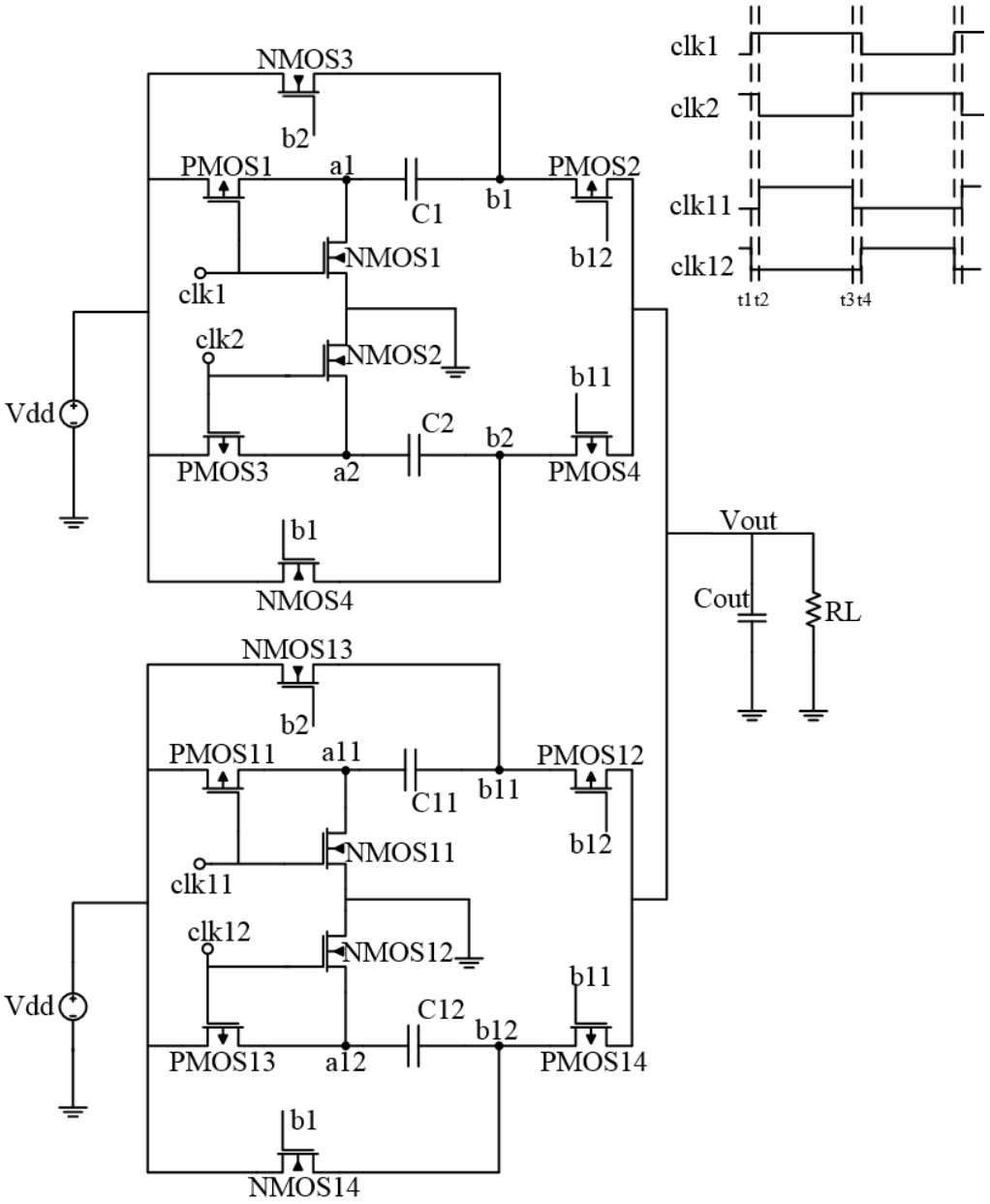


Figure 3.6: Schematic of Voltage Doubler 2.

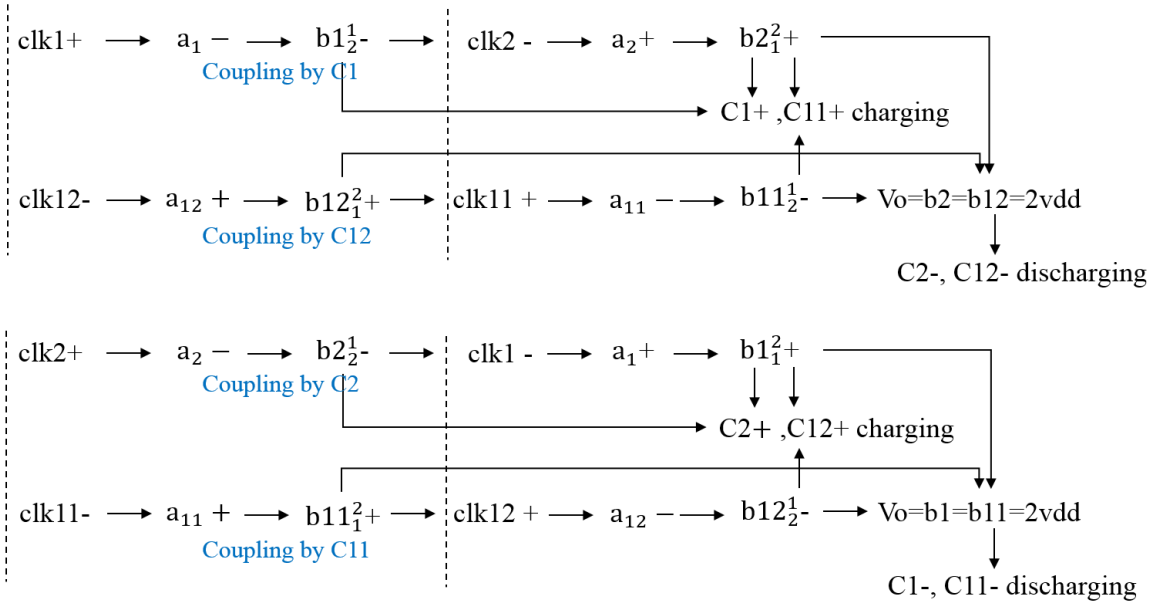


Figure 3.7: Flow chart of events happening in Voltage Doubler 2.

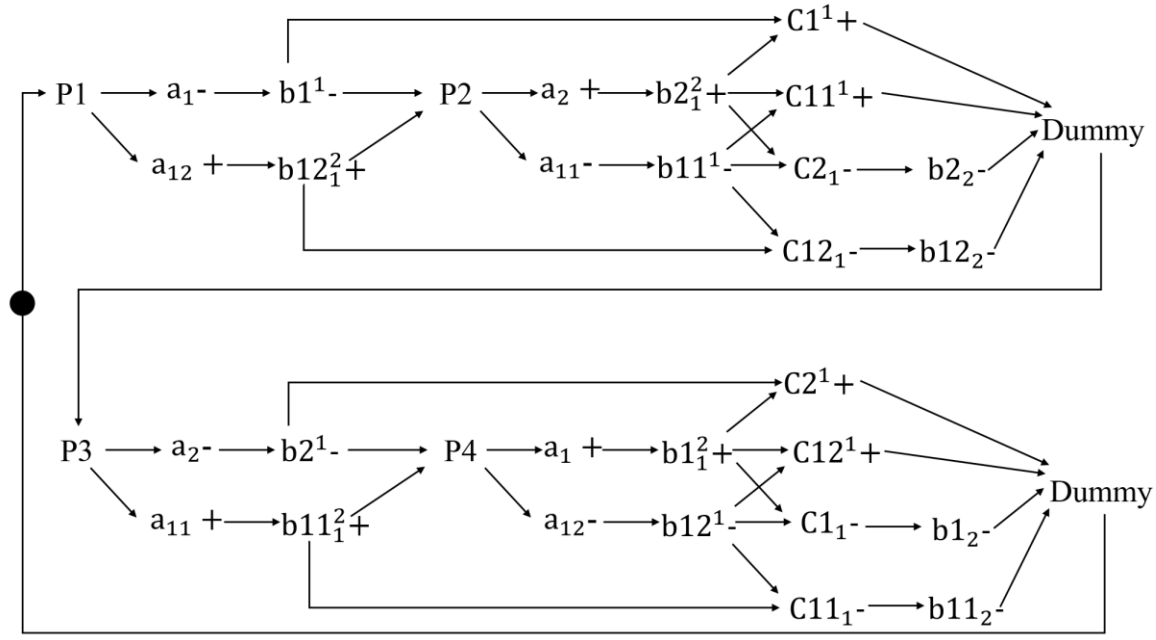


Figure 3.8: SC-STG for Voltage Doubler 2.

Table 3.3: Parts of representations in SC-STG of Voltage Doubler 2.

Notation	Meaning
$P1$	Phase transition including *clk1+* and *clk12-*
$P2$	Phase transition including *clk2-* and *clk11+*
$a1+$	Signal *a1* goes up from 0 to Vdd
$a1-$	Signal *a1* goes down from Vdd to 0
$a2+$	Signal *a2* goes up from 0 to Vdd
$a2-$	Signal *a2* goes down from Vdd to 0
$b1_1^2+$	Signal *b1* goes up from Vdd to 2Vdd
$b1_2-$	Signal *b1* goes down from 2Vdd
$b1^1-$	Signal *b1* goes down to Vdd
$b2_1^2+$	Signal *b2* goes up from Vdd to 2Vdd
$b2_2-$	Signal *b2* goes down from 2Vdd
$b2^1-$	Signal *b2* goes down to Vdd
$C1^1+$	Capacitor C1 charging to Vdd
$C1_1-$	Capacitor C1 discharging from Vdd
$C2^1+$	Capacitor C2 charging to Vdd
$C2_1-$	Capacitor C2 discharging from Vdd
Dummy	Dummy transition

Voltage Doubler 2 consists of two copies of the cross-coupled voltage doublers shown in Figure 3.2. The upper one is driven by overlapping clocks, while the lower one is driven with non-overlapping clocks. The concurrency and causality relations between transitions in Voltage Doubler 2 are described in the flow chart shown in Figure 3.7, which has been verified and confirmed by the simulated waveform.

Figure 3.8 shows the SC-STG for Voltage Doubler 2 drawn based on the relations shown in the flow chart. In this SC-STG, we define $P1 = clk1+ \cap clk12-$ since these two transitions happen together. Similarly, we have $P2 = clk2- \cap clk11+$, $P3 = clk2+ \cap clk11-$ and $P4 = clk1- \cap clk12+$.

In addition, *Dummy* is a dummy transition, which is definition adopted in STG. A dummy transition does not correspond to a signal event and does not change any values of the described system [96]. In this SC-STG, *Dummy* is only employed to simplify the SC-STG model so that several arcs can be omitted. Table 3.3 shows some representations in the SC-STG for Voltage Doubler 2.

All causality and concurrency relations between signal transitions in Voltage Doubler 2 are described in the SC-STG model. For example, after *P1* fires, *b1* goes to Vdd and *b12* goes to 2Vdd due to capacitor coupling effects. After *P2* fires, similarly, due to capacitor coupling effects, *b2* goes up to 2Vdd and *b11* goes down to Vdd. As a result, flying capacitors C11 and C1 are charged to Vdd and C2 and C12 charge the output to 2Vdd. Likewise, transitions due to capacitor coupling effects occur on internal signals *b1*, *b2*, *b11* and *b12* after *P3* and *P4* fire, and then flying capacitors C1, C2, C3 and C4 implement the related charging and discharging processes to maintain *Vout* = 2Vdd.

In summary, SC-STG models for these two cross-coupled voltage doublers show the causality and concurrency relations between signal transitions, which can help engineers and researchers understand and analyse these designs. In addition, we can have a simple comparison for the SC-STG model and the traditional description method of Charge Flow Analysis. The vectors used in Charge Flow Analysis to describe Voltage Doubler 1 and Voltage Doubler 2 are shown below.

Voltage Doubler 1:

$$a^1 = [1 \quad -1 \quad 1 \quad 2]$$

$$a^2 = [1 \quad 1 \quad -1 \quad 2]$$

Voltage Doubler 2:

$$a^1 = [1 \quad -1 \quad 1 \quad 1 \quad -1 \quad 2]$$

$$a^2 = [1 \quad 1 \quad -1 \quad -1 \quad 1 \quad 2]$$

These vectors describe the charge and discharge state for each capacitor in different phases. However, they do not show enough details about how these capacitors get charged and the relations between signal transitions in SCDDCs. SC-STG models for SCDDCs illustrate these concurrency and causality relations between signals, which Charge Flow Analysis cannot do.

In addition, comparing SC-STG shown in Figure 3.8 with the STG shown in Figure 3.5, one can find that signals connected to MOS devices will not transit at the same time during all phases, which means there is no shoot-through current in the second cross-coupled voltage doubler. However, these descriptions in the SC-STG model are not direct.

Consequently, supporting further analysis or verifications for the shoot-through current as well as other reversion losses introduced in Chapter 2 is not a straightforward process.

There are two limitations of the SC-STG in analysing and verifying reversion losses in cross-coupled voltage doublers. Firstly, SC-STG can only model cross-coupled voltage doublers driven by dedicated clock signals, where the existence of reversion losses is unknown when the cross-coupled voltage doubler is driven by other clock signals. Secondly, as can be seen from all the SC-STGs above, the description of reversion losses is not apparent and direct, since there is no sign indicating the occurrence of reversion losses. However, these causality and concurrency relations described in SC-STG can be extended to other discrete event models to analyse and verify reversion losses in SCDDCs, assisting researchers or engineers in verification or design of SCDDCs. These new modelling methods for reversion losses are introduced in Chapter 4.

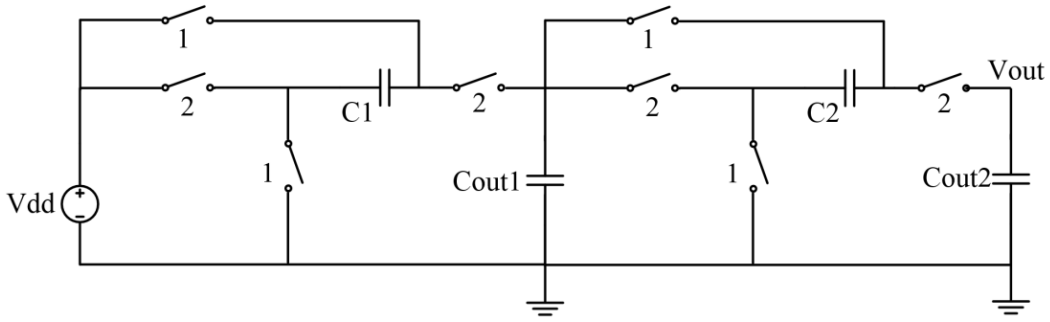
3.4 STG for SCDDCs with different topologies

In this section, the SC-STG method is applied to model more SCDDCs with different topologies including a multi-stage doubler, Ladder and Fibonacci Multiplier, all of which have been introduced in Chapter 2. VCRs of these SCDDCs are different. SC-STGs for these SCDDCs show details about how these SCDDCs achieve different VCRs.

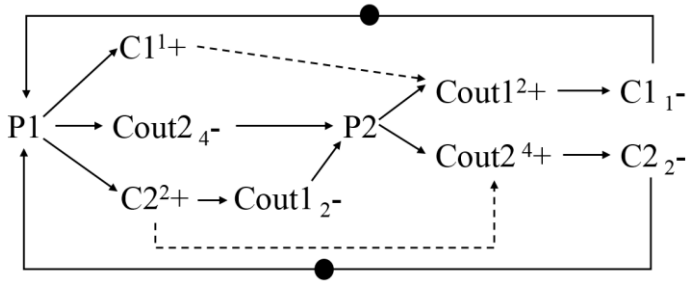
For simplicity, the models of all these converters assume ideal switches ignoring their thresholds and resistances. This does not affect the generality of SC-STG representation, as SC-STGs can represent sets of arbitrary voltage levels, and transistor thresholds usually do not have an infinitely large number of possible values in a single system. As these SCDDCs are also controlled by two synchronous clock signals as shown in Figure 2.3, phase shift transitions are also adopted in their SC-STG models, including $P1 = clk1 + \cap clk2 -$ and $P2 = clk1 - \cap clk2 +$.

Case 1: Two-stage doubler

A two-stage voltage doubler and its SC-STG model are shown in Figure 3.9. It has a VCR of 4.



(a) Two-stage voltage doubler



(b) SC-STG

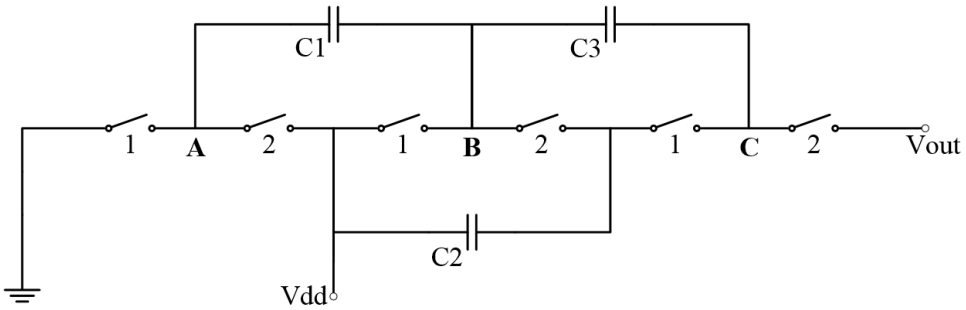
Figure 3.9: Two-stage voltage doubler and its SC-STG model.

The SC-STG model describes the operating principles of the two-stage voltage doubler clearly. We can find that after *P1* happens, C1 is charged to Vdd, which will make Cout1 rise to 2Vdd in the next phase. Meanwhile, C2 is charged to 2Vdd, which will also make Cout2 rise to 4Vdd in the next phase.

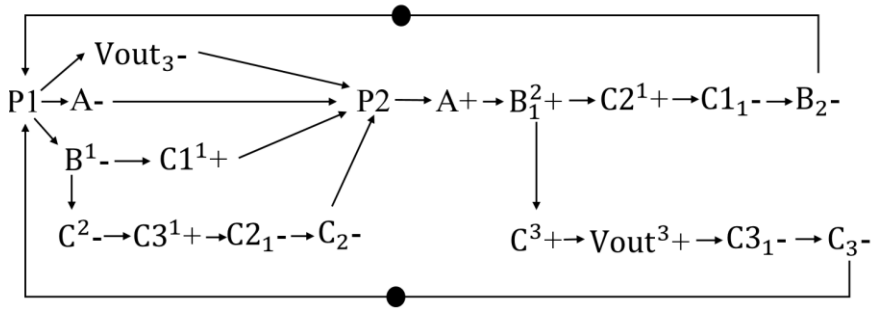
Internal signals are not included in the SC-STG in Figure 3.9 because of the straightforward relations among signals. Other SCDDCs with more complex topologies require internal signals to describe their causality relationships inside, but this is not the case here.

Case 2: Ladder

A Ladder with a VCR of 3 and its SC-STG model are shown in Figure 3.10, where three internal node signals *A*, *B* and *C* need to be represented.



(a) Ladder



(b) SC-STG

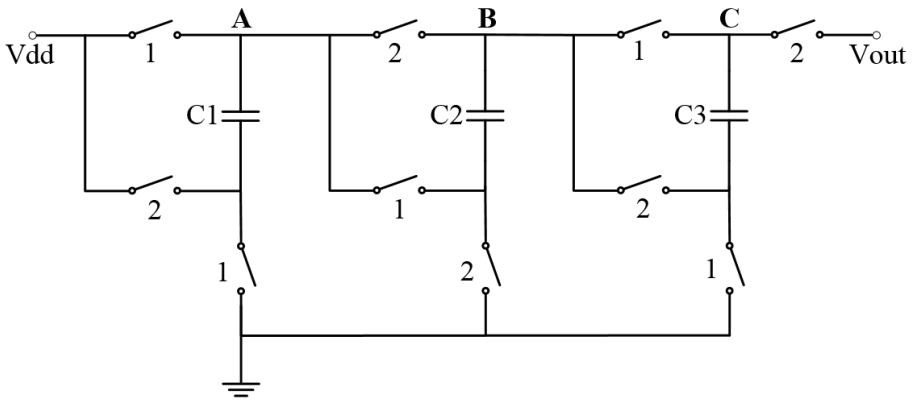
Figure 3.10: Ladder with a VCR of 3 and its SC-STG model.

Based on the SC-STG, we can find after *P1* fires internal signal *A* is connected to the ground, *B* is connected to Vdd and then capacitor C1 is charged to Vdd. At the same time, as C2 was charged to Vdd in the previous phase and *B* is Vdd, *C* goes down from 3Vdd to 2Vdd because of a capacitor coupling effect, charging C3 to Vdd. After *P2* happens, *B* is boosted up to 2Vdd due to a capacitor coupling effect. As a result, capacitor C2 is charged to Vdd. Meanwhile, *C* goes up to 3Vdd because of a capacitor coupling effect, charging the output Vout to 3Vdd.

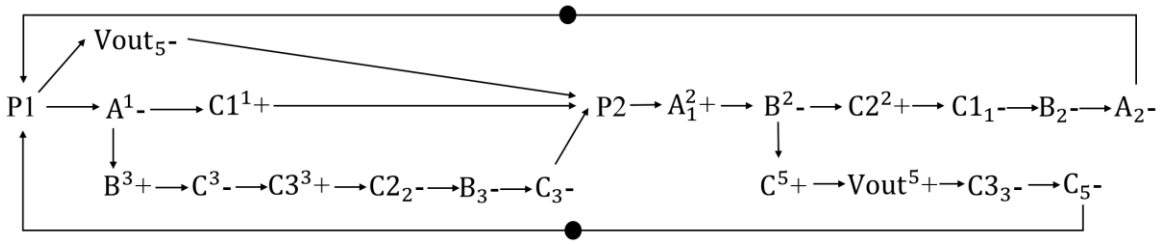
With the representation of internal signals, the causality relations between phase transitions and capacitor transitions in such a converter with complex topology are shown in more detail. For example, C1 getting charged to Vdd is because internal node *B* fell from 2Vdd to Vdd rather than only because *P1* fired.

Case 3: Fibonacci Multiplier

A Fibonacci Multiplier with a VCR of 5 and its SC-STG model are shown in Figure 3.11, where three internal node signals *A*, *B*, *C* are monitored.



(a) Fibonacci multiplier



(b) SC-STG

Figure 3.11: Fibonacci Multiplier with a VCR of 5 and its SC-STG.

Based on the SC-STG model, we can easily understand the working principle of this multiplier: After *P1* fires, C1 is charged to Vdd because *A* is connected to Vdd while it was 2Vdd in the last phase. Meanwhile, C3 is charged to 3Vdd as *C* goes down from 5Vdd to 3Vdd. After *P2* is fired, A goes up from Vdd to 2Vdd due to a capacitor coupling effect, *B* goes down to 2Vdd as *A* is connected to *B* and C2 is charged to 2Vdd. In a similar way, internal signal *C* goes up to 5Vdd and the output Vout is charged to 5Vdd.

In summary, VCRs of these three SCDDCs are different due to the different charging and discharging events happening in the different phases. Their SC-STGs describe the causal and concurrency relationships among the SCDDCs' signals, showing the difference between these SCDDCs. Modelling SCDDCs formally with SC-STGs allows all simple and complex converters to be analysed in a straightforward manner.

3.5 Summary

This chapter presents a new modelling method for SCDDCs by using SC-STG. The new SC-STG models may be used in studying larger systems containing complicated SCDDCs

with arbitrary numbers of stable voltage values across capacitors and at signal nodes, helping the analysis and design of such systems.

In this chapter, two cross-coupled voltage doublers and three other SCDDCs with different topologies are modelled with SC-STGs, and the causality and concurrency relations among signals in these SCDDCs are fully described and clearly analysed. These examples demonstrate that the new modelling approach provides a formalised way to study discrete events and their relationships in SCDDCs, which helps to avoid the potential confusion of using natural language intuition with waveform only.

At the same time, from the STG models for the two types of cross-coupled voltage doublers, we can see that SC-STG is not able to describe reversion losses in SCDDCs clearly and may require further complications if used for the analysis of reversion losses. In the next chapter, a new type of modelling method using Petri nets is proposed to describe the reversion losses in SCDDCs and to further analyse them. It may be seen as a further development of the paradigm of representing discrete events using Petri net type languages first proposed in this chapter.

Chapter 4
Modelling and Analysing Reversion Losses in SCDDCs with Petri Nets

4.1 Introduction

As discussed in Chapter 2, reversion losses in SCDDCs happen when NMOS or PMOS switches are turned on undesirably under certain internal signal combinations. For example, when Voltage Doubler 1 shown in Figure 2.9 is driven by non-overlapping clocks, reversion losses occur from flying capacitors to the voltage source Vdd (known as pump losses). On the other hand, reversion losses from the output to flying capacitors (known as output losses) occur when this cross-coupled voltage doubler is driven by overlapping clocks. These reversion losses result in voltage drops for flying capacitors and the output and backward flows of energy, which will cause power and energy efficiency degradation for SCDDCs. Therefore, it is important to analyse and if possible eliminate these potential reversion losses in SCDDCs.

To eliminate the reversion loss, literature title [18] proposed an improved cross-coupled voltage doubler (referred to as Voltage Doubler 2 in this thesis) that attempts to eliminate reversion losses by adding an extra branch to the cross-coupled voltage doubler with a further cross-coupled technique. In this design, one branch of the cross-coupled voltage doubler is driven with overlapping clocks and the other is driven with non-overlapping clocks. Reversion losses generated in each branch are blocked by the internal signals from the other branch. However, transitions of the overlapping clocks and non-overlapping clocks for Voltage Doubler 2 have to be synchronised. If clock mismatch due to clock skew

or clock jitter happens, Voltage Doubler 2 may suffer from reversion losses. To eliminate reversion losses as well as to avoid timing mismatch problems, [40]-[42] proposed reversion-loss-free cross-coupled voltage doubler designs with relaxed clock timing restrictions by employing extra blocking transistors, and [43]-[50] proposed different reversion-loss-free designs by introducing fixed external control signals. Among all reversion-loss-free designs with these two types of techniques, Voltage Doubler 3 in [40] adopting the first technique and Voltage Doubler 4 in [47] employing the second technique are good exemplars of power conversion performance and power efficiency. They have been reviewed and intuitively analysed in Subsection 2.2.3. However, all these works describe and analyse reversion losses by natural language descriptions, intuitive diagrams and verbal reasoning. They do not provide a formal way to verify and detect reversion losses to support computer-aided design and verification of complex SCDDC architectures.

In Chapter 3, Voltage Doubler 1 and Voltage Doubler 2 have been modelled with SC-STG, which aims to formally describe discrete events and relations between these events. However, as discussed in Section 3.3, SC-STG aims to model an SCDDC driven by a dedicated clock signal, where the existence of reversion losses is unknown when the cross-coupled voltage doubler is driven by other control signals. Also, SC-STG models do not have direct representations of the causes and existence of reversion loss.

Therefore, this chapter presents a new modelling method that models reversion losses in SCDDCs with Petri nets. Petri net models for reversion losses are developed to model the reversion losses in an SCDDC when it is driven by different control signals rather than only a dedicated one. At the same time, the Petri net model directly represents the occurrence of reversion losses. In the Petri net model, level changes are also represented as transitions. Explicit places are added to represent signal values, the combinations of which may indicate reversion losses. Monitoring sub-nets for reversion losses can then be constructed to record the occasions when these combinations of signal value states happen. With a reachability analysis, the model only needs to provide for the possibility of monitoring places becoming marked if reversion losses happen. Another important reason why we model reversion losses with the Petri net model rather than SC-STG is the support of the tools. The multi-value transitions in SC-STG are not supported in commonly available tools such as Workcraft so far. In Petri net model, we do not focus on the multiple voltage levels such as 2Vdd and Vdd when studying reversion loss, it is not necessary to explicitly differentiate the different types of + and – signals as in SC-STG. As a result SC-STG

models do not offer practical advantages over Petri net models and the latter are easier to use for reversion loss analysis.

The Petri net model will provide researchers and engineers with a formal way to analyse reversion losses and their causes in SCDDCs, which is especially important for SCDDCs of larger size and higher complexity. Firstly, the Petri net models for SCDDCs also have the capability of describing the causality and concurrency relations between events in a formal way. Secondly, the Petri net model for an SCDDC presents a systematic and efficient way to verify and detect reversion losses. These models can be used for analysis supported by the rich set of tools such as Workcraft, the use of which may facilitate the design flow for SCDDCs in the next step.

This chapter is organised as follows: Section 4.2 introduces the modelling method. Section 4.3 presents two modelling examples of two cross-coupled voltage doublers (Voltage Doubler 1 and Voltage Doubler 2) that have been introduced and studied in previous chapters. Section 4.4 contains comparisons and analyses of these two cross-coupled voltage doublers based on the results of reachability analysis. Section 4.5 analyses other cross-coupled voltage doubler designs (Voltage Doubler 3 and Voltage Doubler 4) with corresponding Petri net models.

Some schematics and SC-STGs of SCDDCs that have been shown and reviewed in previous chapters are reused in this chapter for the completeness of the modelling work as well as for easy comprehension.

The work presented in this chapter was partly published in [95].

4.2 Modelling method

The method of modelling SCDDCs with Petri nets is extended from the SC-STG, so that the causality and concurrency relations between transitions can be obtained from the SC-STG with some modifications. At the same time, there are some differences between the SC-STG model and the Petri net model such as the representations of transitions.

In this section, the definitions and related representations about modelling reversion losses with Petri nets are introduced first, before the general modelling method is presented.

Definition

The Petri net model for reversion losses in SCDDC adopts the definition of conventional Petri nets. A Petri net structure C is a tuple $C = \langle P, T, F, M_0 \rangle$, where P is a set of places, T is a finite set of transitions, F is the flow relation between place P and transition T and is M_0 is the initial marking.

The basic Petri net view of a system focuses on two primitives, including events and conditions [60]. Events are actions taking place in the system and conditions describe the state of the system, which are represented as transitions and places in a Petri net graph. In a Petri net graph modelling the reversion losses in SCDDC, signal transitions, charging and discharging processes of capacitors and revision losses are represented as transitions and places, the details of which are introduced as follows.

Signal transitions

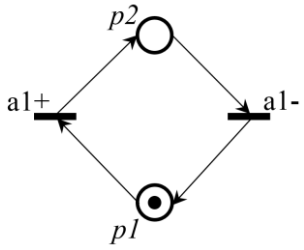


Figure 4.1: Petri net modelling example of transitions *a1+* and *a1-*.

Signal transitions are typical discrete events happening in SCDDCs, which change the value of signals. It is easy to describe signal transitions with Petri nets by following the traditional Petri net modelling method. Figure 4.1 shows a Petri net example that describes the signal transitions of *a1* between 0 and Vdd. The token in place *p1* means the current value of *a1* is 0. It also indicates that the transition *a1+* is enabled, which may fire in the future. When transition *a1+* fires, the token in *p1* is consumed and a token is produced in place *p2* to indicate that the value of *a1* has changed from 0 to Vdd.

Reversion loss

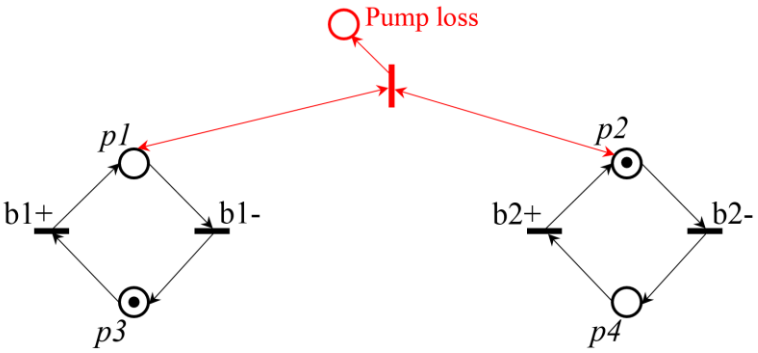


Figure 4.2: Petri net modelling example of monitoring sub-nets for reversion loss.

Reversion losses may be represented as places. Reversion losses may happen when the place of reversion loss is marked. Using this representation, the eventuality of reversion losses happening in an SCDDC is modelled as a question as to whether the place of reversion losses can be marked in the Petri net model, which is indeed a question of reachability analysis for a place.

The sub-net shown in red in Figure 4.2 is used to monitor pump losses. The sub-net includes one transition and one place. The transition means the occurrence of the pump loss and the place of *pump loss* will be marked if the transition is fired. The transition is connected to the place of *pump loss* with a normal arc while connected to place *p1* and *p2* with a bi-direction arc. The bi-direction arcs only read the states of *p1* and *p2* and will not consume the token in *p1* or *p2*. These arcs are referred as to read-arcs [96]. When there are tokens in *p1* and *p2*, the place of reversion loss will be marked and the token in *p1* and *p2* will not be consumed until the next transitions of *b1* or *b2*. As places *p1* and *p2* represent, *b1* is 2Vdd and *b2* is 2Vdd, and the sub-nets mean that pump losses may happen when both *b1* and *b2* are 2Vdd.

It is noteworthy that these monitoring sub-nets are used to facilitate a direct evidence of the reversion losses and for manual reachability analysis or for explanatory purposes. They are not necessary for finding reversion loss conditions which can be recorded by the simultaneous marking of relevant places that the monitoring sub-net transition depends on, and the related reachability analysis can also be run in tools automatically without these monitoring sub-nets so long as the relevant markings are recorded properly. For example, in Petri net tool Workcraft, verifying reversion losses as described in Figure 4.2 only needs to run reachability analysis for simultaneous tokens in places *p1* and *p2*. The addition of

monitoring sub-nets may bring deadlock problems to the models in some complex cases, as a result, it is a good idea to have these monitoring sub-nets only for illustration purposes and manual Petri net animations, but to stick to basic models without monitoring sub-nets in the computer-aided analysis.

Modelling method

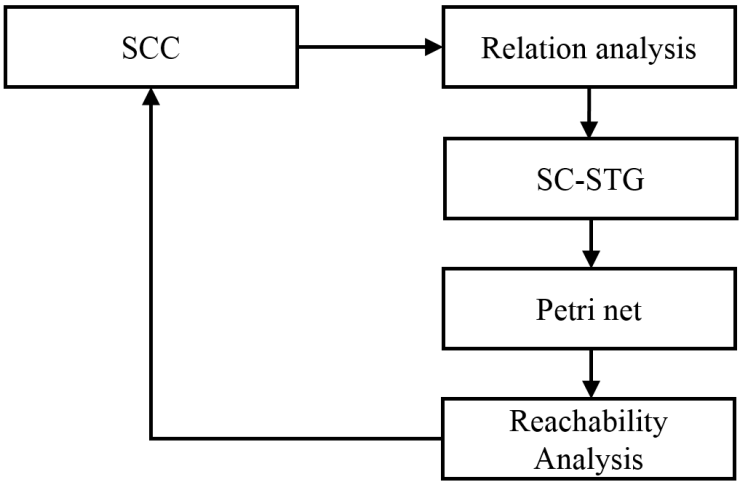


Figure 4.3: Flow chart of modelling reversion losses in SCDDCs.

The method of modelling reversion losses in SCDDC is illustrated in Figure 4.3. An SC-STG model of the concurrency and causality relations in an SCDDC can firstly be derived from the SCDDC study, with which an understanding of the crucial factors that affect the charging and discharging processes for flying capacitors is obtained. As discussed in Chapter 3, these causality and concurrency relations can be verified by SCDDC simulations or other types of experimental studies. With certain steps, the Petri nets model can be developed based on the concurrency and causality relations described in SC-STG, which are introduced in the next subsection. Finally, with reachability analyses for these models, control signals that enable or do not enable reversion losses can be verified and investigated, which will be helpful for the analysis and design of SCDDCs. Reachability analysis can also be employed to examine reversion losses caused by other clock problems like clock skew or clock jitter. The reachability analysis can be carried out using facilities provided by Petri net tools such as Workcraft, which is a significantly more useful process than the intuitive verbal reasoning found in existing SCDDC reversion loss research. These verbal reasoning attempts are effectively trying to analyse the state space without a rigorous mathematical model or even a formal definition of the states.

Develop a Petri net model based on SC-STG

As the Petri net model is developed to analyse reversion losses in an SCDDC when it is driven by different control signals instead of a dedicated one in SC-STG, it is not convenient to directly convert a SC-STG model to a Petri net model. However, the concurrency and causality relations in the Petri net model can be inherited from the SC-STG and a Petri net model can be developed based on SC-STG. Details of the steps are shown in Figure 4.4.

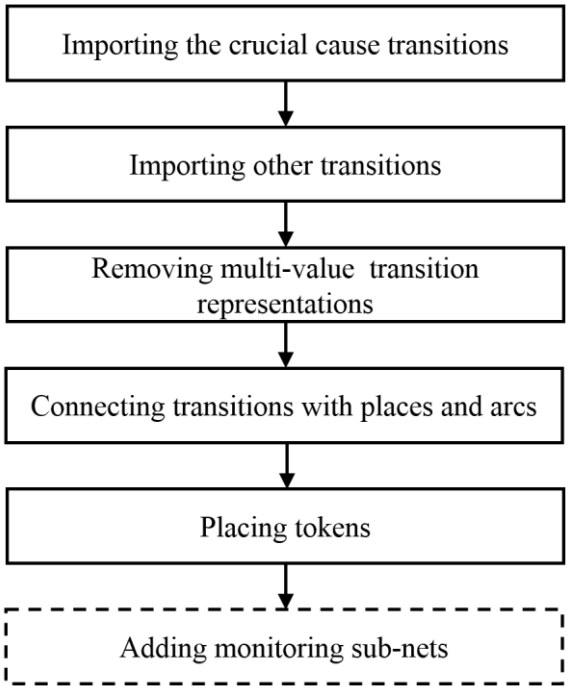


Figure 4.4: Steps of developing a Petri net model based on SC-STG.

Always as the first step is isolating and importing the crucial transitions that are the direct causes of the reversion losses. As analysed in Section 2.2.2, the direct cause of these reversion losses is the dedicated signals connected to the MOS switches where the reversion losses happen. The second step is, based on the concurrency and causality relations in SC-STG, finding and adding the cause transitions of these crucial transitions and then adding the causes of these found transitions again until the control signals are added. Note that as phase transitions are used in some SC-STG, the causality relations between control signals included in the phase transitions and other transitions should be carefully analysed. The third step is removing explicit multiple voltage level representations for all transitions as they are not essential for the reversion loss modelling in Petri nets. The next step is connecting all transitions obtained with places and arcs to construct a basic structure of

Petri nets, where the concurrency and causality relations corresponds with the SC-STG model. Meanwhile, we also need to add arcs and places to the + and - transitions for the same signal to create a full Boolean value loop. The places in the loop represent different states of a signal. These loops do not exist in the SC-STG model, the presence of which in Petri nets helps to describe the SCDDC when it is driven by different control schemes. The fifth step is placing the initial condition tokens, which represents the current states of signals, determining the enabled transitions. The tokens of the control signals can be placed by following the placements of tokens in SC-STG. The placement of other tokens needs to be carefully analysed as well, e.g. observing which transitions will be enabled by the firing of the control signals. And the final step (optional) is adding monitoring sub-nets and connecting them to the cause signal value combinations of the reversion losses, which helps when trying to identify reversion losses by animating the Petri nets manually.

4.3 Examples

Two examples of cross-coupled voltage doublers are modelled with Petri nets in this section. These two cross-coupled voltage doublers have already been studied in Chapter 2 and modelled with SC-STG in Chapter 3. The work presented in this chapter continues the modelling work carried out in Section 3.3.

Petri net Model for Voltage Doubler 1

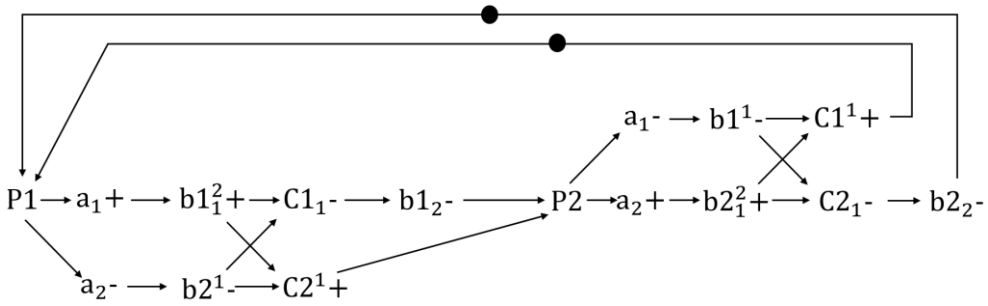


Figure 4.5: SC-STG for Voltage Doubler 1.

In the previous chapter, an SC-STG model for Voltage Doubler 1 was obtained, as shown in Figure 4.5. The concurrency and causality relations between signal transitions and capacitor charging and discharging processes have been illustrated clearly. In the first phase (after *P1* fired) flying capacitor C2 is charging and C1 is discharging, since *b1* is 2Vdd and *b2* is Vdd, and flying capacitor C1 is charging and C2 is discharging as b2 is 2Vdd and *b1*

is Vdd in the second phase (after *P2* fired). Based on the modelling method presented in Section 4.2, a Petri net model for the reversion loss can be developed, which is shown in Figure 4.6.

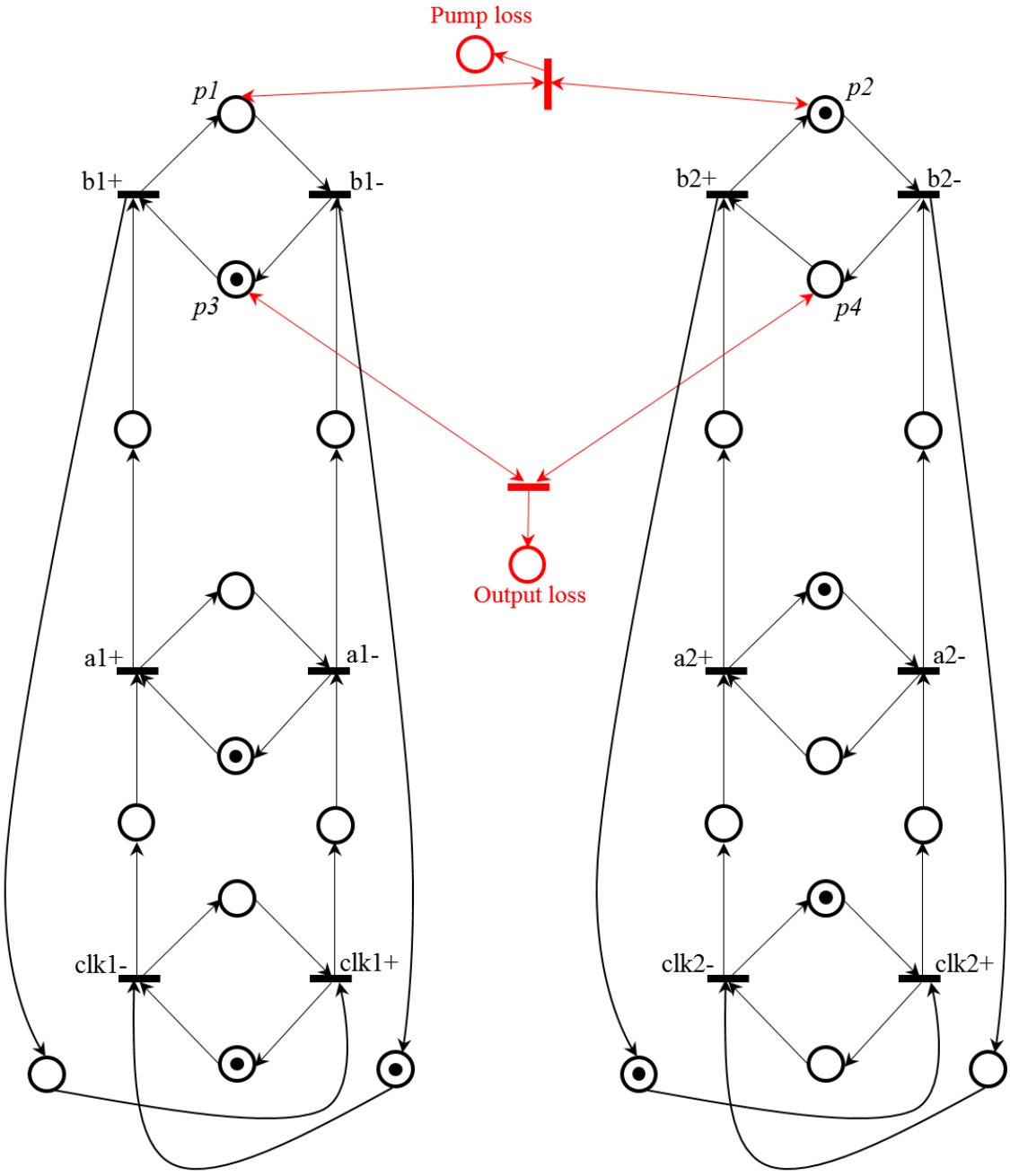


Figure 4.6: Petri net model for reversion losses in Voltage Doubler 1.

In Figure 4.6, the causality and concurrency relations between transitions are obtained from its SC-STG model. For example, control signal *clk1-* causes *a1* to transit from 0 to Vdd, finally resulting in *b1* going up from Vdd to 2Vdd. This Petri net model also shows these causality relations among the reversion losses and internal signals. For example, in this model, we can find that the transition *Pump loss* may fire if there are tokens in places *p1* and *p2* at the same time, which means reversion losses from capacitor C1 and C2 to Vdd may occur when both *b1* and *b2* are 2Vdd. At the same time, the transition *Output loss* may fire when there are tokens in places *p3* and *p4*, which means reversion losses from the output Vout to the capacitor C1 and C2 happen when both *b1* and *b2* signals are Vdd. Based on the causality relations shown in this Petri net model, all the control signals that may trigger reversion losses can be traced by using reachability analysis. The corresponding reachability analysis results will be shown and discussed in Section 4.4.

It is noteworthy that if the model is animated/simulated, not every occurrence of simultaneous marking of *p1* and *p2* would cause a firing of transition Pump loss. This is not a problem for a Petri net model designed for reachability analysis. A reachability analysis finds traces to all reachable states and answers the qualitative questions of whether reversion losses exist, and if so, what their causes are. The fact that this model also includes reachable states indicating monitoring failure is not an issue. This is fundamentally different from models targeting simulation studies, where the designer may want to have 100% monitoring success in every run. That will require a more complex monitoring sub-net and is outside the scope of this thesis.

Petri net model for Voltage Doubler 2

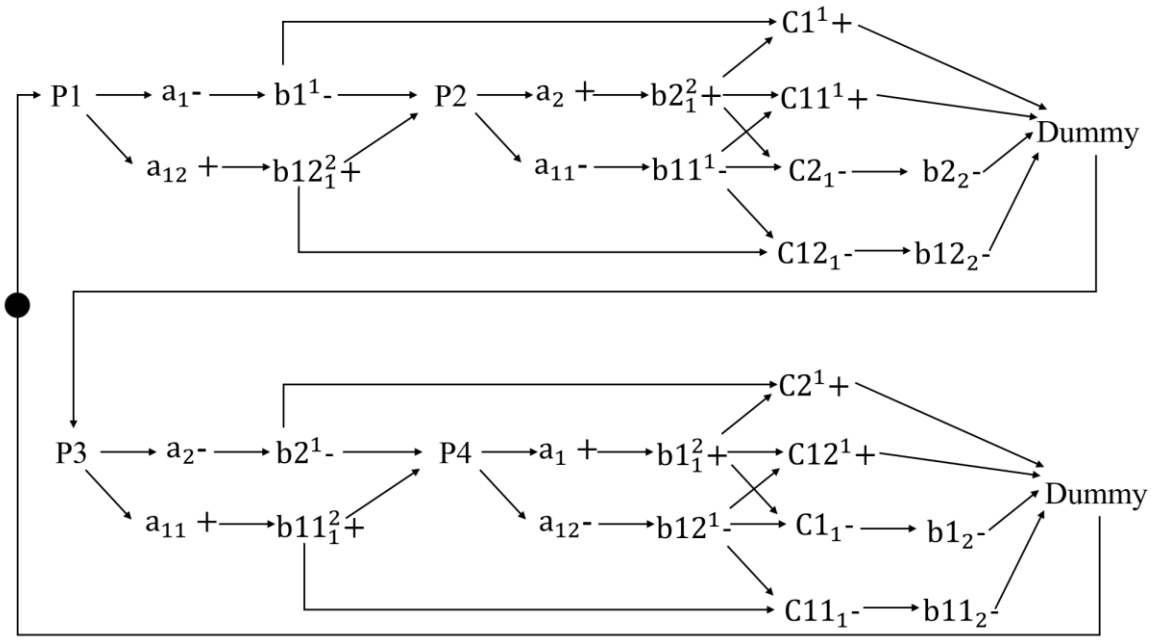


Figure 4.7: SC-STG model for Voltage Doubler 2.

In Voltage Doubler 2, pump losses from flying capacitors to Vdd happen in one of the following cases: both *b1* and *b2* are at 2Vdd, both *b1* and *b12* are at 2Vdd and both *b2* and *b11* are at 2Vdd. Output losses from output to flying capacitors happen in one of the following cases: both *b11* and *b12* are at Vdd, both *b1* and *b12* are at Vdd and both *b2* and *b11* are at Vdd. Figure 4.7 shows the SC-STG model for Voltage Doubler 2. Based on the concurrency and causality relations shown in this SC-STG, the Petri net model for the reversion losses of this cross-coupled voltage doubler is drawn as shown in Figure 4.8.

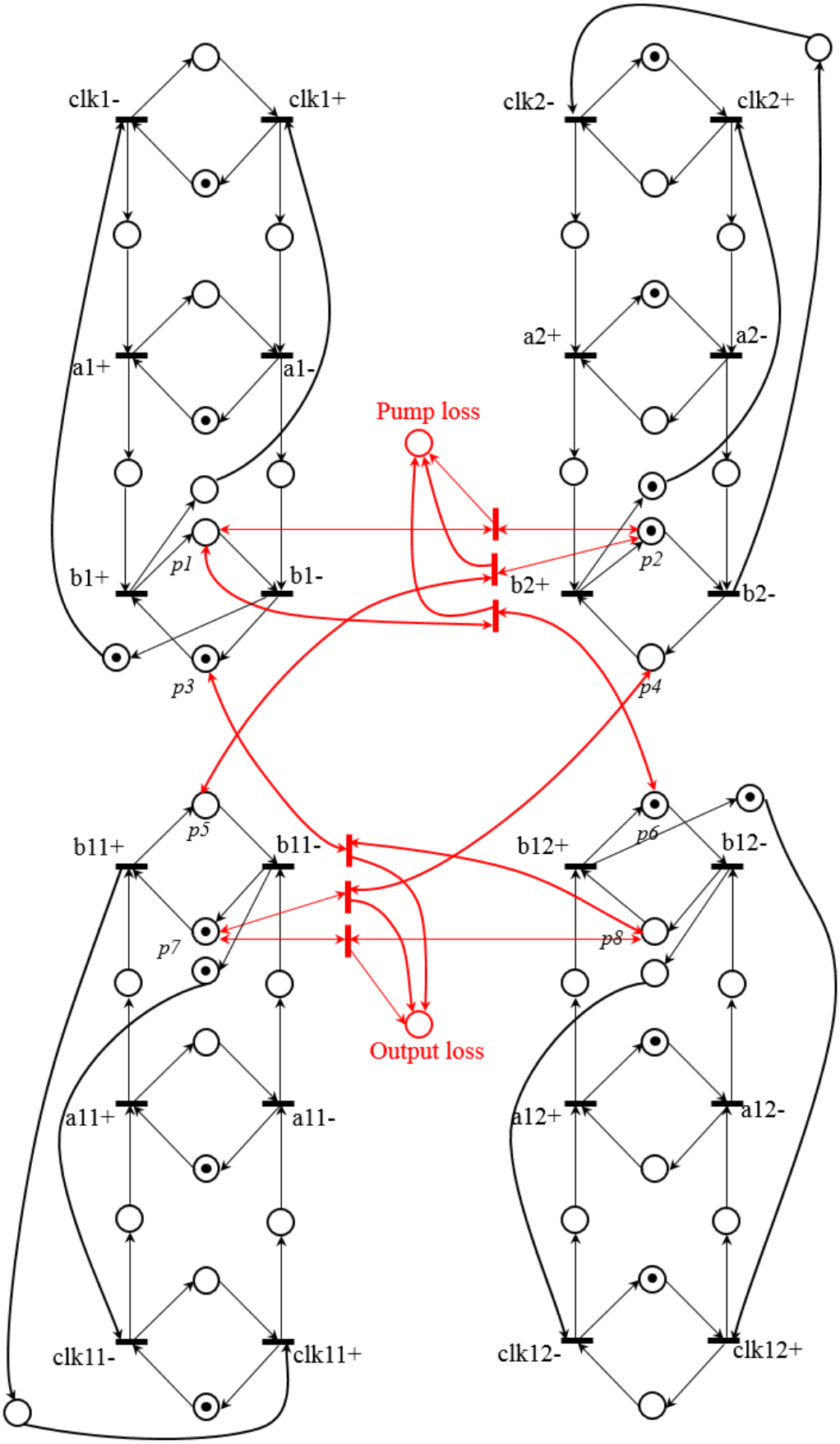


Figure 4.8: Petri net model for the reversion losses in Voltage Doubler 2.

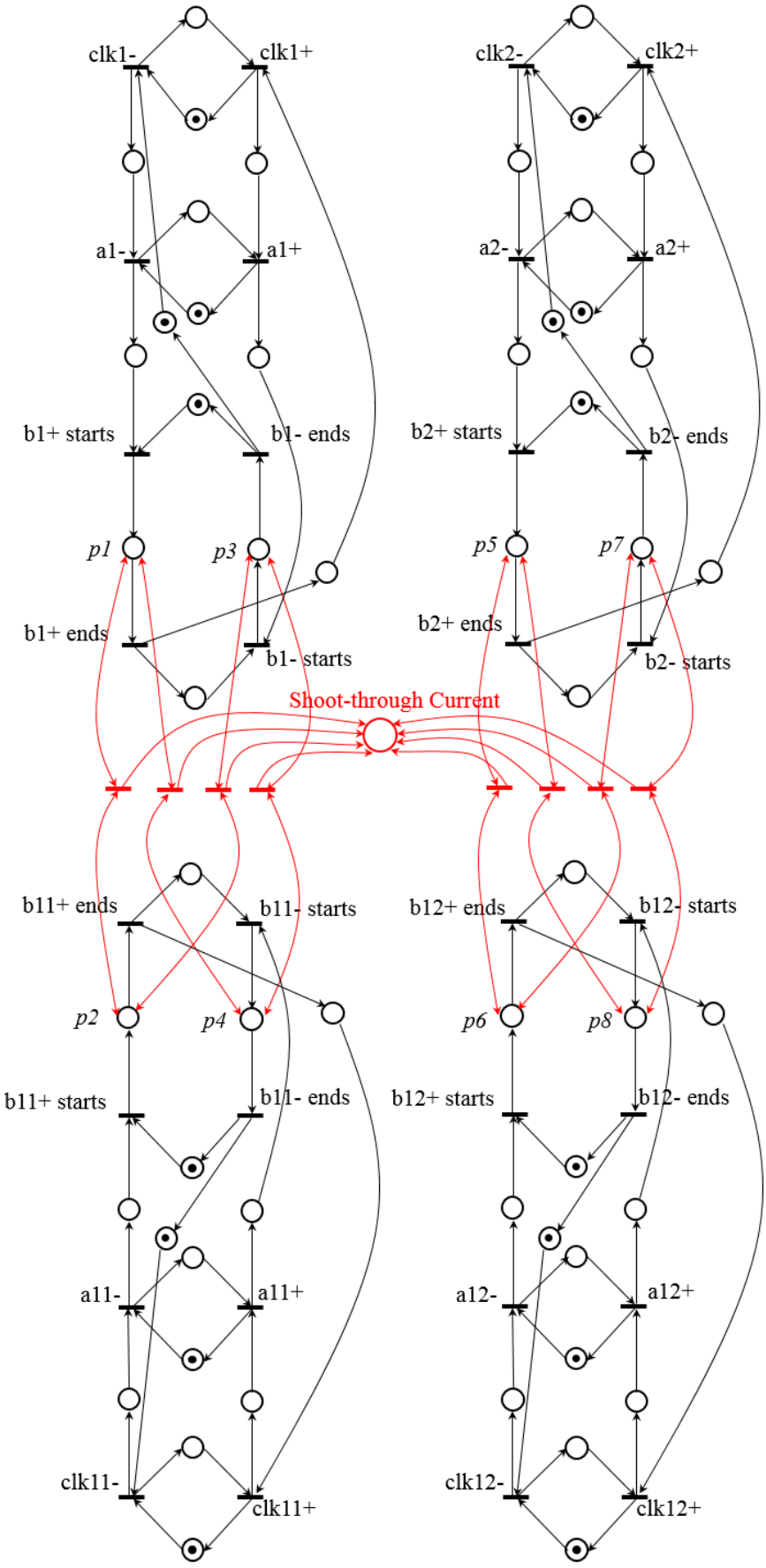


Figure 4.9: Petri net model for shoot-through currents in Voltage Doubler 2.

The Petri net model shown in Figure 4.8 shows the concurrency and causality relations among internal signals and reversion losses. For instance, when there are tokens in *p1* and *p2*, the transition *Pump loss* may fire, as reversion losses from capacitor C1 and C2 to Vdd may occur when both *b1* and *b2* are 2Vdd. Similarly, the transition *Output loss* may fire if there are tokens in places, since *p7* and *p8* since there may be reversion losses from the output Vout to the capacitors C11 and C12 when *b11* and *b12* are both Vdd.

Compared with Voltage Doubler 1, Voltage Doubler 2 claims to eliminate shoot-through currents when these two voltage doublers are driven with non-synchronised clocks (as analysed and verified in the next section). Shoot-though currents can also be modelled with Petri nets. But this requires a further extension of the Petri net model. The Petri net model for shoot-through currents in Voltage Doubler 2 is shown in Figure 4.9.

In the Petri net model for shoot-through current, the value changes of internal signals *b1*, *b2*, *b11* and *b12* are represented by two transitions and one place, where the two transitions represent the start and end of the value change and the place represents the relevant value being changed. This is because to check for shoot-through currents, we must modify the model by viewing the change processes of related signals as non-atomic to find the simultaneous conduction of two switches, which happens when both signals are in transit at the same time. The causality and concurrency relations can also be obtained from the SC-STG. In this way, control schemes that lead to shoot-through currents can also be determined using a reachability analysis.

In the Petri net model shown in Figure 4.9, the causality relations between the internal signals and the shoot-through current monitoring are described clearly. Taking a simple example, when there is a token pair in any of the following pairs of places, (*p1, p2*), (*p1, p4*), (*p3, p2*) or (*p3, p4*), the place for monitoring shoot-through currents may get marked. It means that shoot-through currents occur when internal signals *b1* and *b11* transit at the same time as the token in places *p1* or p2. The same arguments lead to the other pairs of places being monitored in the same way.

In summary, Petri net models for these cross-coupled voltage doublers represent the relations between transitions and reversion losses, providing a formal way to describe reversion losses in these cross-coupled voltage doublers. Most importantly, using a reachability analysis, control signals causing reversion losses can be determined and

verified. The related reachability analysis and further analysis for these Petri net models are presented in Section 4.4.

4.4 Analysis and verification

Reachability analysis for the Petri net model can be run in Workcraft, which is a tool for the development of interpreted models such as Petri nets and STGs, including visual editing, simulation and analysis. For any Petri net models, Workcraft not only can run any specific reachability analysis automatically or manually but also can provide a verification such as deadlock freeness.

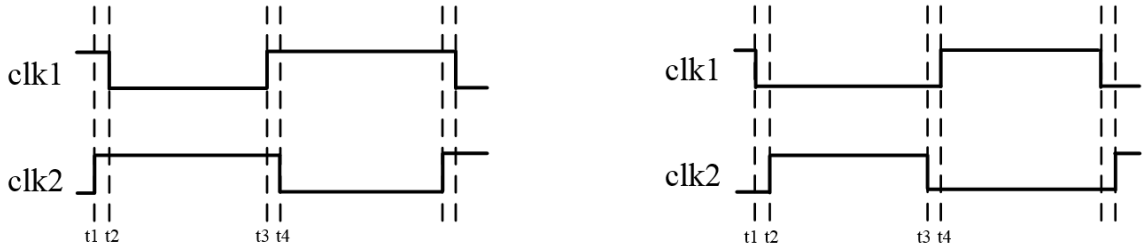
In the Workcraft, reachability analysis can be implemented by Reach Language [71] in Workcraft (the monitoring sub-nets are not required). However, reachability analysis for Petri nets modelling reversion losses is currently partly compatible with Workcraft. For example, Workcraft does not support the synchronous signal transitions (signal transitions happen at the same time). For some specified cases such as the determination of the healthy controls, the related reachability analysis should be carried out manually in Workcraft (sub-nets are still required).

In this section, the results of reachability analysis for the Petri net models shown in Section 4.3 is presented. Moreover, the cross-coupled voltage doublers are further analysed based on the results of reachability analysis. In [18], Voltage Doubler 2 was proposed to eliminate pump losses and output losses. However, as stated earlier, what Voltage Doubler 2 eliminates is the shoot-through current rather than pump loss and output loss, which will also be verified based on the result of reachability analysis in this section.

Results for Voltage Doubler 1

Table 4.1: Results of reachability analysis for Voltage Doubler 1.

	Control scheme	Output loss	Pump loss
1	*clk1-,clk1+,clk1-,clk1+*	No	Yes
2	*clk1-,clk1+,clk1-,clk2+*	No	Yes
3	*clk1-,clk1+,clk2+,clk2-*	Yes	Yes
4	*clk1-,clk1+,clk2+,clk1-*	Yes	Yes
5	*clk1-,clk2+,clk1+,clk1-*	Yes	Yes
6	*clk1-,clk2+,clk2-,clk1+*	Yes	Yes
7	*clk1-,clk2+,clk2-,clk1+*	No	Yes
8	*clk1-,clk2+,clk2-,clk2+*	No	Yes
9	*clk2+,clk2-,clk2+,clk2-*	Yes	No
10	*clk2+,clk2-,clk2+,clk1-*	Yes	No
11	*clk2+,clk2-,clk1-,clk1+*	Yes	Yes
12	*clk2+,clk2-,clk1-,clk2+*	Yes	Yes
13	*clk2+,clk1-,clk2-,clk1+*	Yes	Yes
14	*clk2+,clk1-,clk2-,clk2+*	Yes	Yes
15	*clk2+,clk1-,clk1+,clk2-*	Yes	No
16	*clk2+,clk1-,clk1+,clk1-*	Yes	No
17	(*clk1-, clk2+*), (*clk1+, clk2-*), (*clk1-, clk2+*), (*clk1+, clk2-*)	No	No



(a) Overlapping clock (b) Non-overlapping clock

Figure 4.10: Overlapping clock signals and non-overlapping clock signals.

Table 4.1 illustrates reachability analysis results of the Petri net model shown in Figure 4.6. Since the results for the Petri net model with different initial states are the same because of the model's symmetry, they are not shown here. In that table, control schemes are denoted by their order of transitions. For example, overlapping clock signals as shown in Figure

4.10(a) are denoted as (*clk2+*, *clk1-*, *clk1+*, *clk2-*) and non-overlapping clock signals as in Figure 4.10(b) are denoted as (*clk1-*, *clk2+*, *clk2-*, *clk1+*).

If clock signals change one at a time (1 to 16), all the control schemes cause at least one type of reversion loss and most of them cause both types of reversion loss. It is also shown that the overlapping and non-overlapping control schemes are only sub-sets of all possible clock signal orders. The reversion loss behaviours of these two control schemes identified from the model agree with the intuitive results described in Chapter 2, where overlapping clocks are found to cause output reversion loss and non-overlapping clocks are found to cause pump loss. (cf. Figure 4.10(a) and Figure 4.10(b) with rows 15 and 6 in Table 4.1).

Interestingly, the result changes when the two clocks *clk1* and *clk2* change at the same time, the clock transition sequences (*clk1-*, *clk2+*), (*clk1+*, *clk2-*), (*clk1-*, *clk2+*), (*clk1+*, *clk2-*) (See row 17 of Table 4.1) do not cause pump loss or output loss. This control scheme is indeed the synchronous clock signals introduced in Chapter 2 [18]. To investigate if there are any reversion losses generated with these clock signals, a simulation is run in Cadence, the result of which is shown in Figure 4.11.

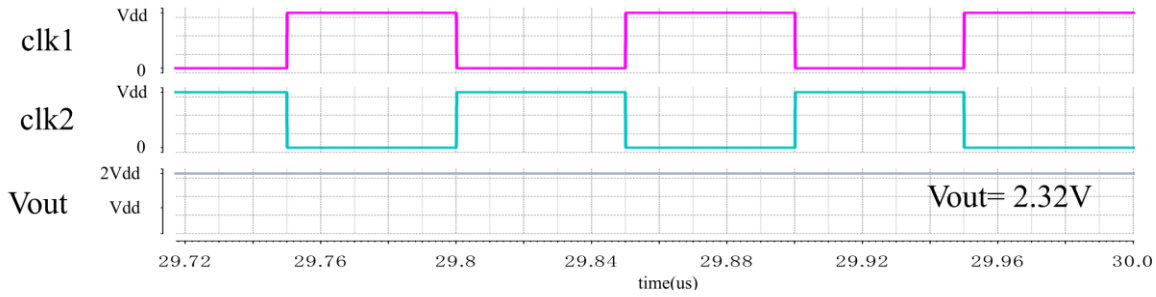


Figure 4.11: Simulation result for Voltage Doubler 1 with the particular control scheme.

Compared to the simulation waveforms for overlapping clocks and non-overlapping clocks shown in Chapter 2, the waveform in Figure 4.11 has a higher *Vout* showing the absence of pump losses and output losses. Therefore, for Voltage Doubler 1, it is clear that the only healthy control schemes that do not cause pump loss and output loss are when both clocks are synchronised and are exact inversions of each other. However, this synchronisation of the clocks may cause shoot-through currents, which will be analysed with the more complex example below.

Results for Voltage Doubler 2

The number of states for the Voltage Doubler 2 are too large to enumerate here. We ignore the control schemes that may cause reversion loss and only show the healthy control schemes that do not cause reversion losses in Figure 4.12.

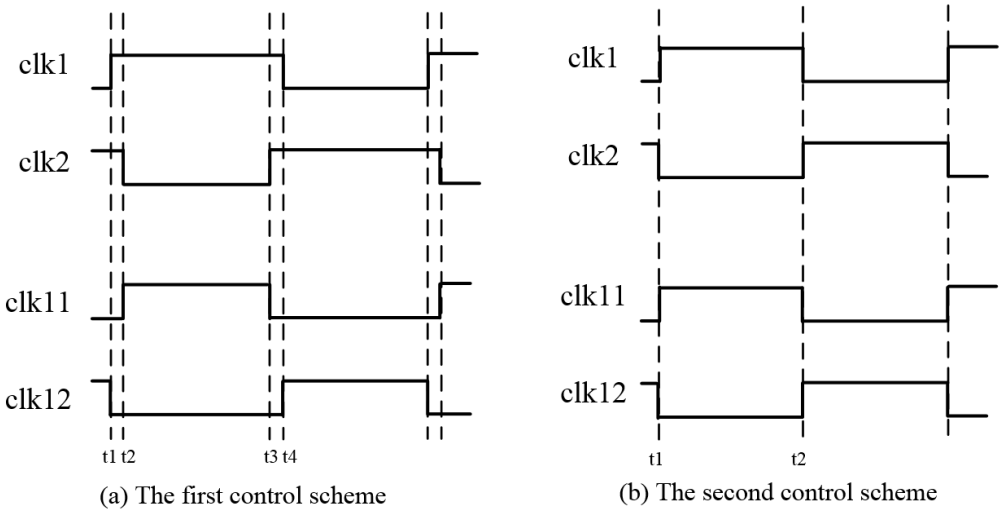


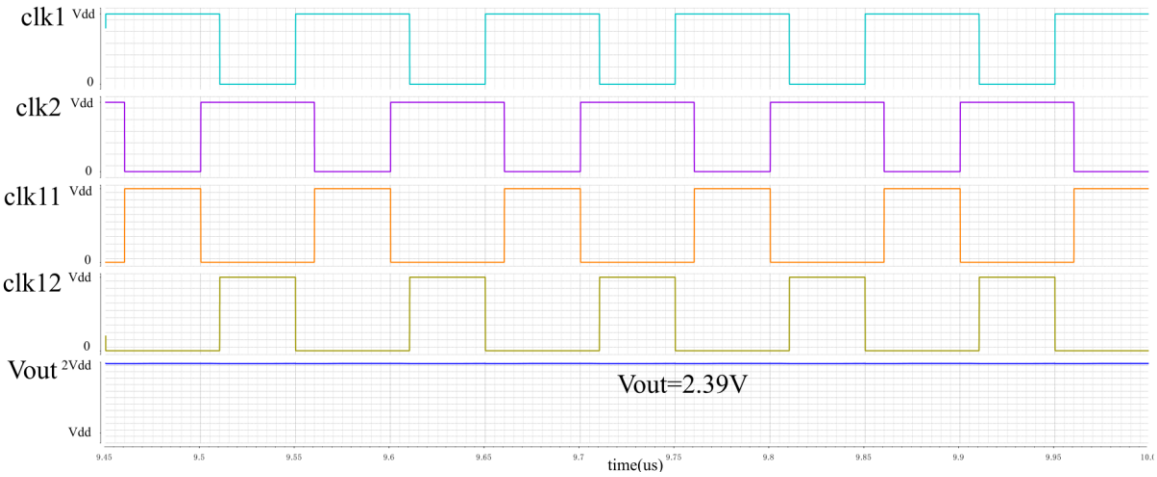
Figure 4.12: Healthy control schemes determined from reachability analysis.

The first control scheme is the original clocks adopted by [18]. The second is similar to the synchronised inverse clock signals shown in Figure 4.11. This control scheme was ignored by [18], most likely because of shoot-through current losses, as discussed below.

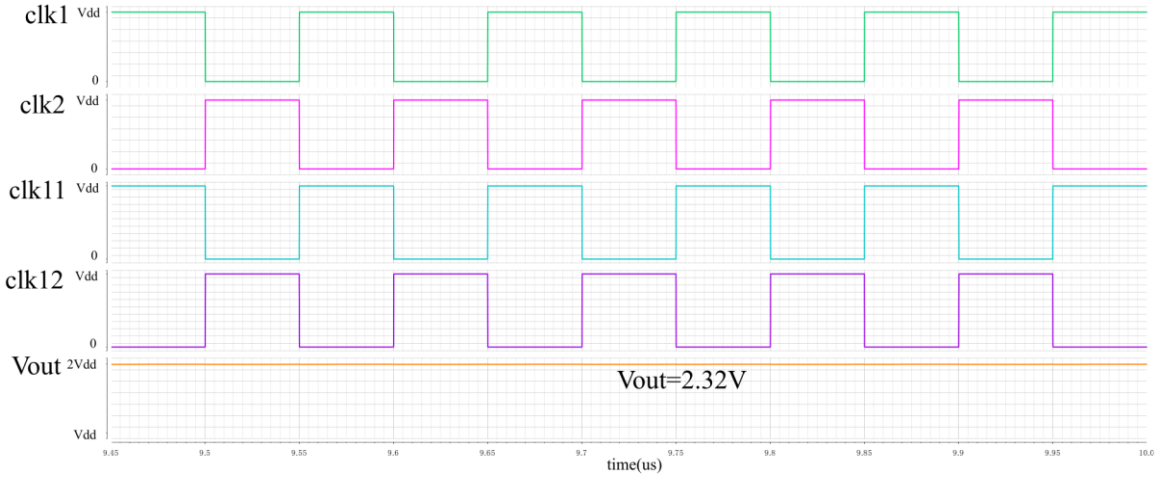
Reachability analysis for shoot-through currents is carried out for these two clock signal schemes. The result shows that shoot-through currents are not caused in Voltage Doubler 2 with the first clock signal scheme (shown in Figure 4.12(a)), while shoot-through currents exist at every clock transit when Voltage Doubler 2 is driven by the second control scheme where all clocks are synchronised (shown in Figure 4.12(b)).

Further verifications and discussion of the results.

Cadence simulation results from running the Voltage Doubler 2 with the two clock control schemes in Figure 4.12 are shown in Figure 4.13.



(a) Waveform for the first control scheme



(b) Waveform for the second control scheme

Figure 4.13: Simulation waveforms for Voltage Doubler 2 driven with the determined healthy control scheme.

Comparing the waveforms, the *Vout* of the doubler with the first determined control scheme (Figure 4.13(a)) has a higher value at 2.39V while the one with the second determined control scheme (Figure 4.13(b)) has a lower maximum output voltage at 2.32V. Indeed, *Vout* with the second control signals is similar to *Vout* in Figure 4.11. Both of them get a little voltage drop when clock signals transit, which is caused by shoot-through currents. In theory, it can also be verified that the Voltage Doubler 2 contains two similar copies of Voltage Doubler 1 with the same clock signals.

It is worth noting that the Voltage Doubler 2, like the Voltage Doubler 1, requires the synchronisation of signal transitions to avoid pump losses and output losses, as shown in Figure 4.12(a). For instance, in the scheme of Figure 4.12(a), *clk1* needs to be precisely synchronised to *clk12* and *clk2* needs to be precisely synchronised to *clk11* to avoid

reversion losses. Any misalignment between the relevant clock edges causes the reversion losses found in our reachability analysis. This is qualitatively the same requirement as the Voltage Doubler 1, which under synchronised inverse clock signals also exhibits no reversion loss, as shown in Table 4.1 (row 17). Therefore, what this cross-coupled voltage doubler achieves is the additional elimination of shoot-through currents, once reversion losses have been removed by clock synchronisation. Quantitatively, this may not bring a very significant voltage enhancement, depending on the implementation, at the cost of doubling the hardware size. Considering that capacitors are relatively large on a chip, Voltage Doubler 2's practical value is debatable.

To summarise, with a reachability analysis for the Petri net models of the two cross-coupled voltage doublers, all the clock signal schemes that may cause pump loss and output loss can be traced and verified. In addition, by modifying signal changes from transitions to places, shoot-through current conditions can also be found with the help of extended models. Besides, by analysing Voltage Doubler 1 and Voltage Doubler 2 with Petri nets, we find what Voltage Doubler 2 has really achieved is the elimination of shoot-through currents, which is not mentioned in [18].

4.5 Other cross-coupled voltage doubler studies with Petri nets

Additional reachability analysis was carried out for irregular combinations of clock signals including arbitrary jitter and skew relations, and more reversion loss conditions were found. Whilst these are trivial exercises for the computer-aided analysis environment, intuitive reasoning for these types of variations would involve substantial effort. Some of these relate to the subject of this section.

Reversion losses will also happen in the Voltage Doubler 2 when there are clock control mismatches. The clock mismatch is a phenomenon in the synchronous circuit, possibly caused by a clock skew or clock jitter [43]. For the control signals of the Voltage Doubler 2 adopted in [18], there are strict synchronous requirements for the clock transitions of (*clk1+*,*clk12-*), (*clk1-*,*clk12+*), (*clk2+*,*clk11-*) and (*clk2-*, *clk11+*), where any misalignment between control signals will introduce reversion losses. In [18], as clock pairs (*clk1*,*clk2*) and (*clk11*,*clk12*) are generated by their respective clock generators, the clock mismatches can be divided into two types: the clock pair (*clk11*,*clk12*) is advanced and the clock pair

(*clk11*,*clk12*) is delayed. Corresponding reversion losses due to clock mismatches can also be traced by a reachability analysis for the Petri net model shown in Figure 4.7.

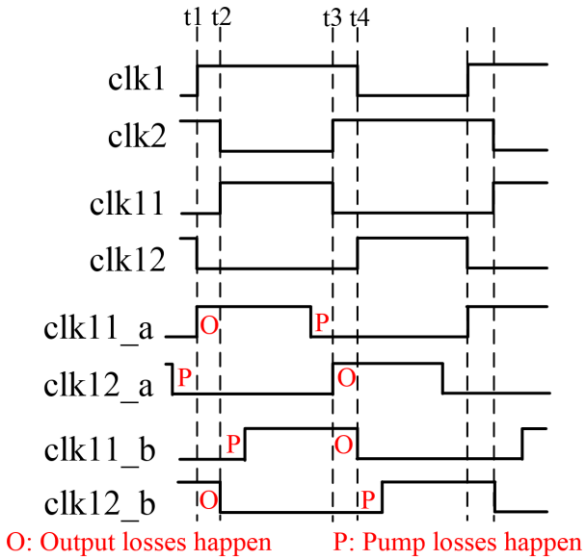


Figure 4.14: Reversion losses caused by clock mismatches in Voltage Doubler 2.

The results of reachability analysis for control signal mismatches in Voltage Doubler 2 are shown in Figure 4.14, where (*clk11_a*,*clk12_a*) is an advanced clock pair and (*clk11_b*,*clk12_b*) is a delayed clock pair. According to the results of reachability analysis, each type of control signal mismatch will cause a more severe reversion loss problem where both types of reversion losses occur. For example, when Voltage Doubler 2 is driven with *clk1*, *clk2* and the advanced clock pair (*clk11_a*, *clk12_a*), output losses happen during the interval between clk1+ and clk2- and the interval between clk2+ and clk1-, and pump losses happen during the interval between clk12_a- and clk11_a+ and the interval between clk11_a- and clk12_a+.

To eliminate the reversion losses and avoid the clock synchronisation problem, two other types of cross-coupled voltage doubler are proposed as introduced in Chapter 2. The first type of designs eliminate reversion losses with extra blocking transistors and the second type of designs eliminate reversion losses using external control signals; two representative designs of each type (Voltage Doubler 3 and Voltage Doubler 4) have been shown in Figure 2.15 and Figure 2.16 respectively. In this section, these two types of cross-coupled voltage doublers trying to solve the reversion loss problems are analysed using Petri net models.

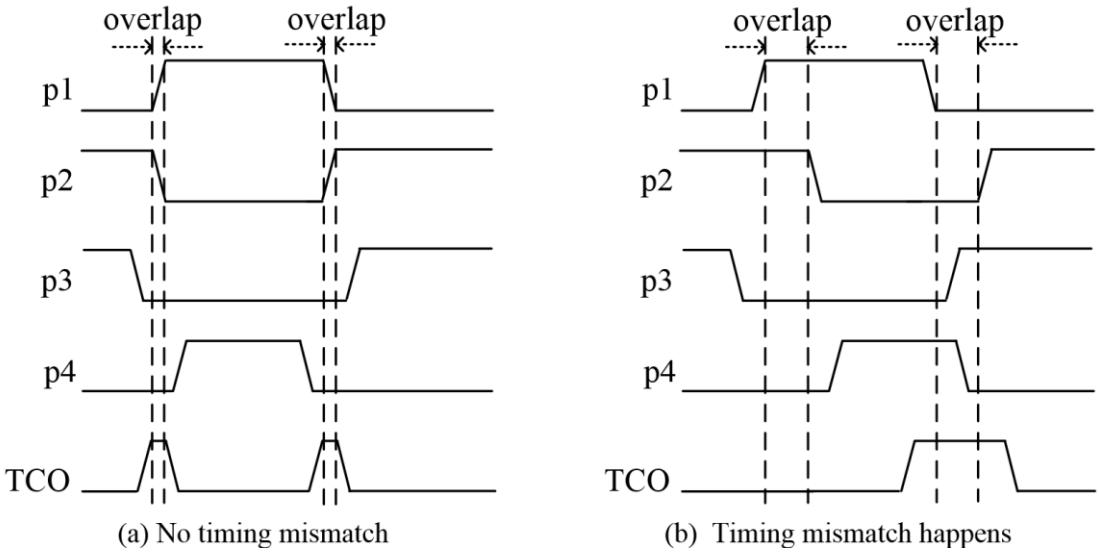


Figure 4.15: Control signals of Voltage Doubler 3, adapted from [40].

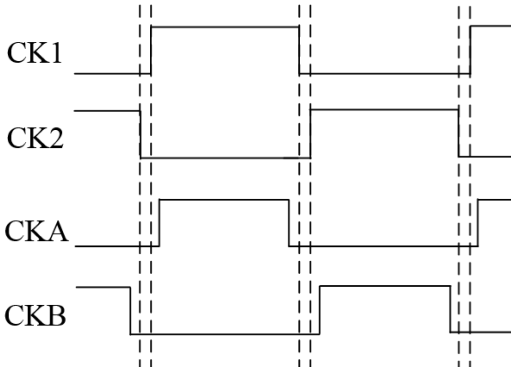


Figure 4.16: Control signals of Voltage Doubler 4, adapted from [47].

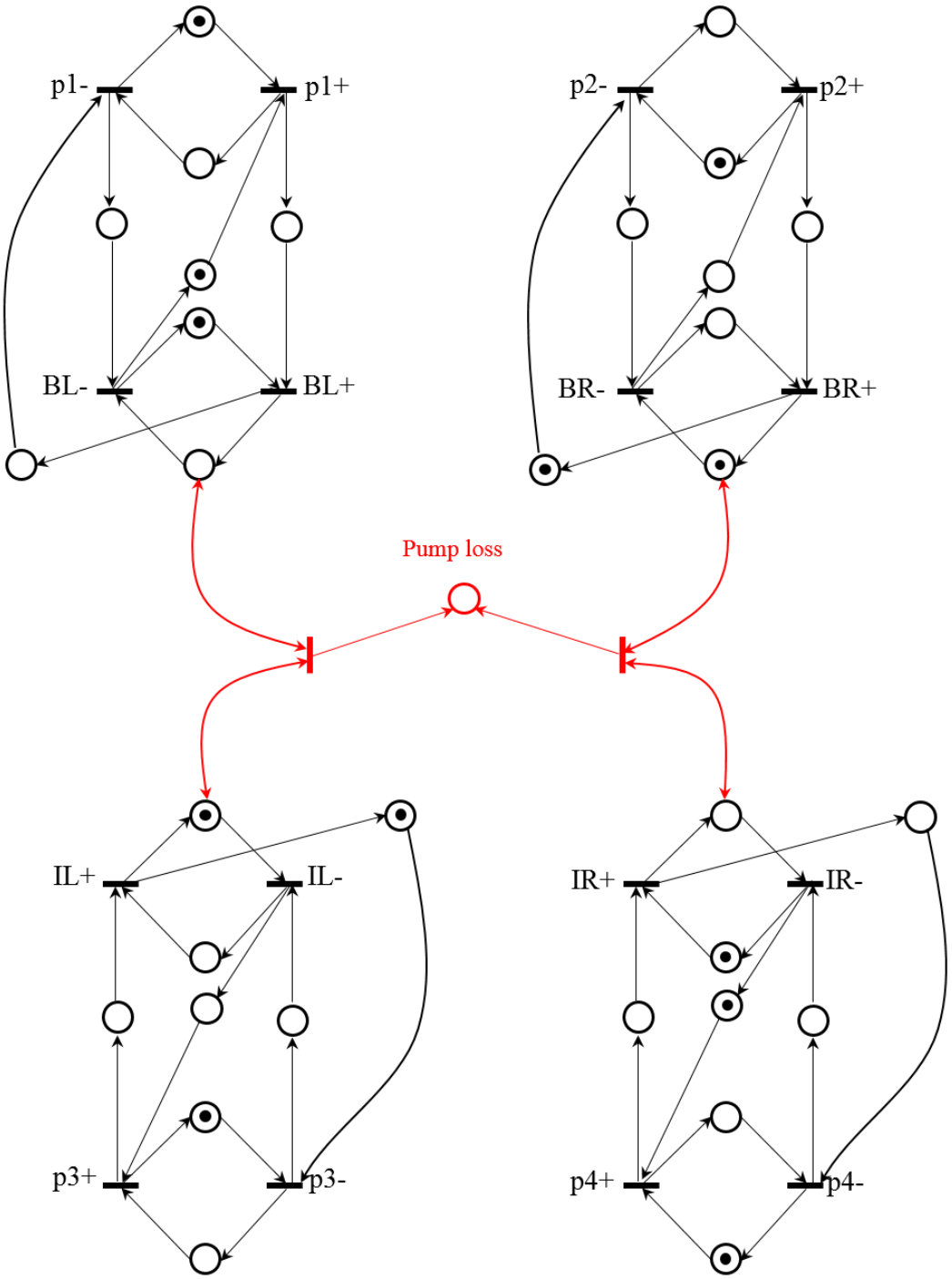


Figure 4.17: Petri net model for reversion losses in Voltage Doubler 3.

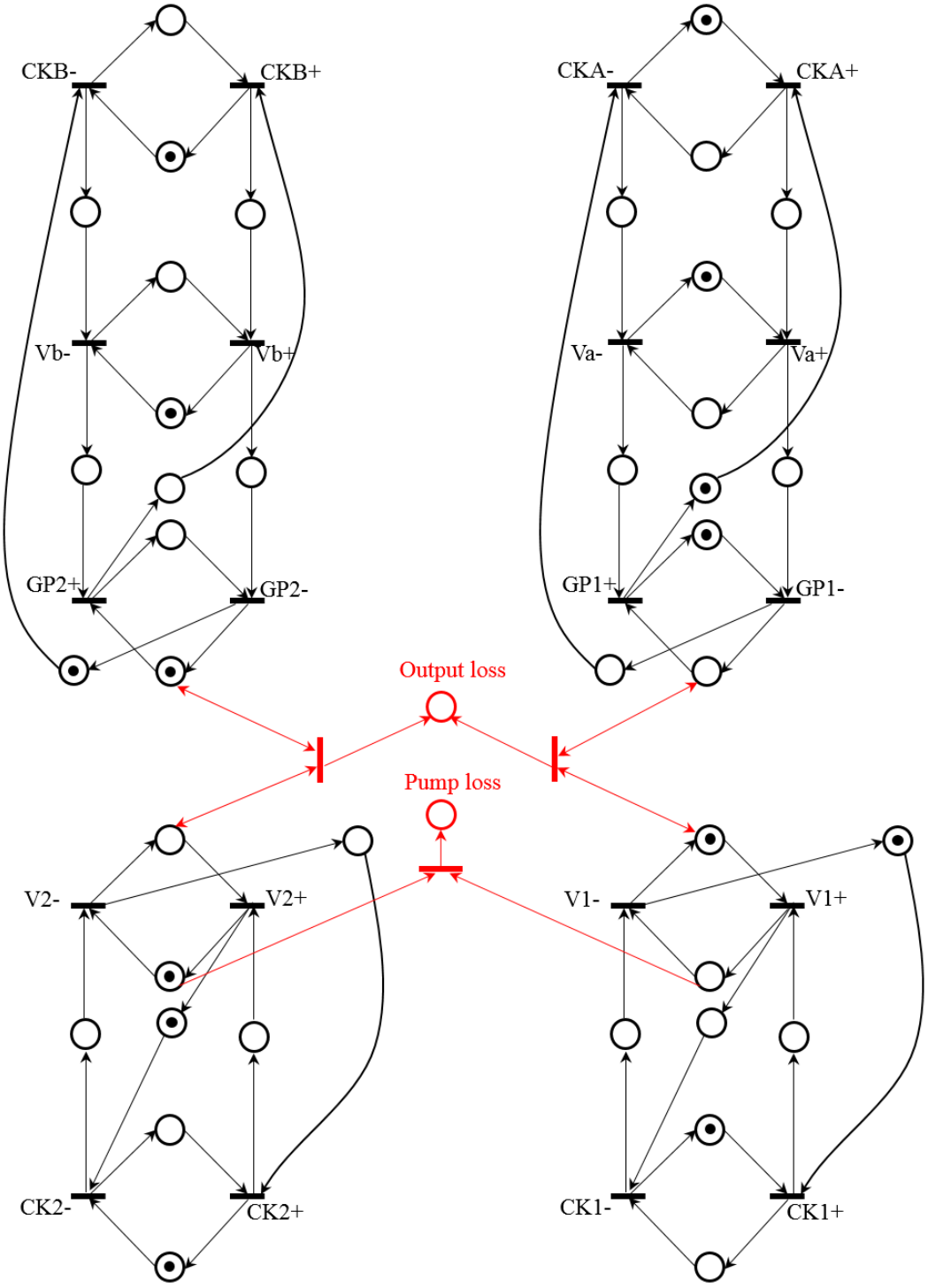
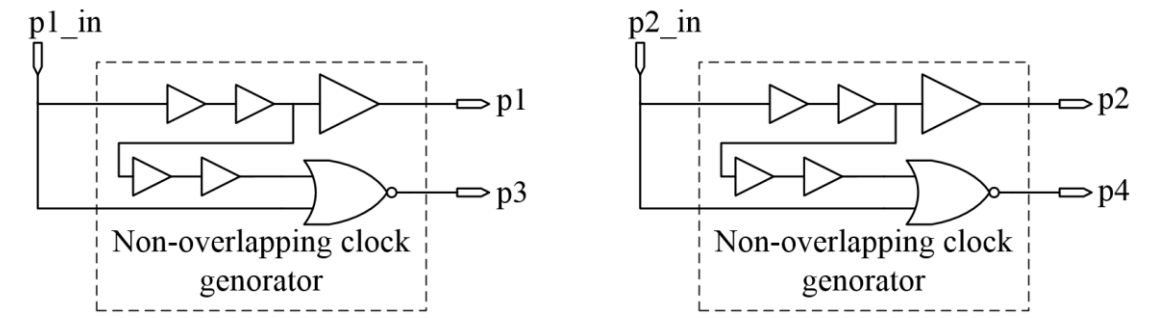
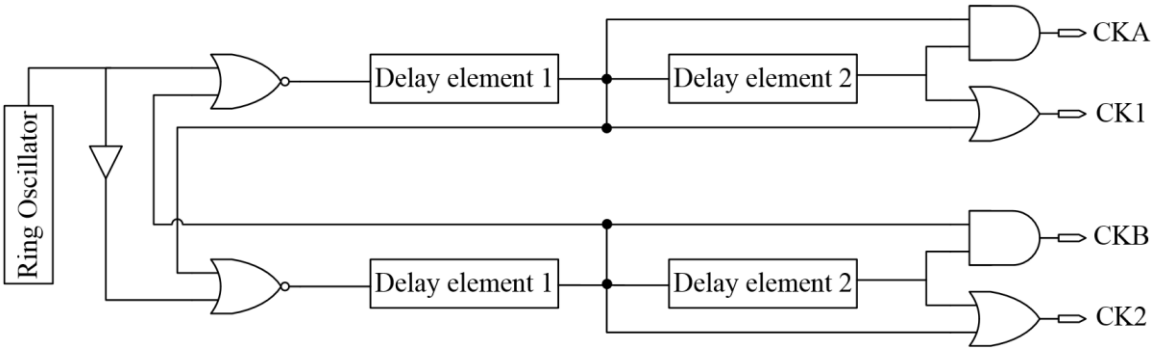


Figure 4.18: Petri net model for reversion losses in Voltage Doubler 4.



(a) Clock generator for Voltage Doubler 3



(b) Clock generator for Voltage Doubler 4

Figure 4.19: Clock generators for Voltage Doubler 3 and Voltage Doubler 4, adapted from [40] and [47].

Following the modelling method introduced in Section 4.2, Petri net model for reversion losses in Voltage Doubler 3 (Figure 2.16) is drawn as shown in Figure 4.17, where causality relations between transitions and reversion losses are described clearly. Based on the Petri net model, there is no output loss in Voltage Doubler 3. Because the potential output losses are blocked by the blocking transistor MR3 and ML3 once *BR* and *BL* are both at Vdd. On the other hand, pump losses from flying capacitors to Vdd happen when both *BR* and *IR* are at 2Vdd or both *BL* and *IL* are at 2Vdd. Since the control signals adopted in the [40] *p1* and *p3* or *p2* and *p4* are generated from a dedicated non-overlapping clock generator as shown in Figure 4.19(a), assuming no clock mismatch happened between *p1* and *p3* or *p2* and *p4*. Using a reachability analysis, we can find that there is also no pump reversion loss when Voltage Doubler 3 is driven with the clocks shown in Figure 4.15(a) (no timing mismatch) and Figure 4.16(b) (timing mismatch happens). In summary, based on the Petri nets and the related reachability analysis, there is no reversion loss when Voltage Doubler 3 is driven by control signals as shown in Figure 4.15(a) and Figure 4.6(b), and the possible reversion loss caused by clock mismatches have been eliminated by external transistors.

The blocking transistor scheme effectively removes the requirement for clock synchronisation.

Figure 4.18 shows the Petri net model for reversion losses in Voltage Doubler 4 (Figure 2.16). As can be seen from the Petri net model, output losses happen when both *GP1* and *V1* or both *GP2* and *V2* are at Vdd. Pump losses from the flying capacitor happen when both *V1* and *V2* are at 2Vdd. Using a reachability analysis, we can find that there is also no reversion loss when this cross-coupled voltage doubler is driven by the control signals, as shown in Figure 4.18. At the same time, when the control signals are generated from a dedicated non-overlapping clock generator as shown in Figure 4.19(b), there will be no timing mismatch problem in theory.

In summary, with reachability analyses for their Petri net models we can identify that there are no reversion losses in these two types of cross-coupled voltage doublers with dedicated control signals. However, some common problems for these designs can also be detected with their Petri net models.

Firstly, both Voltage Doubler 3 and Voltage Doubler 4 employ a dedicated clock generator to avoid corresponding clock mismatch. For example, Voltage Doubler 3 uses a non-overlapping generator as shown in Figure 4.19(a) to avoid clock mismatch between *p1* and *p3* or *p2* and *p4* and Voltage Doubler 4 also uses a dedicated clock generator as shown in Figure 4.19(b) to avoid clock mismatch among all control signals. There will be two issues when using a dedicated clock generator:

- Lack of scalability. Not all necessary control schemes can be produced by the corresponding clock generators. If the structure of an SCDDC gets complicated, it is hard to find a specified clock generator to produce such controls.
- Potential reversion loss problems. For example, as analysed previously, pump losses do not exist in Voltage Doubler 3 as it employs a non-overlapping clock generator that produces non-overlapping signals. However, by checking the clock generator shown in Figure 4.19(a), clock mismatch between *p1* and *p3* may happen when there is a clock jitter or clock skew. Based on the reachability analysis for the Petri net model, this clock mismatch will result in pump losses for Voltage Doubler 3.

Secondly, even though different techniques are proposed to eliminate reversion losses and to avoid the synchronisation problem, there is no general way to systematically design a cross-coupled voltage doubler without reversion losses. In the literature, almost all cross-

coupled voltage doubler designs seem to have been produced intuitively and then validated through waveform analysis or verbal reasoning. In effect, these are products of design and validation processes where the validation method is not formal.

To eliminate the reversion loss as well as other problems mentioned above, a new design method for SCDDCs based on discrete event models is presented in the next chapter.

4.6 Summary

This chapter proposes a new method of modelling reversion losses in SCDDCs with Petri nets. By representing states and events in SCDDCs as places and transitions, the causality and concurrency relations can be described formally and clearly. By using Petri net places to represent conditions that need checking, this type of model is demonstrated to be useful for verifying the occurrence and causes of properties such as reversion losses in SCDDCs. At the same time, the tool-supported reachability analysis capability of Petri nets facilitates the process of analysis, especially when SCDDCs get complex and large-sized. Above all, this Petri net model for SCDDCs will provide engineers and researchers with a systematic and efficient way to verify and detect reversion losses.

The modelling approach presented in this chapter extended the concurrency and causality relations described in the SC-STG model. The Petri net model applied to analyse and verify reversion losses is a practical application for modelling SCDDCs with discrete event models. Several cross-coupled voltage doublers are analysed with Petri nets in this chapter. Employing reachability analysis for their Petri net models, all reversion losses that may happen in these cross-coupled voltage doublers are explored, verifying how all potential reversion losses in these designs may or may not be removed. The weaknesses of these designs have also been exposed with Petri net models, such as the clock synchronisation problem and or the utilisation of dedicated clock generators.

Based on the analyses of these cross-coupled voltage doublers using Petri nets in this chapter, a new formalised design method for reversion-loss-free SCDDCs is being presented in Chapter 5. This new method is not only an extended work based on the Petri net model proposed in this chapter but also another practical application of this thesis: analysis and design of SCDDCs with discrete event models.

Chapter 5
Designing Reversion-Loss-Free SCDDCs with Discrete Event Models

5.1 Introduction

Several new designs with different techniques have been proposed in the literature to solve the problem of reversion losses in cross-coupled voltage doublers. These proposed cross-coupled voltage doublers have been modelled and analysed with the Petri net model in Chapter 4. With corresponding reachability analyses, these designs have been verified to alleviate reversion losses to different degrees, requiring different control measures. However, as studied in Chapter 4, there is no formal method to design an SCDDC without reversion loss systematically, and the elimination of reversion losses in these designs depends on the utilisation of dedicated clock generators, which must perform according to strict requirements including timing assumptions.

Based on the Petri net model for reversion losses, this chapter presents a method to design reversion-loss-free SCDDCs using Petri nets and STG. This new method employs external asynchronous controls to avoid reversion losses as well as timing mismatch problems. SCDDCs with asynchronous controls are potentially free of reversion losses caused by clock mismatches, since clock mismatches are inherently irrelevant in asynchronous circuits [65].

In this method, reversion losses in the targeted SCDDC designs are first modelled using Petri net models. Through reachability analyses of such Petri net models, corresponding

healthy control schemes that do not cause reversion losses can be determined. Then by modelling the determined healthy control schemes with STGs, the related asynchronous circuits producing such controls can be synthesised and obtained automatically using STG tools. The reachability analysis for the Petri net model and the verification and synthesis for STG can be both conducted in the tool Workcraft, which presents a systematic and convenient way to implement SCDDC designs. From the perspective of designers, the new design process based on discrete event models will be more efficient than methods adopted in designs in [40]-[50] that employ fixed clocks or external controls, based on intuitive design supported complex waveform validations. Also, the new method is more flexible than methods adopted in the literature for potentially extending to different types of SCDDCs. The utilisation of those discrete event models in SCDDC design avoids the dependency on dedicated clock generators. This is important because the relationship between external clock generators and the SCDDC block is open-loop, necessitating design-time timing matching which requires extra effort for precision at implementation time to ensure its correctness at run-time. With asynchronous control, the control signals may be organised in a closed-loop with the SCDDC, ensuring relative timing correctness, and thereby providing a degree of implementation precision tolerance.

A revision-loss-free cross-coupled voltage doubler design with the new design method is presented in this chapter as a case study example. The proposed cross-coupled voltage doubler achieves high conversion ratio and power efficiency, which demonstrates the validity of the Petri net modelling and the design method for SCDDCs as presented in this thesis.

This chapter is organised as follows. Section 5.2 presents the new design method for reversion-loss-free SCDDCs based on discrete event models, Section 5.3 shows example implementations of reversion-loss-free cross-coupled voltage doublers designed with the proposed method and Section 5.4 contains the simulation results of the proposed cross-coupled voltage doubler and the related comparisons with other designs.

5.2 Design method

The design method for a reversion-loss-free SCDDC based on discrete event models is illustrated in Figure 5.1. Firstly, a Petri net model capturing reversion losses in the targeted SCDDC is established, following which the healthy control without causing reversion

losses can be determined from a reachability analysis. Secondly, the determined healthy control is specified in an STG model, such that the corresponding asynchronous circuit producing such a control can be obtained by synthesising the STG model in Workcraft. The controls produced from asynchronous circuits are free of timing mismatch problems because of their event-driven nature. As both the Petri net model and STG model can be analysed and processed in tools such as Workcraft, this new method will provide engineers and researchers with a high-efficiency design flow for SCDDCs. Finally, based on other requirements for the targeted SCDDC, further specifications for the SCDDC can be performed, such as voltage promotion design and controller design. More details for the method are introduced as follows;

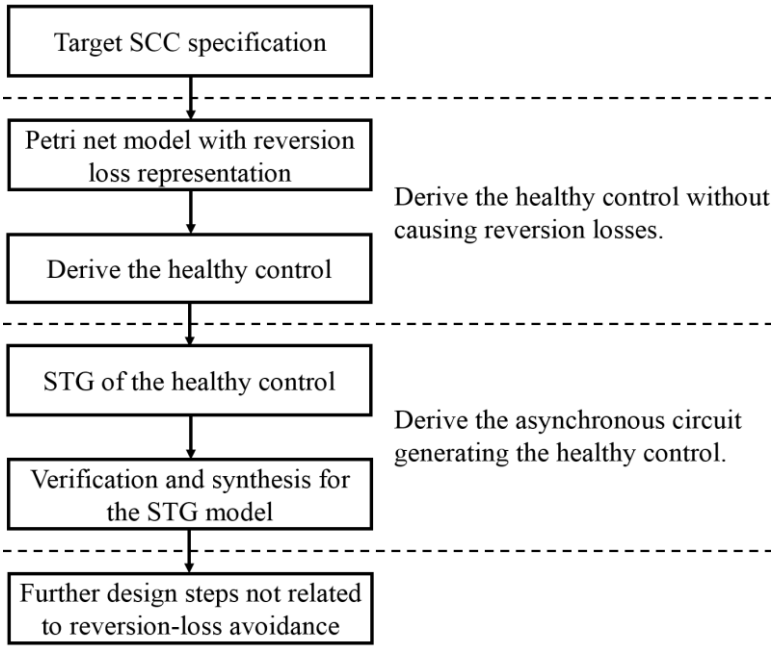


Figure 5.1: Flow chart of the new design method.

Deriving the healthy control scheme that avoids reversion losses

The acquisition of healthy control schemes is based on the Petri net models for reversion losses in SCDDCs, as introduced in Chapter 4. The concurrency and causality relations between events in Petri net models for SCDDCs can be obtained from SC-STG models. Alternatively, the concurrency and causality relations can also be obtained from the study of the SCDDC, as in some design processes we do not know the control signals and thus cannot develop related SC-STG model.

Deriving the asynchronous circuit implementing the healthy control

In this thesis, we convert the specification of the healthy control scheme into an STG model. Hence, a technique of modelling the obtained healthy control scheme in STG is needed. The modelling method is similar to the modelling method of SC-STG introduced in Chapter 3, which describes the concurrency and causality relations between signal transitions. The STG model can be formally verified and then automatically synthesised to an asynchronous circuit in Workcraft, which follows the conventional design flow for asynchronous circuits as introduced in Chapter 2.

Further design steps not directly related to reversion loss avoidance

The synthesised asynchronous control from the previous step is directly related to reversion loss avoidance. The SCDDC's other functionalities and requirements must then be designed separately after reversion loss avoidance has been achieved. These may include control signal voltage boosting that ensures conductance of MOS devices under all operating circumstances, the SCDDC's duty cycle and operating frequency requirements, etc. Some of these may be designed together or in line with the two previous steps, instead of being taken care of afterwards as shown in Figure 5.1. For instance, the required control signals may need to operate in a higher voltage range than the normal 0 to Vdd because the MOS device being controlled is connecting 2Vdd to Vdd. Moreover, if the clock signals are controlled asynchronously, the frequency and duty cycle of an SCDDC must be tuned by delay elements in the asynchronous control circuit. These additional design issues not related to reversion loss avoidance are included in the design studies below.

5.3 Case study of a cross-coupled voltage doubler design

In this section, a reversion-loss-free cross-coupled voltage doubler is designed as an example case study, using which the design method is demonstrated. The entire system structure is outlined in Subsection 5.3.1. This includes the basic SCDDC block itself and the associated support components such as the voltage boosting and controller modules. This is introduced upfront purely to facilitate description, as the actual design was achieved using the subsequently described steps. In Subsection 5.3.2, more design details are presented step by step based on the design method.

5.3.1 Overview of the proposed cross-coupled voltage doubler

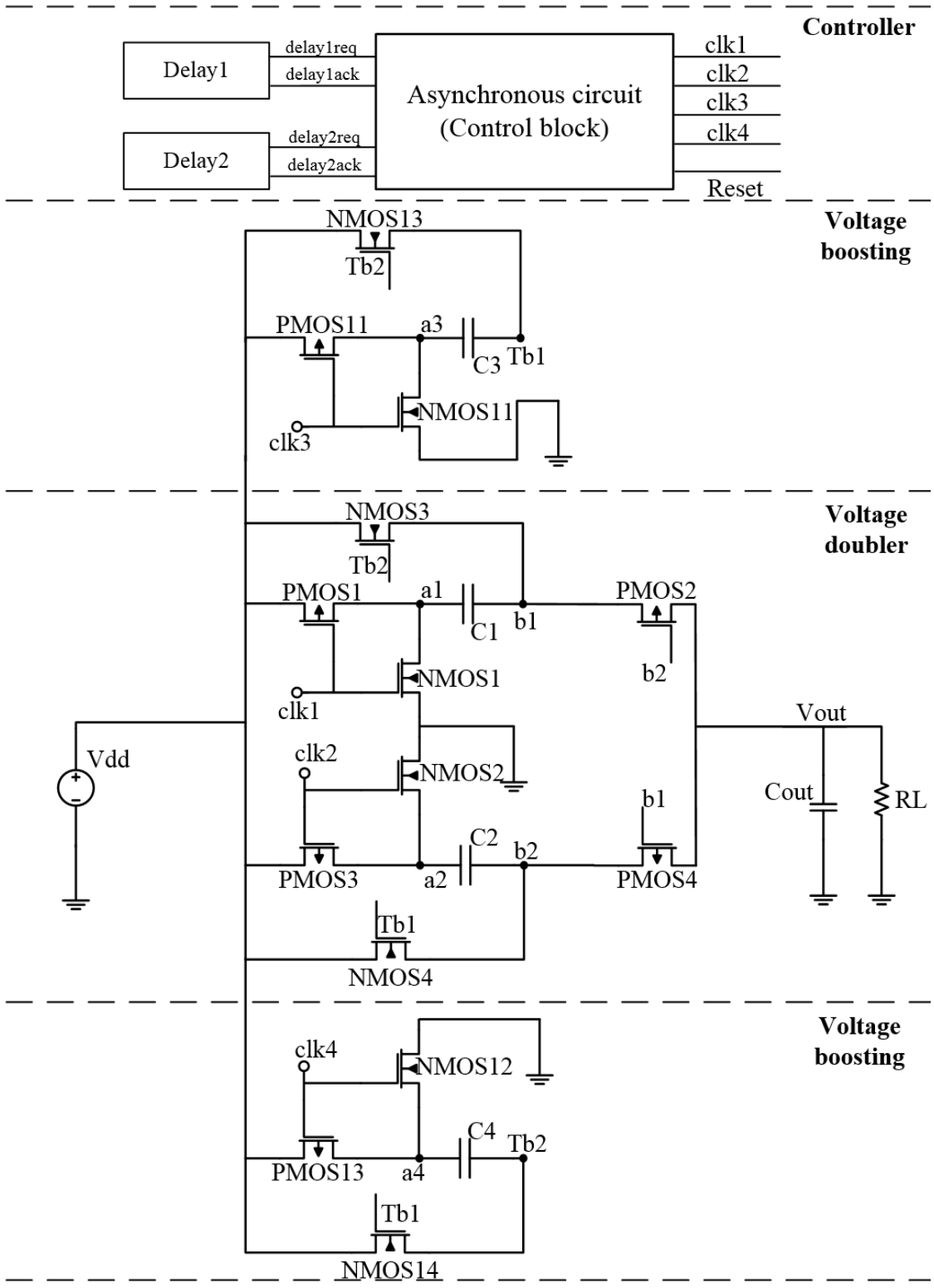
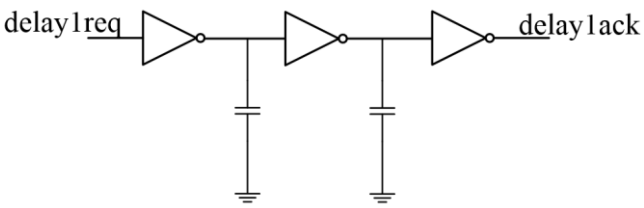


Figure 5.2: Schematic of the proposed cross-coupled voltage doubler.

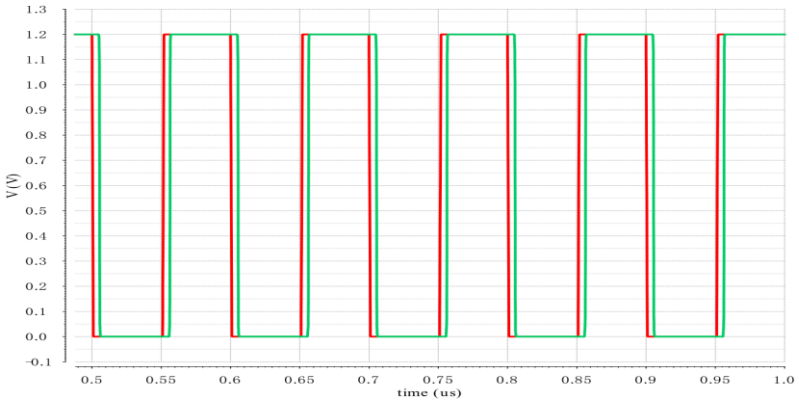
A sketch of the whole cross-coupled voltage doubler design is shown in Figure 5.2. It consists of three modules, including voltage doubler module, voltage boosting module and controller module. The principle of the voltage doubler module is similar to that of Voltage Doubler 1. This was chosen as the foundation because of its structural simplicity and suitability to demonstrate the workflow in Figure 5.1. The difference is that NMOS3 and NMOS4 are controlled by external signals *Tb2* and *Tb1*. The voltage boosting module is employed to boost the voltage of *Tb2* and *Tb1*. To ensure conduction of NMOS3 and NMOS4 under different circumstances, *Tb2* and *Tb1* must transit between Vdd and 2Vdd. The controller module generates asynchronous control signals for the proposed cross-coupled voltage doublers.

For the voltage boosting module, level shifters [40][45] or extra voltage doublers [40][46][47] from the literature may be utilised. In this design, extra voltage doublers are employed to boost the voltage because of their higher power efficiency. As can be seen from the voltage boosting module in Figure 5.2, two extra voltage doublers are employed; the first one generating control signal *Tb1* is controlled by a control signal of *clk3* and the second one generating control signal *Tb2* is controlled by a control signal of *clk4*. Meantime, these two voltage doublers are also cross-coupled, in which NMOS13 and NMOS14 are controlled by internal signals from each other. A system based on level shifters will incur significantly less silicon cost but will have lower power efficiency. The design method remains the same whichever voltage boosting technique is used, as the control signals are the important elements of the design and voltage boosting simply ensures that the MOS devices receive the control signals at the right voltages.

In this design, the control module regulating the frequency and duty cycle of control signals is implemented by delay elements, including one with a long period and one with a short period. The delay element is realised by cascaded inverters and capacitors, whose schematic and waveform are shown in Figure 5.3(a) and Figure 5.3(b) respectively. These may be made programmable by using multiplexes to control the number of stages used.



(a) Schematic



(b) Waveform

Figure 5.3: Delay element Delay1 and its waveform.

As can be seen from Figure 5.3(b), the red waveform is the original control signal and the green waveform is the signal with a short delay period of 5ns. By adjusting the number of delay stages, intervals with different periods can be produced. Consequently, the frequencies and duty cycle ratios of the control signals can be made programmable.

Since conventional cross-coupled voltage doublers in [40], [47] adopted a fixed frequency and duty cycle design, to have a better comparison with these designs, the example cross-coupled voltage doubler design is similarly studied only at a fixed frequency and duty cycle ratio. However, the proposed cross-coupled voltage doubler opens up for future work on the controller design by allowing arbitrary tuning of the working frequency and ratio of the duty cycle for better performance, with programmable delays.

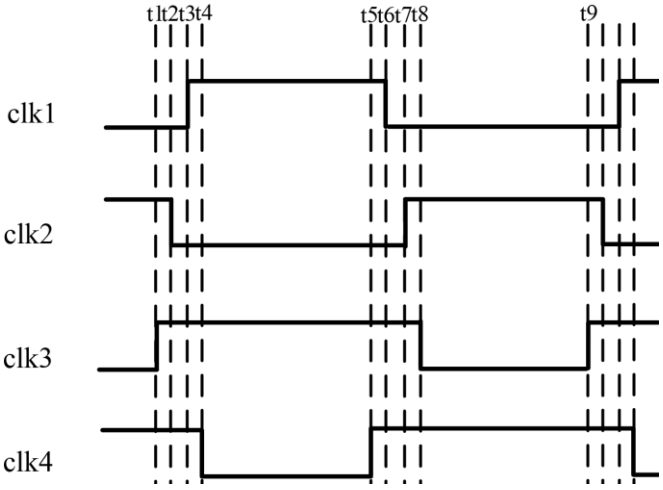


Figure 5.4: The control scheme for the proposed cross-coupled voltage doubler.

Control signals for the proposed cross-coupled voltage doubler are shown in Figure 5.4. These control signals are developed based on the proposed design method, which will not trigger any reversion losses. More detail regarding the obtainment of control signals is presented in Section 5.3.1.

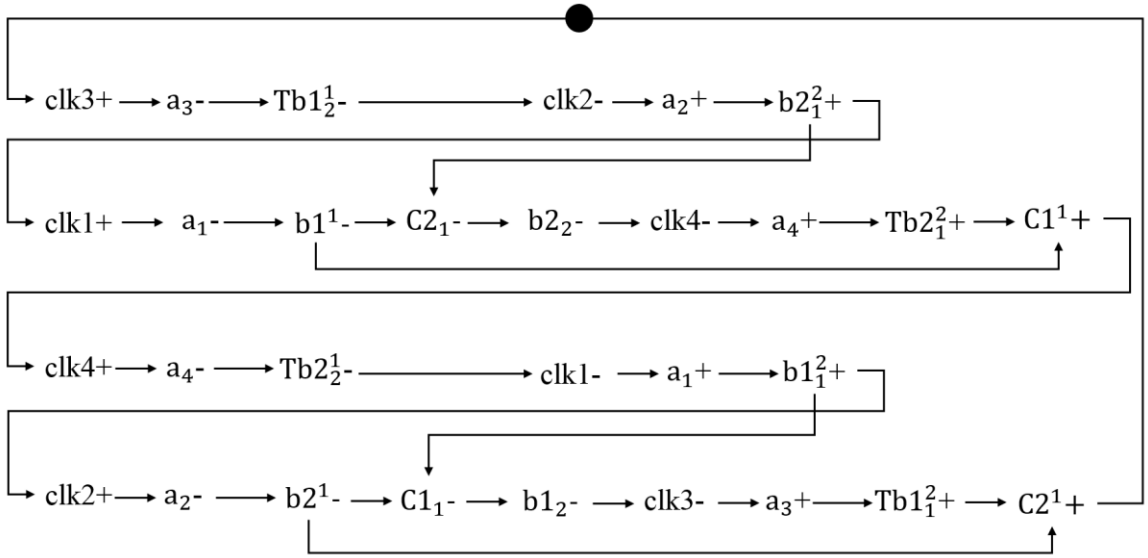


Figure 5.5: SC-STG for the proposed cross-coupled voltage doubler.

The SC-STG for the proposed design is shown in Figure 5.5, illustrating the principle of the design and the relations between events. The charging and discharging processes of C3 and C4 do not contribute to the energy transfer of the proposed design, which are not included in the SC-STG for simplicity. As can be seen from this SC-STG, the flying capacitor C2 starts to be discharged from Vdd when *b1* is Vdd and *b2* is 2Vdd and it starts to be charged to Vdd when *b2* is Vdd and *Tb1* is 2Vdd. Similarly, the flying capacitor C1 starts to be discharged from Vdd when *b1* is 2Vdd and *b2* is Vdd, and it starts to be charged

to Vdd when *b1* is Vdd and *Tb2* is 2Vdd. Meanwhile, other relations between signals are also shown in the STG. Relations between signals in the voltage boosting module are similar to ones in the voltage doubler module, since they indeed adopt the same voltage doubler unit. For example, *clk3+* makes *a3* go down from Vdd to 0, and then signal *Tb1* drops from 2Vdd to Vdd. It is similar to that *clk1+* makes *a1* go down from Vdd to 0 and then *b1* drops from 2Vdd to Vdd.

According to the new design method, there should be no reversion losses in the proposed design. In Section 5.4, the corresponding simulation results are presented and compared with other designs in the literature. In the next subsection, this proposed cross-coupled voltage doubler is constructed step by step by following the new method.

5.3.2 Designing the proposed cross-coupled voltage doubler step by step

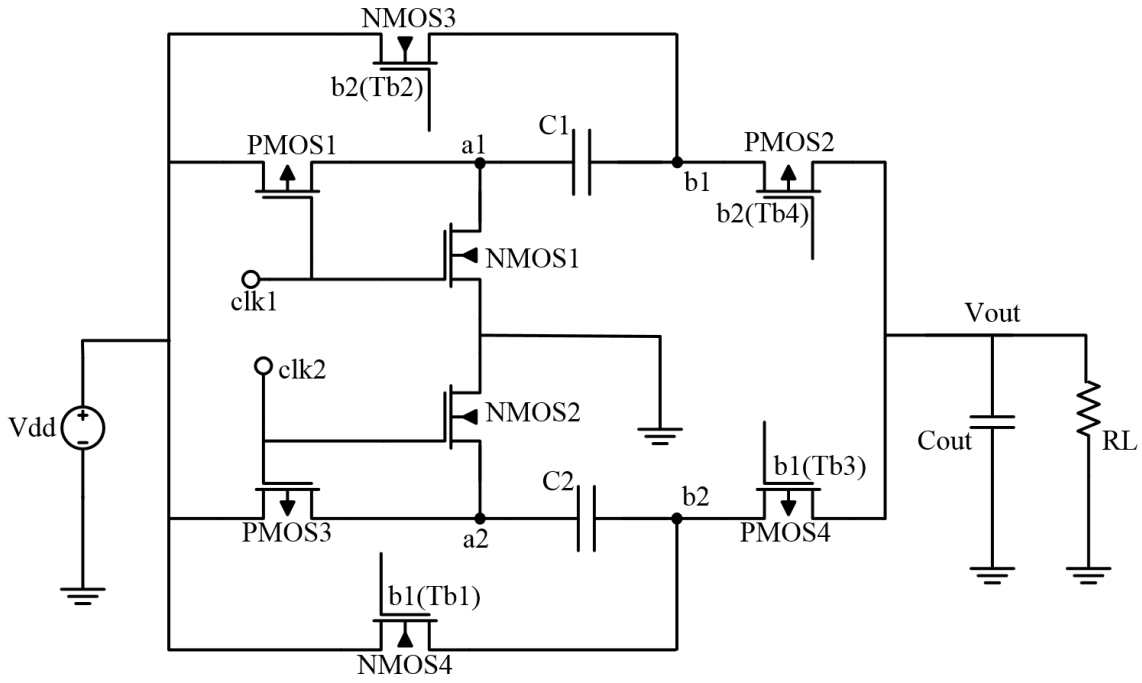


Figure 5.6: Schematic of a cross-coupled voltage doubler with external controls.

Figure 5.6 shows the Voltage Doubler 1, which is chosen as the basis for this case study. As analysed previously, there are three types of reversion losses when this cross-coupled voltage doubler is driven with different control signals. These reversion losses have been described in Chapter 2, and include pump losses, output losses and shoot-through current. This cross-coupled voltage doubler with the first two types of reversion losses can be divided as two cases, one case is shown in this subsection and the other is shown in

Appendix B. Neither of these cases suffers from shoot-through currents, as neither case uses synchronised clocks. In the first case, the cross-coupled voltage doubler is driven with non-overlapping clocks, where pump losses from flying capacitors to voltage source happen since NMOS3 and NMOS4 have undesirable conduction during the non-overlapping interval. In the second case, the cross-coupled voltage doubler is driven with overlapping clocks, where output losses from output to flying capacitors happen since PMOS2 and PMOS4 have undesirable conduction during the overlapping interval. The related healthy controls and asynchronous circuits generating such controls for these two cases are separately investigated using the new method as examples. As the design process of Case 2 is similar to Case 1, the design process of Case 2 is presented in Appendix B.

To eliminate such reversion losses, we introduce external control signals for MOS devices that may have reversion losses. In the Case 1, when *clk1* and *clk2* are non-overlapping we can introduce external control *Tb2* and *Tb1* for NMOS3 and NMOS4, with which NMOS3 and NMOS4 can be turned off by *Tb2* and *Tb1* to avoid the pump losses. The healthy control scheme without causing a reversion loss for *Tb2*, *Tb1*, *clk1* and *clk2* can be determined from a reachability analysis of the Petri net model. It is noteworthy that the proposed cross-coupled voltage doubler design presented in Subsection 5.3.1 is indeed the complete design for Case 1.

The new method designing SCDDCs with discrete event models is in a closed loop with the SCDDC and does not depend on a dedicated clock generator. In the following subsections, the healthy control scheme for Case 1 is analysed and generated using the new design method.

Deriving the healthy control scheme for reversion loss avoidance.

As analysed previously, there are pump losses from flying capacitors C1 or C2 to Vdd if the cross-coupled voltage doubler shown in Figure 5.6 is driven by non-overlapping clocks. To develop an asynchronous control to eliminate such reversion losses, NMOS3 and NMOS4 are controlled by external signals *Tb2* and *Tb1*. In theory, the control scheme of these signals can be determined with a reachability analysis for its Petri net model. However, the transitions of control signals *Tb1* and *Tb2* should be between Vdd and 2Vdd instead of 0 and Vdd to turn on NMOS3 and NMOS4 during the dedicated period. As introduced in Section 5.3.1, extra voltage doublers are employed to increase the voltage of these control signals. Extra voltage doublers are controlled by *clk3* and *clk4*, generating signals *Tb1* and

Tb2. The causality relations between these signals are: *clk3+*/ *clk3-* causes *Tb1-*/ *Tb1+* and *clk4+*/*clk4-* causes *Tb2-*/*Tb2+*. These are fully sequential actions without being concurrent with any other parts of the system, as can be seen in Figure 5.5. This means that there is no need to separately synthesise *Tb1* and *Tb2*, only the external signals *clk3* and *clk4* need to be considered in the design.

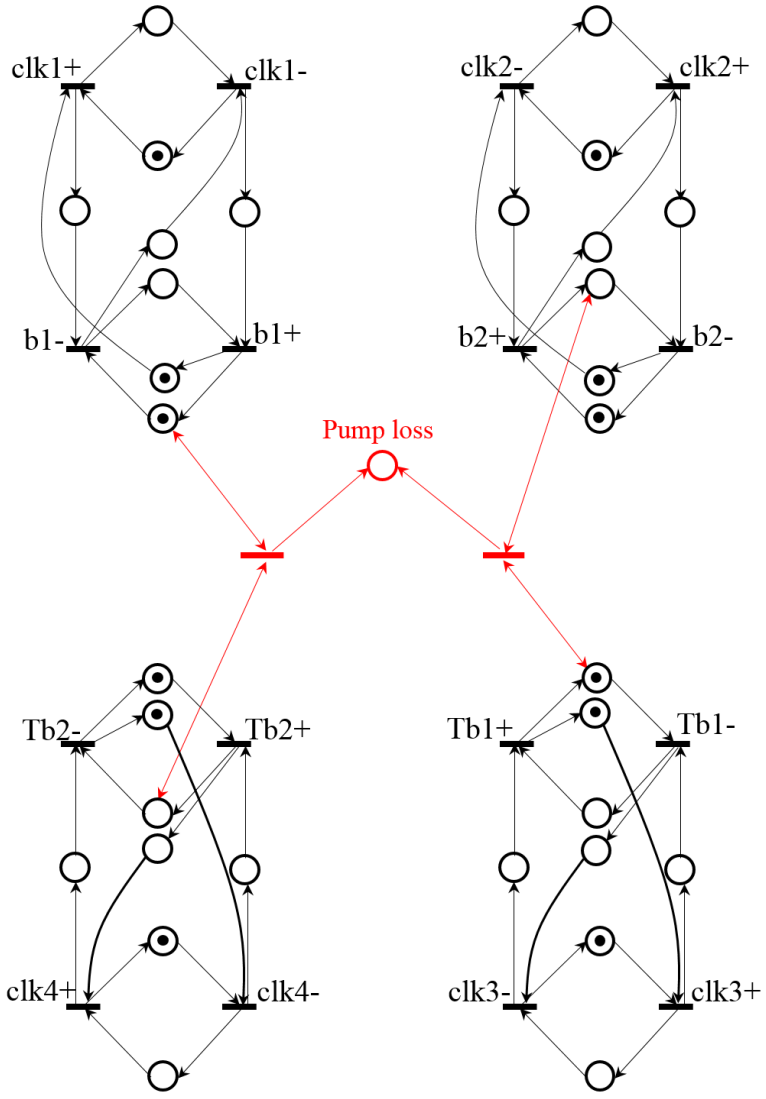


Figure 5.7: Petri net model for reversion losses in Case 1.

As signals *Tb1* and *Tb2* are affected by *clk3* and *clk4* from the extra voltage doublers, a Petri net model for the cross-coupled voltage doubler controlled by *clk1*, *clk2*, *clk3*, *clk4* is drawn as shown in Figure 5.7 to determine the healthy control scheme. Note here that unlike in the SC-STG of Figure 5.5, the *b* and *Tb* signals do not need an explicit representation of their higher than Vdd voltage ranges, because we are only interested in their moving up and down and not as to from which voltage to which other voltage the up and down

movement happens. The range of variance is only 1Vdd for both and the correct voltage boosting has already been ensured by the boosting modules.

In this Petri net model, since signals *clk1* and *clk2* are non-overlapping, there are only pump losses from the flying capacitors to Vdd, which occur when *Tb1* is 2Vdd and *b2* is 2Vdd or *Tb2* is 2Vdd and *b1* is 2Vdd. With a reachability analysis, a healthy control scheme for *clk3* and *clk4* which eliminates these signal value combinations can be obtained. This is shown in Figure 5.8.

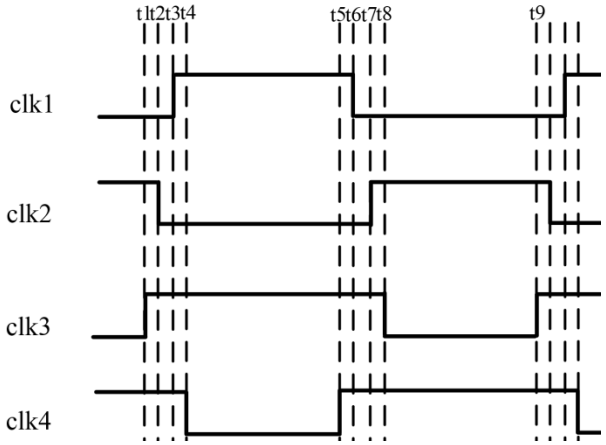


Figure 5.8: Determined healthy control scheme for Case 1.

As can be seen from Figure 5.8, signals *clk3* and *clk4* are overlapping. The overlapping gaps between *clk3* and *clk4* are wider the non-overlapping gap between *clk1* and *clk2*. Meanwhile, all these signals are not synchronised. The positive transition of *clk3* happens before the negative transition of *clk2* and the negative transition of *clk4* happens after the positive transition of *clk1*. The positive transition of *clk4* happens before the negative transition of *clk1* and the negative transition of *clk3* happens after the positive transition of *clk2*.

In summary, by implementing reachability analysis for the Petri net models, the healthy control scheme for Case 1 can be obtained formally. The next step is modelling these controls with STG and synthesising it to asynchronous circuits.

Deriving the asynchronous circuit generating the healthy control scheme.

The second step is to generate these control signals with an asynchronous circuit to avoid the clock mismatch problem caused by clock skews or clock jitters. The asynchronous circuit generating such control signals can be obtained directly with Workcraft by synthesising the STG model for these control signals. Following the conventional STG

modelling method, the STG for the determined healthy control scheme shown in Figure 5.8 is drawn, which is shown in Figure 5.9.

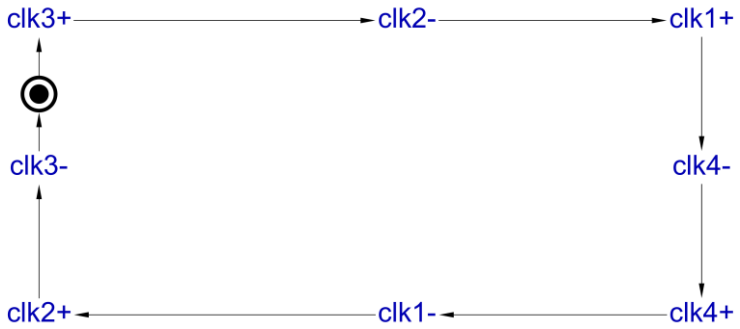


Figure 5.9: STG model for the determined healthy control scheme (Case 1).

However, in the experimental design, extra regulations for the frequency of control signals are required to make the cross-coupled voltage doubler work properly. As introduced in Subsection 5.3.1, delay elements are employed to regulate the frequencies and duty cycle ratios of control signals. Delay elements are inserted between two clock signal transitions. In this case, delay element Delay1 with input *delay1req* and output *delay1ack* is inserted to the short interval (e.g. interval *t1-t2*, *t2-t3*, *t3-t4*, *t5-t6*, *t6-t7* in Figure 5.8), while delay element Delay2 with input *delay2req* and output *delay2ack* is inserted to the long interval (e.g. interval *t4-t5* and *t8-t9* in Figure 5.8). The STG for the healthy control scheme inserted with delay is shown in Figure 5.10.

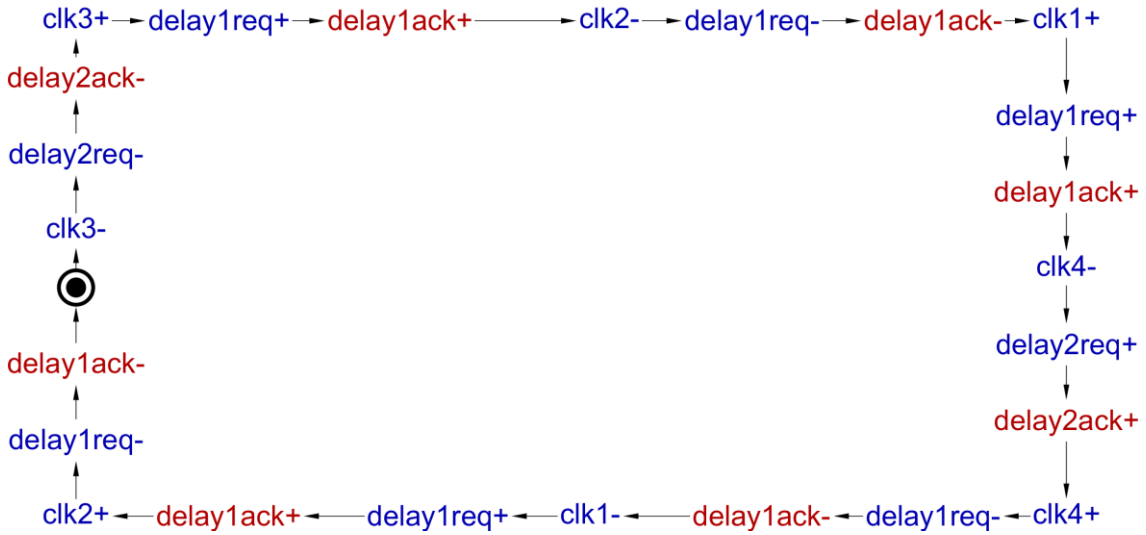


Figure 5.10: Practical STG model for the determined healthy control scheme (Case 1).

The STG can be synthesised to an asynchronous circuit in Workcraft after processing related verifications such as deadlock check, consistency check and persistency check as introduced in Chapter 2.

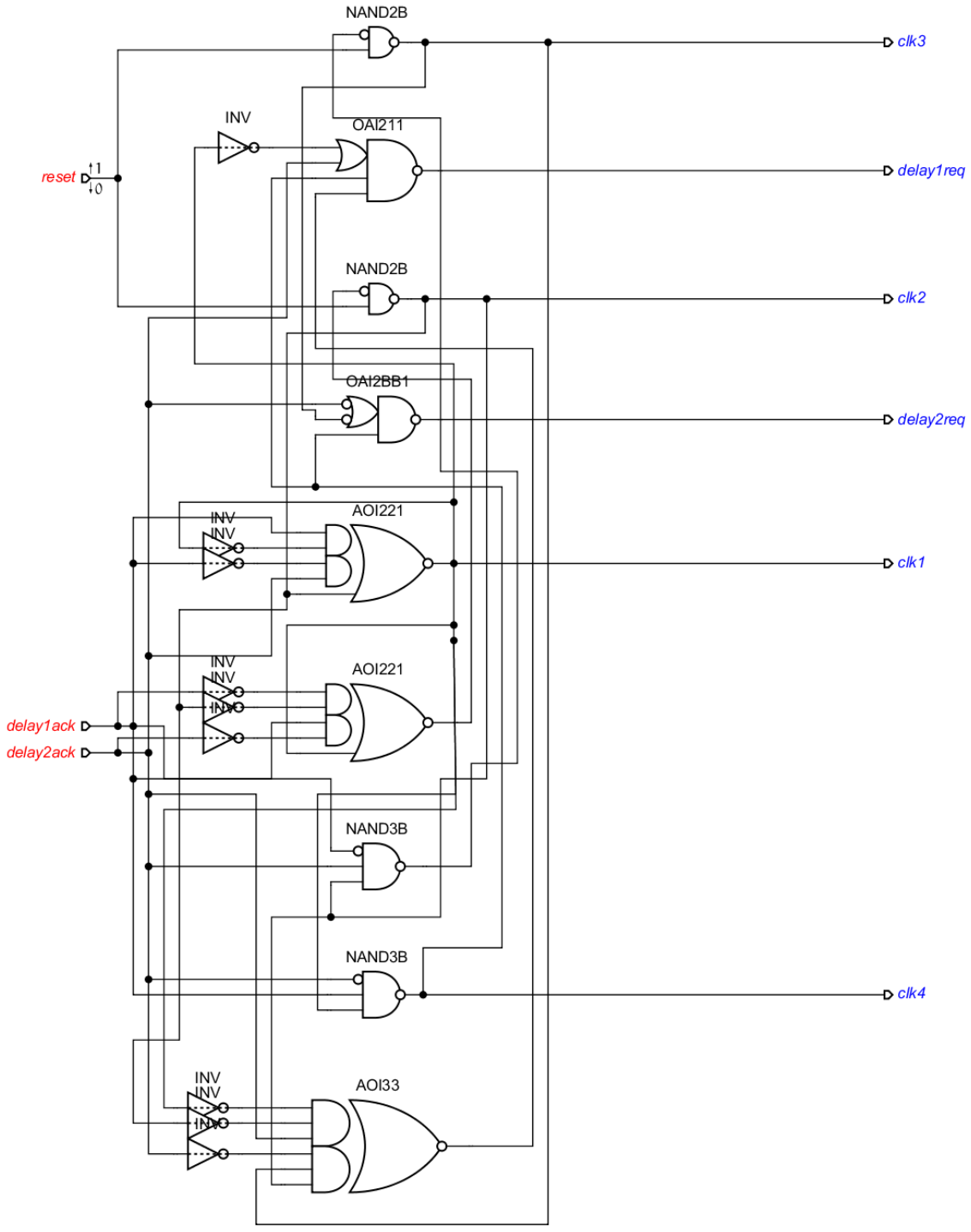


Figure 5.11: Asynchronous circuit synthesised from STG model (with reset signal).

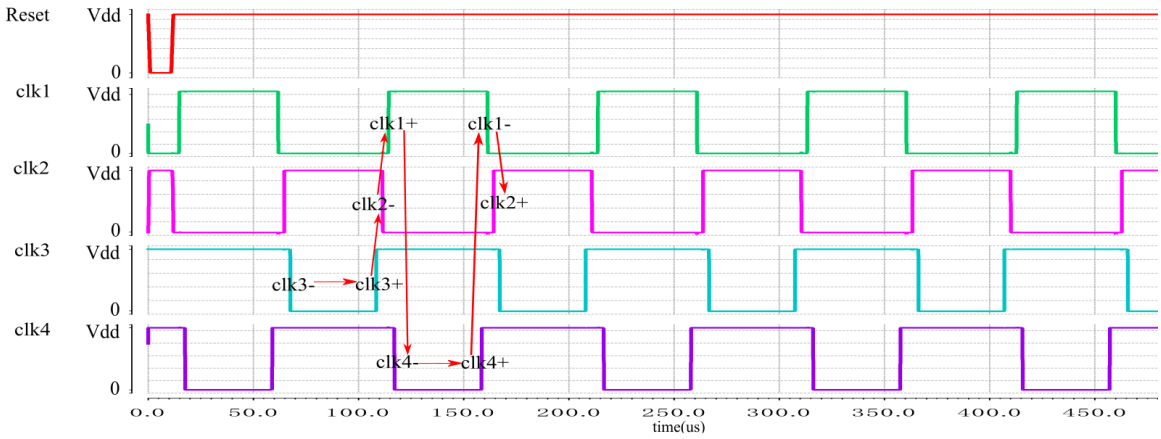


Figure 5.12: Simulation waveform for the generated asynchronous circuit (Case 1).

The synthesised asynchronous circuit with an additional reset signal is shown in Figure 5.11. Controls generated from this circuit are with asynchronous logic, where every transition is triggered by another one and there will be no timing mismatches problem. It does not require any dedicated clock generator to produce such controls. The only assumption is inverters with dashed lines, the delays of their output wire must be negligible. It can be satisfied by placing these inverters close to the main gates in the placing and routing stage.

The initialisation of the asynchronous circuit can also be analysed and designed in Workcraft. Initialisation Analyser is a tool integrated in Workcraft, which aims to provide asynchronous circuits with proper initialisations. The reset signal of the above circuit is obtained from Initialisation Analyser, the circuit can be initialised by resetting the reset signal. After inserting appropriate delay elements, a simulation for this circuit can be run in Cadence for the circuit in Figure 5.11. Figure 5.12 shows the waveform from the simulation, which is obtained using UMC 65nm technology. The timing of those signals perfectly matches the one in Figure 5.8. It has a frequency of around 10 MHz, which is generated by setting the long delay element to 40us and the short one to 2.5us. The model-driven design process ensures that when the proposed cross-coupled voltage doubler in Case 1 (as well as the one shown in Figure 5.2) is driven by the control signals generated by the circuit shown in Figure 5.11, there are no reversion losses due to clock mismatches.

In summary, the design flow of Case 1 is also the whole design flow for the proposed cross-coupled voltage doubler shown in Figure 5.2. This proposed cross-coupled voltage doubler is designed with discrete event models, from determining the healthy control scheme using a reachability analysis to obtaining an asynchronous control module by synthesising the

corresponding STG model. From the design example of the proposed cross-coupled voltage doubler design, the new design method provides designers with a formal and efficient way to determine the healthy control scheme and generate associated control circuits. Moreover, as can be seen from the design process of Case 1 as well as Case 2 in Appendix B, the healthy control schemes for Case 1 and Case 2 are totally different, but both designs avoid reversion losses. These two case studies prove that this method is flexible, which can generate different controls for SCDDCs with different requirements. Meanwhile, the production of these controls does not depend on any dedicated clock generators. This design method can be applied to SCDDC designs with different control requirements, as asynchronous circuits generating any type of control scheme can be obtained with their STG models. Most importantly, those two design steps with Petri nets and STGs are efficient, as the related design flows can be implemented with computer-aided design tools such as Workcraft.

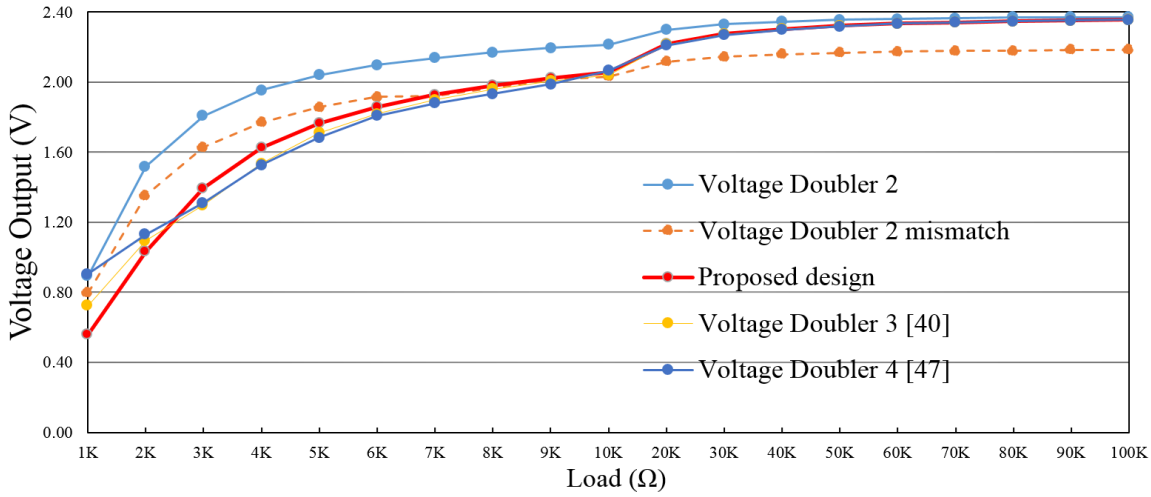
5.4 Simulation

The proposed cross-coupled voltage doubler and other designs are simulated in tool Cadence Virtuoso with UMC 65nm technology to enable comparison of their power conversion performance and power efficiencies. Comparisons of output voltages with different loads and power efficiencies with different loads are shown in this section. The power efficiency η is calculated as [32]:

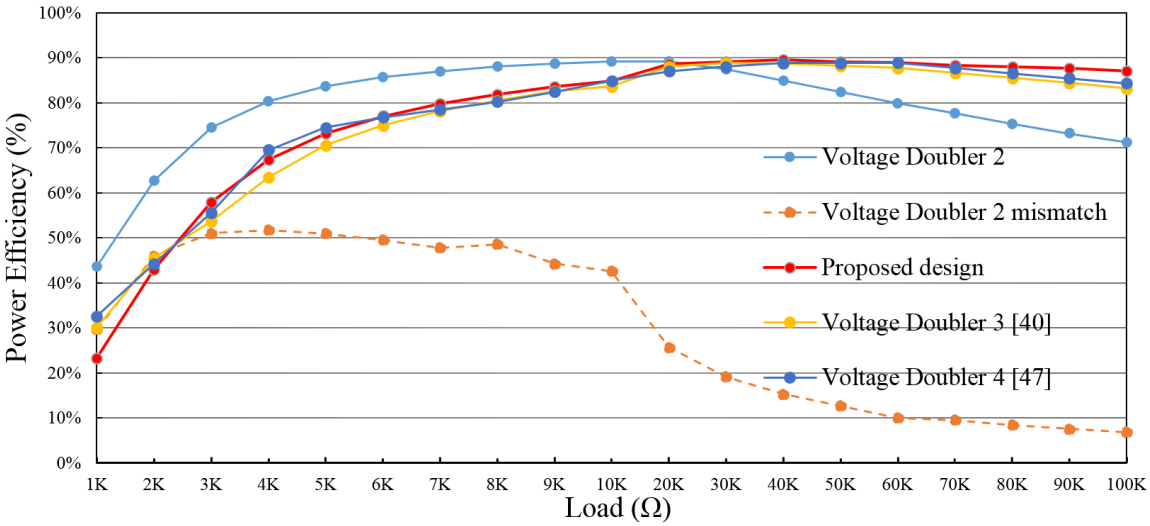
$$\eta = \frac{P_{out}}{P_{in}} \times 100\% = \frac{V_{out} I_{out}}{V_{in} I_{in}} \times 100\%$$

Where P_{out} is the output power, P_{in} is the input power, V_{out} in the output voltage, I_{out} is the output current, V_{in} is the input voltage and I_{in} is the input current.

In the proposed design, flying capacitors C1, C2, C3 and C4 are 100pF and the output capacitor Cout is 200pF. The frequency of control signals is set to 10MHz. For a fair comparison, other designs Voltage Doubler 2 [18], Voltage Doubler 3 [40] and Voltage Doubler 4 [47] have the same capacitor value, frequency and MOS device size.



(a) Voltage output



(b) Power efficiency

Figure 5.13: Simulated output voltages and power efficiencies versus load resistances.

The output voltages and power efficiencies for these designs with a 1.2V Vdd under different load resistances are shown in Figure 5.13. For the proposed cross-coupled voltage doubler, both the output voltage and power efficiency go up gradually with increasing load resistance. The voltage output reaches the highest level of 2.37V when the load is 100K and the power efficiency reaches the highest level of 88.49% when the load is 40K. When the load resistance is less than 4K, the proposed voltage doubler cannot work properly since the output drops to below 1.7V.

To compare the output voltages with different loads, Voltage Doubler 2 always has higher outputs for overall load from 1K to 100K (with a highest of 2.37 when the load is 100K). However, the output voltage reduces by about 0.2V when there is a 10% clock mismatch,

with the highest output of 3.6V being when the load is 100K. From load 1K to 10K, the proposed design also has nearly the same output voltage as the Voltage Doubler 3 and Voltage Doubler 4. From the power efficiency comparison shown in Figure 5.13(b), Voltage Doubler 2 is seen to achieve the highest efficiency when the load is from 1K to 10K, while Voltage Doubler 3 and Voltage Doubler 4 have almost the same values. The proposed design achieves the maximum power efficiency of 88.49% when the load is 40K, which is almost the same as the highest power efficiencies of 88.04% and 88.63% for Voltage Doubler 3 and Voltage Doubler 4 when the loads are 40K and 60K respectively.

In summary, the proposed design has almost the same voltage conversion performance and power efficiency as Voltage Doubler 3 and Voltage Doubler 4. Voltage Doubler 2 in most cases has better voltage conversion performance and power efficiency than the other three designs, but these parameters drop dramatically when there is a clock mismatch. Taking the clock mismatch problems for Voltage Doubler 2 into account, it is reasonable to say the proposed design, Voltage Doubler 3 and Voltage Doubler 4 have better voltage conversion performance and power efficiency. Most importantly, even though the proposed design has almost the same voltage conversion capability and power efficiency as Voltage Doubler 3 and Voltage Doubler 4, the proposed design is the result of a formal and efficient computer-aided design process rather than an intuitive design achieved through verbal reasoning validation process.

5.5 Summary

This chapter proposes a new method to design reversion-loss-free SCDDCs with discrete event models. In this method, the healthy control schemes without causing reversion losses for SCDDCs can be obtained formally from reachability analyses from Petri net models. Then the so-determined healthy control can be converted to asynchronous control by synthesising its STG model, eliminating the problem of timing mismatch and the requirement of external clock precision by the closed-loop nature of the event-driven control scheme. The design flow can be run in discrete event model tools such as Workcraft, which shows a higher design efficiency than other conventional design flows. In addition, this method is also more flexible than the conventional ones as it is able to generate different controls for different types of SCDDCs with maximum involvement of computer-aided

design automation. There is no need for intuition-based manual design and verbal reasoning-based validation, which tend to be quite different for different types of SCDDCs.

A new proposed cross-coupled voltage doubler is designed as a showcase for this method. It has almost the same level of voltage conversion performance and power efficiency as Voltage Doubler 3 and Voltage Doubler 4. This proposed voltage doubler is designed with the help of related CAD tool Workcraft. Compared with Voltage Doubler 3 and Voltage Doubler 4, whose designs are based on intuition and dependent on designer expertise, the design method behind is more reliable and the design process of the proposed voltage doubler is more efficient.

Chapter 6
Conclusions

This thesis presents new modelling methods for Switched-capacitor DC-DC Converters (SCDDCs) in low power integrated systems by using discrete event models. These discrete event models such as STGs and Petri nets aim to describe and model the causality and concurrency relations between discrete events in SCDDCs. Modelling SCDDCs with these discrete event models introduces new perspectives for the SCDDCs' designs, which have been partly exploited by this thesis. For example, STGs can be used to describe the relations between signal transitions, Petri net models can be utilised to detect undesirable reversion losses in SCDDCs, and asynchronous circuits synthesised from STGs can be employed to avoid the clock jitter and skew problems in SCDDC control. These examples in this thesis only partly explore the benefits taken from the discrete event models, which can be further exploited in the future for SCDDC designs.

In this chapter, Section 6.1 summarises the main contributions of this thesis, whereas Section 6.2 lists the potentials areas for future work.

6.1 Summary of contributions

Chapter 2 introduced the necessary background for SCDDCs and discrete event models. Previous modelling methods for SCDDCs and different cross-coupled voltage doubler designs were introduced and discussed in this chapter.

Chapter 3 presented a new modelling method that represents SCDDCs with an extended STG language called SC-STG. The causality and concurrency relations between discrete events in SCDDCs can be described formally and clearly with SC-STG models, which avoid the potential confusion caused by describing these relations with intuitive verbal language and simulation waveforms. Meanwhile, the introduction of multi-value transitions enables the analogue variation processes such as charging and discharging processes available to be described with SC-STG, presenting more details of the SCDDCs that can be used for analysis and design.

Several modelling examples including three ideal SCDDCs with different topologies and two cross-coupled voltage doublers were also given in Chapter 3, demonstrated the modelling method in detail. These SCDDCs were also modelled with Charge Flow Analysis for comparison; this conventional model fails to describe the concurrency and causality relations between events, especially when SCDDCs become complex and large-sized.

Chapter 4 presented an extension work based on SC-STGs, modelling reversion losses in SCDDCs with Petri nets. This leads to a formal method of determining and verifying reversion losses in SCDDC designs. With the Petri net models, the healthy control schemes without causing reversion losses can be determined and verified by reachability analysis. Related reachability analysis can be implemented in tools such as Petrify and Workcraft, which facilitates the design flow of SCDDCs.

The reversion losses in several typical cross-coupled voltage doubler designs were modelled with Petri nets in Chapter 4. It was discovered that Voltage Doubler 2 eliminated shoot-through currents with clock synchronisation requirements, similar to Voltage Doubler 1 which requires clock synchronisation to avoid other types of reversion losses, an aspect neglected by the literature [18]. Consequently, clock mismatch problems existed in both designs. Other cross-coupled voltage doubler designs from [40][47] are proposed to solve the clock mismatch problems. Although different techniques are adopted in these designs to eliminate the mismatch problem, almost all these cross-coupled voltage doubler designs require dedicated clock generators, which are open-loop and require attention in the entire process of design, implementation and manufacture to achieve reversion-loss avoidance.

Chapter 5 presented a formal method to design reversion-loss-free SCDDC with Petri nets and STGs, aimed at solving the reversion-loss problem by design. With Petri nets describing the causality relations among control signals, internal signals and reversion losses, the healthy control scheme which does not cause reversion losses can be obtained with reachability analysis. By modelling the healthy control scheme with STG and using these models for synthesis, a corresponding asynchronous circuit generating such controls can be obtained automatically in Workcraft. The discrete event asynchronous control scheme avoids the use of clock generators which must be reliably and precisely tuned to achieve the required control signal relations, including timing matching, overlapping and non-overlapping, because the control events are generated by the same controller according to their specified causal relations. This means that clock skew and jitter are not relevant to the correctness of the system. Both these steps can be run in tool Workcraft, providing a systematic and efficient design flow for SCDDCs. By replacing the existing verbal reasoning with computer-aided design, the new method is scalable and flexible, potentially covering any kind of control goal beyond reversion loss for any type of SCDDC beyond voltage doublers.

A new reversion-loss-free cross-coupled voltage doubler was designed with the new method to demonstrate the method. It has a similar voltage conversion ability and maximum power efficiency as theses parameters of state-of-the-art cross-coupled voltage doubler designs using transfer block mechanism and fixed clock controls. This shows the relative competence of the method: a simpler and more trustworthy design process does not need to result in worse results.

6.2 Future work

Bringing in event-based models into the analysis and design of the discrete behaviours of SCDDCs opens up exciting new research opportunities.

SCDDC designs with asynchronous control

In the new reversion-loss-free cross-coupled voltage doubler proposed in Chapter 5, asynchronous controls generated from STG model are utilised to avoid the clock mismatch problems in SCDDCs. Since the asynchronous circuit has other different inherent advantages such as high speed, low power consumption and robustness towards PVT

variations, designing and analysing SCDDCs with STGs or other discrete event models could potentially bring these positive features into SCDDC designs. From this perspective, designing SCDDCs with asynchronous controls based on discrete event models will potentially be a new method to improve the performance of SCDDCs.

Specifically, the new cross-coupled voltage doubler designed with discrete event models can be further optimised with asynchronous controls. As shown in Figure 5.13, the output of the proposed cross-coupled voltage doubler is going down gradually with the decrease of the load resistance, where the proposed design cannot work correctly since the output has dropped under 2.3V when the load resistance is less than 4K. This output voltage needs to be optimized when it is applied to a real low-power integrated system such as a wireless energy harvesting system. Conventionally, the output voltage can be optimised by a controller tuning the frequency, duty cycle and even topology. This controller also can be modelled with discrete event models and then designed with asynchronous logic. Consequently, the utilisation of the asynchronous circuit will potentially provide a bonus as introduced above to this design.

Extended work for SC-STG and Petri nets

In Chapter 3, the work modelling SCDDCs with SC-STGs is only applied to describe the causality and concurrency relations in SCDDCs. Even though these relations described in SC-STG are then extended to Petri net model whose verification can be run directly in Workcraft, SC-STG is not yet directly compatible with Workcraft or any other existing Petri net and STG tool. As conventional STG models can be processed directly in Workcraft for analysis or synthesis, further work can be done for an extending SC-STG model that is compatible with Workcraft. The extended SC-STG model compatible with Workcraft could potentially bring more analyses and verifications from the view of asynchronous logic to SCDDC designs and may even promote an automatic design flow for SCDDC designs. Alternatively, an SC-STG plug-in may be created for Workcraft.

Meanwhile, reachability analysis for Petri nets modelling reversion losses is currently partly compatible with Workcraft. For some specified cases such as the determination of the healthy controls, the related reachability analysis has to be carried out manually in Workcraft. Therefore, further work can also be done by extending the Petri net modelling work or creating a related plug-in module in Workcraft for the purpose of determining the healthy controls automatically.

A unified model for all types of analysis in this thesis

In this thesis, SC-STG is developed to model the concurrency and causality relations between events in SCDDCs, Petri nets model is used to model the SCDDCs and trace the reversion losses and STG is used for the specification of an asynchronous circuit. A possible area for future work is a unified model for all modelling work presented in this thesis.

The first candidate is the SC-STG model. It has the capability of describing the transition between different voltage levels clearly and explicitly. However, the problem of the SC-STG is the support of CAD tool such as Workcraft. If the extension work for SC-STG described in the previous subsection can be done, related reachability analysis for reversion losses and the specification of asynchronous circuits also can be carried out by the SC-STG in Workcraft. The second candidate is the Petri nets model. It has the capability of implementing a reachability analysis for reversion loss and specifying an asynchronous circuit in Workcraft. Petri nets can also be used to represent transitions between different voltage levels with certain extensions, however, the problem is how to keep the overall model in a simple and straight way.

Quantitative analysis for Petri nets

The Petri net model proposed in Chapter 4 aims for qualitative analysis for reversion losses, in which it is not essential to track the amount of reversion loss that occurred. Therefore, one of the potential areas for the Petri net modelling reversion losses in SCDDCs is the quantitative analysis of the reversion losses in SCDDCs.

Modelling mixed-signal circuits with discrete event models

This thesis reveals how the processes of analysing and designing SCDDCs benefit a lot from the proposed discrete event models. As the SCDDC is a type of mixed-signal circuit, thus the modelling work with discrete event models presented in this thesis could potentially be extended to other types of mixed-signal circuits such as inductor-based DC-DC converters, DAC, ADC, etc. Basically, discrete event models can be used to describe the causality and concurrency relations in these circuits, whilst analogue analysis can be conducted with traditional analogue methods. Most importantly, these models will provide designers with a new perspective of discrete event for corresponding design flows, which may also introduce some attractive benefits into their designs

Appendix A

Reachability analysis results for Case 1

As Workcraft currently does not support an automatic reachability analysis for Petri net modelling reversion losses to determine the healthy control schemes eliminating reversion losses, the healthy controls are obtained by animating the Petri nets manually in Workcraft. For Case 1 in Chapter 5, there are two ways to determine the healthy control schemes manually in Workcraft. The first one is listing all possible control schemes (*clk1* and *clk2* must be non-overlapping) as shown in Table A.1. Then implementing reachability analysis for these control schemes one by one to verify if the place of *pump loss* is marked. The results with the first method are also shown in Table A.1.

Table A.1: Results of reachability analysis for Case 1 (method 1).

	Control scheme	**Pump loss**
1	*clk2-*, *clk1+*, *clk3+*, *clk4-*	Yes
2	*clk2-*, *clk3+*, *clk4-*, *clk1+*	Yes
3	*clk2-*, *clk3+*, *clk1+*, *clk4-*	Yes
4	*clk3+*, *clk4-*, *clk2-*, *clk1+*	Yes
5	*clk3+*, *clk2-*, *clk4-*, *clk1+*	Yes
6	*clk3+*, *clk2-*, *clk1+*, *clk4-*	No
7	*clk2-*, *clk1+*, *clk4-*, *clk3+*	Yes
8	*clk2-*, *clk4-*, *clk3+*, *clk1+*	Yes
9	*clk2-*, *clk4-*, *clk1+*, *clk3+*	Yes
10	*clk4-*, *clk3+*, *clk2-*, *clk1+*	Yes
11	*clk4-*, *clk2-*, *clk3+*, *clk1+*	Yes
12	*clk4-*, *clk2-*, *clk1+*, *clk3+*	Yes

As can be seen from the results, control scheme 6 will not lead to any pump losses for the cross-coupled voltage doubler in Case 1. Because of the symmetry of the Petri nets, the whole control scheme 6 should be (*clk3+*, *clk2-*, *clk1+*, *clk4-*, *clk4+*, *clk1-*, *clk2+*, *clk3-*), which is the one shown in Figure 5.8.

The second method is adding extra monitoring sub-nets in the Petri net model as shown in Figure A.1. The extra window for output loss is employed to make sure that *clk1* and *clk2* are non-overlapping (output loss happens when both *clk1* and *clk2* are at Vdd). Then have

reachability analysis for all possible control schemes one by one until the healthy scheme is determined. The reachability analysis result with the second method is shown in Table A.2.

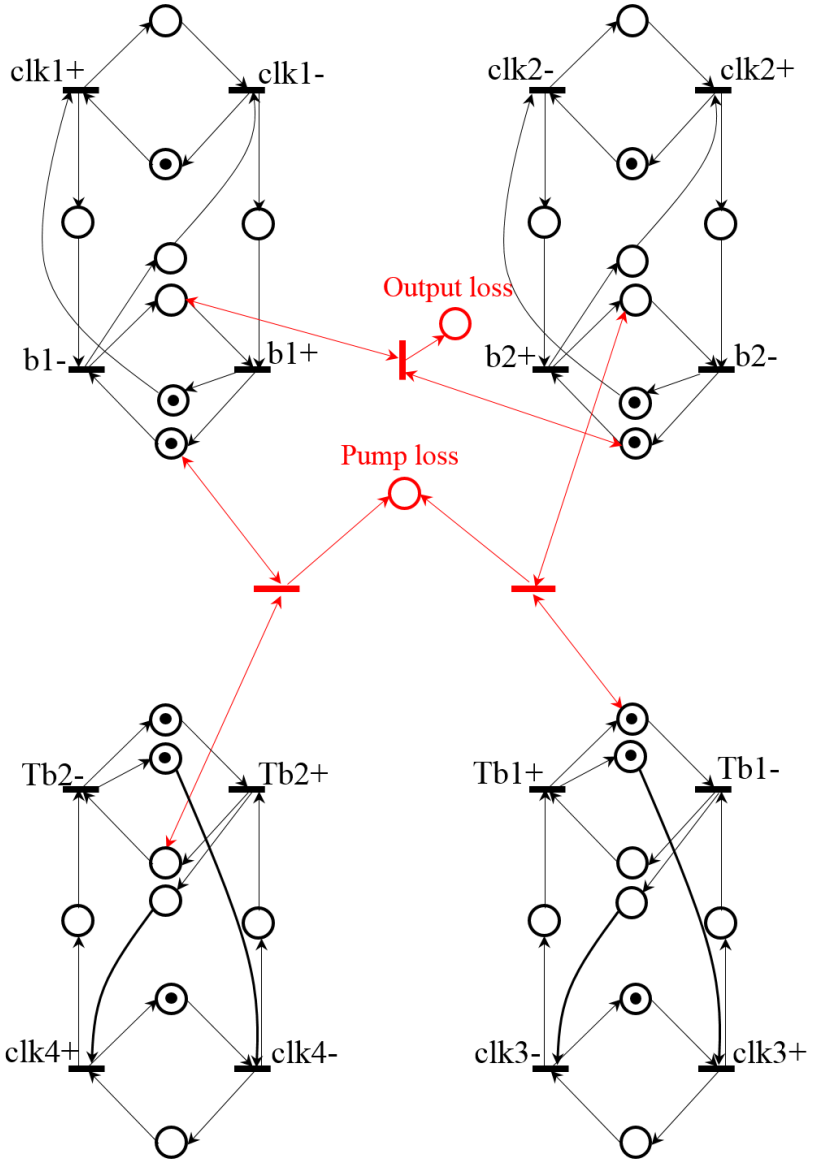


Figure A.1: Petri nets for Case 1 with extra monitoring sub-nets.

Table A.2: Results of reachability analysis for Case 1 (method 2).

	Control scheme	Pump loss	Output loss
1	*clk1+*	No	Yes
2	*clk2-*	Yes	No
3	*clk3+*	No	No
4	*clk3+,clk1+*	No	Yes
5	*clk3+, clk2-*	No	No
6	*clk3+, clk2-, clk1+*	No	No
7	*clk3+, clk2-, clk1+,clk4-*	No	No
8	*clk3+, clk2-, clk1+,clk4-,clk1-*	Yes	No
9	*clk3+, clk2-, clk1+,clk4-,clk2+*	No	Yes
10	*clk3+, clk2-, clk1+,clk4-,clk3-*	Yes	No
11	*clk3+, clk2-, clk1+,clk4-,clk4+*	No	No
12	*clk3+, clk2-, clk1+,clk4-,clk4+,clk1-*	No	No
13	*clk3+, clk2-, clk1+,clk4-,clk4+,clk1-,clk2+*	No	No
14	*clk3+, clk2-, clk1+,clk4-,clk4+,clk1-,clk2+,clk3-*	No	No

From the reachability analysis, the control scheme (*clk3+*, *clk2-*, *clk1+*, *clk4-*, *clk4+*, *clk1-*, *clk2+*, *clk3-*), which is the one shown in Figure 5.8, will not result in any reversion losses in the proposed cross-coupled voltage doubler.

The healthy control scheme for Case 2 also can be determined in Workcraft with these two methods.

Appendix B

System structure and design process of Case 2

A sketch of the whole cross-coupled voltage doubler design based on Case 2 in Chapter 5 is shown in Figure B.1.

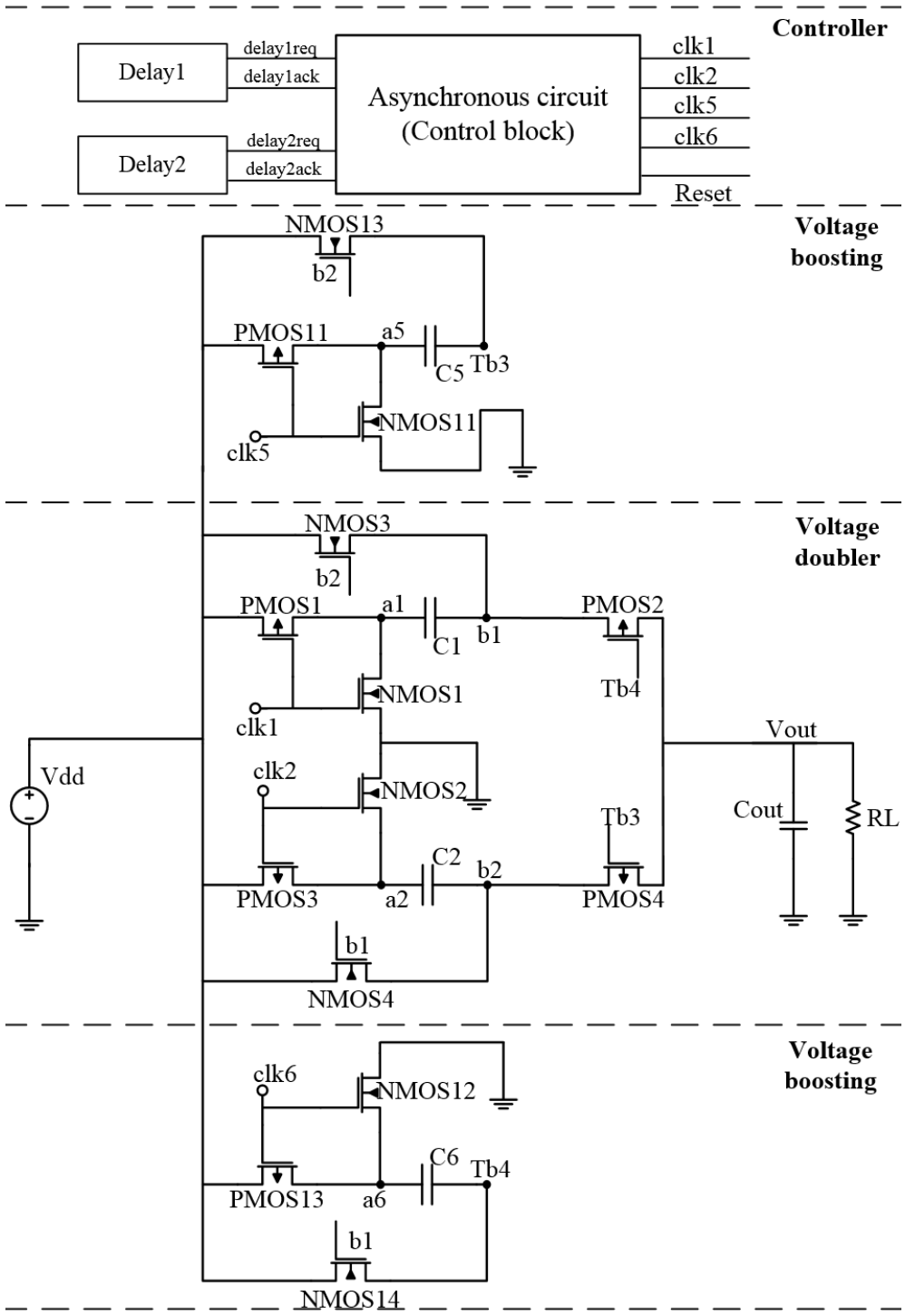


Figure B.1: Schematic of a new cross-coupled voltage doubler based on Case 2.

It also consists of three modules, including voltage doubler module, voltage boosting module and controller module. The principle of this voltage doubler module is similar to the one shown in Figure 5.2. The difference is that NMOS3 and NMOS4 are controlled by internal signals *b2* and *b1* and PMOS2 and PMOS4 are controlled by external signals *Tb4* and *Tb3*. The voltage boosting module is employed to boost the voltage of *Tb4* and *Tb3*. To ensure conduction of PMOS2 and PMOS4 under different circumstance, *Tb4* and *Tb3* must transit between Vdd and 2Vdd. The controller module generates asynchronous control signals for the proposed cross-coupled voltage doublers, which has been shown in Figure B.7. The healthy control scheme for this cross-coupled voltage doubler is shown in Figure B.4.

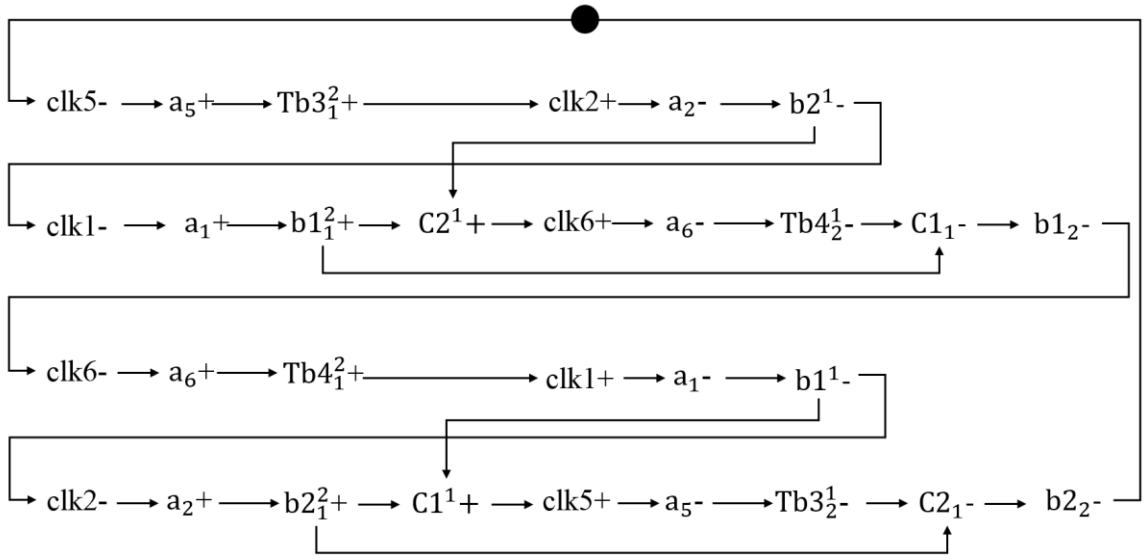


Figure B.2: SC-STG for the cross-coupled voltage doubler based on Case 2.

The SC-STG for the cross-coupled voltage doubler for Case 2 is shown in Figure B.2, illustrating the principle of the design and relations between events. As can be seen from this SC-STG, the flying capacitor C2 starts to be charged to Vdd when *b2* is Vdd and *b1* is 2Vdd and it starts to be discharged from Vdd (charge the output) when *b2* is 2Vdd and *Tb3* is Vdd. Similarly, C1 starts to be discharged (charge the output) when *b1* is 2Vdd and *Tb4* is Vdd and to be charged when *b1* is Vdd and *b2* is 2Vdd.

In Case 2, which is not shown in the diagram but has a similar structure, we introduce external signals *Tb4* and *Tb3* for PMOS2 and PMOS4 when *clk1* and *clk2* are overlapping, with which PMOS2 and PMOS4 can be turned off by *Tb4* and *Tb3* to avoid the output losses. The healthy control schemes for *Tb4*, *Tb3*, *clk1* and *clk2* can also be determined from a reachability analysis of the Petri net model.

In the following subsections, healthy control scheme for Case 2 is analysed and generated using the new design method.

Deriving the healthy control scheme for reversion loss avoidance.

In this case, there are only output losses from the output to flying capacitors C1 or C2 during the overlapping interval, when the load charges these capacitors, causing energy to flow backwards. To develop an asynchronous control and eliminate reversion losses, PMOS2 and PMOS4 are controlled by external signals *Tb4* and *Tb3*. It is similar to Case 1; the voltage promotion is implemented by external voltage doublers, where *Tb3* and *Tb4* are boosted from Vdd to 2Vdd with controls of *clk5* and *clk6*. The causality relations between these signals are: *clk5+*/*clk5-* causes *Tb3-*/ *Tb3+* and *clk6+*/*clk6-* causes *Tb4-*/*Tb4+*. With this, an SC-STG similar to that in Figure 5.5 may be drawn for this case. The entire system structure and SC-STG for Case 2 are shown in Appendix B.

A Petri net model for the cross-coupled voltage doubler controlled by *clk1*, *clk2*, *clk5*, *clk6* can be drawn, which is shown in Figure B.3. As can be seen from the Petri net model, since *clk1* and *clk2* are overlapping, there are only output losses from output to the flying capacitor. The reversion losses occur when *Tb3* is Vdd and *b2* is Vdd or *Tb4* is Vdd and *b1* is Vdd. Likewise, from a reachability analysis for the Petri net model, the healthy control scheme which avoids these signal combinations can be obtained. This is shown in Figure B.4.

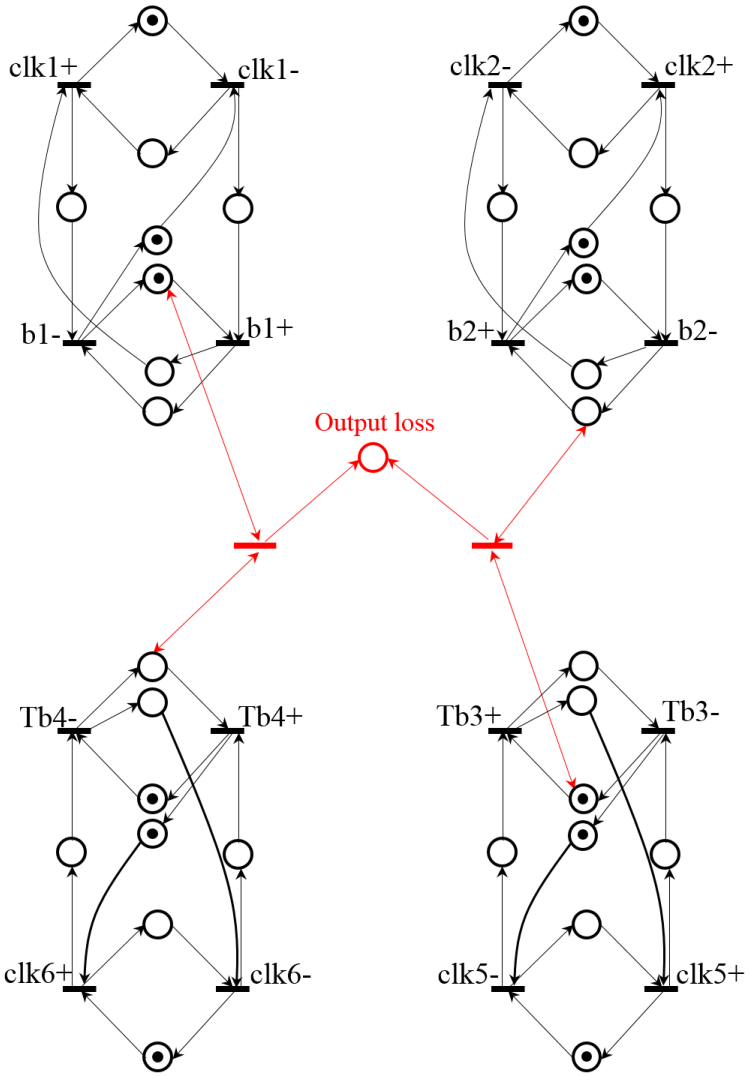


Figure B.3: Petri net model for reversion losses in Case 2.

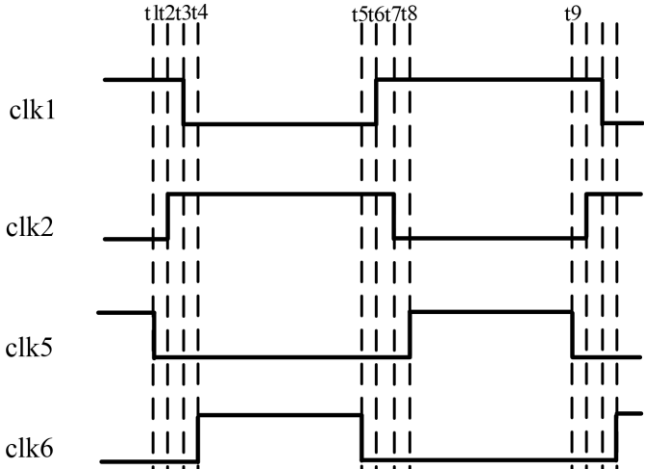


Figure B.4: Determined healthy control scheme for Case 2.

As can be seen from Figure B.4, signals *clk5* and *clk6* are non-overlapping. The non-overlapping gaps between *clk5* and *clk6* are wider than the overlapping gap between *clk1*

and *clk2*. Similarly, all these signals are not synchronised. The negative transition of *clk5* happens before the positive transition of *clk2* and the positive transition of *clk6* happens after the negative transition of *clk1*. The negative transition of *clk6* happens before the positive transition of *clk1* and the positive transition of *clk5* happens after the negative transition of *clk2*.

The next step is modelling these controls with STG and synthesising it to asynchronous circuits.

Deriving the asynchronous circuit generating the healthy control scheme.

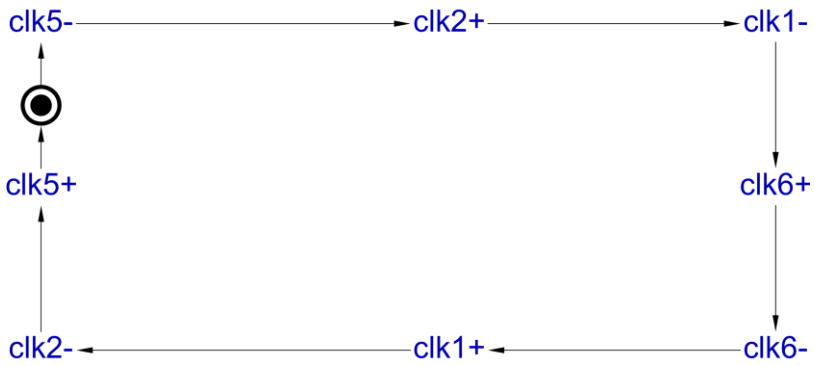


Figure B.5: STG model for the determined healthy control scheme (Case 2).

Following the reachability analysis method described in Chapter 3, we obtain the STG for the determined healthy control scheme for Case 2, which is shown in Figure B.5.

Likewise, delay elements are employed to regulate the frequencies and duty cycle ratios of control signals. Delay element Delay1 with input *delay1req* and output *delay1ack* is inserted to the short interval (e.g. interval *t1-t2*, *t2-t3*, *t3-t4*, *t5-t6*, *t6-t7* in Figure B.4), while Delay element Delay2 with input *delay2req* and output *delay2ack* is inserted to the long interval (e.g. interval *t4-t5* and *t8-t9* in Figure B.4). The STG for the healthy control scheme inserted with delay is shown in Figure B.6.

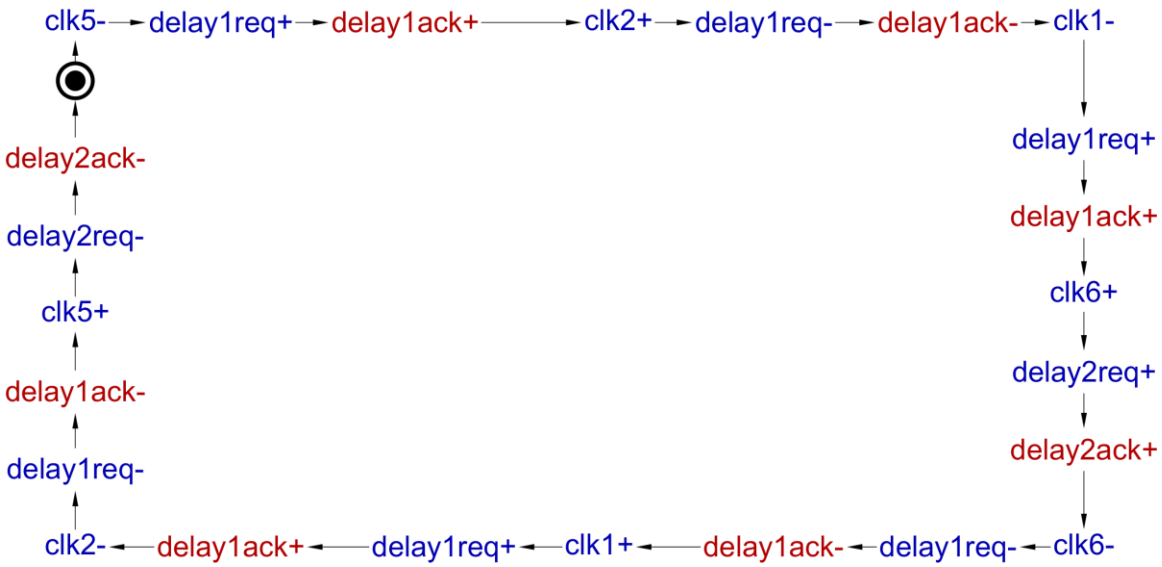


Figure B.6: Practical STG model for the determined healthy control scheme (Case 2).

After related verifications, this STG can be synthesised to an asynchronous circuit in Workcraft. The obtained asynchronous circuit with a reset signal is shown in Figure B.7.

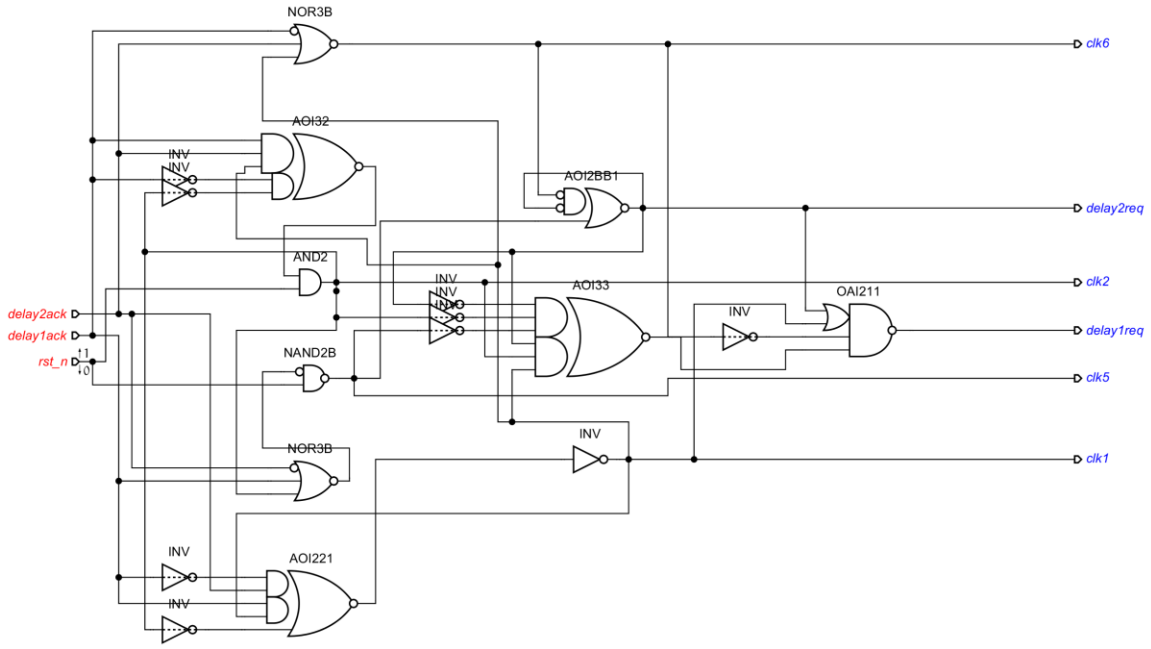


Figure B.7: Asynchronous circuit synthesised from STG model (with reset signal).

Note that this circuit is of similar size as that shown in Figure 5.11, but the corresponding signals are on different terminals.

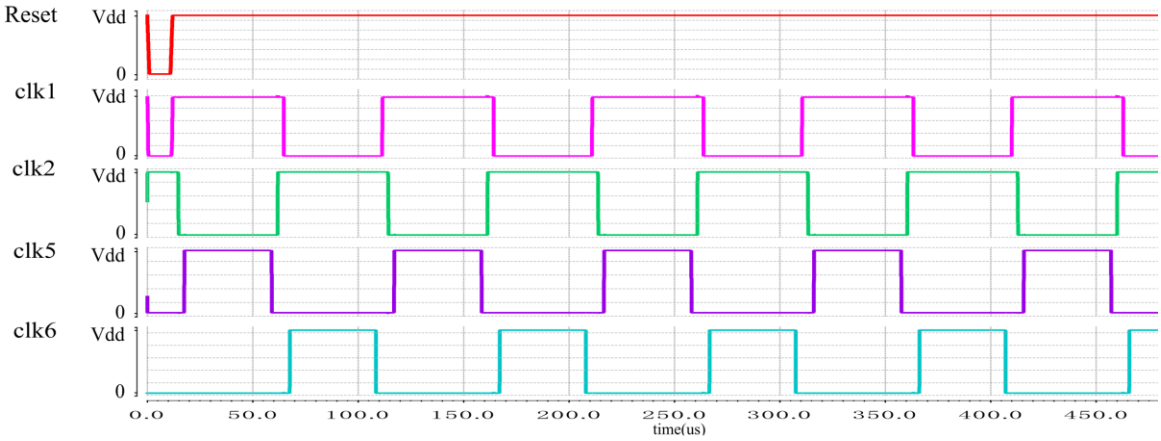


Figure B.8: Simulation waveform for the generated asynchronous circuit (Case 2).

This asynchronous circuit can also be initialised by resetting reset signals. Figure B.8 shows the waveform from the Cadence simulation of the circuit with appropriate delays inserted, where the timing of control signals perfectly matches the one in Figure B.4. In the same way, when the proposed cross-coupled voltage doubler in Case 2 is driven by the control signals generated by the circuit shown in Figure B.7, there is no reversion loss due to clock mismatch.

In summary, the reversion-loss-free cross-coupled voltage doubler for Case 2 is also designed with the proposed design method, from determining the healthy control scheme using a reachability analysis to obtaining an asynchronous control module by synthesising the corresponding STG model.

References

[1] D. Yang, G. Xue, X. Fang and J. Tang, "Incentive Mechanisms for Crowdsensing: Crowdsourcing with Smartphones," in *IEEE/ACM Transactions on Networking*, vol. 24, no. 3, pp. 1732-1744, June 2016.

[2] M. S. Hossain and G. Muhammad, "An Emotion Recognition System for Mobile Applications," in *IEEE Access*, vol. 5, pp. 2281-2287, 2017.

[3] W. Xu, W. Liang, J. Peng, Y. Liu and Y. Wang, "Maximizing Charging Satisfaction of Smartphone Users via Wireless Energy Transfer," in *IEEE Transactions on Mobile Computing*, vol. 16, no. 4, pp. 990-1004, 1 April 2017.

[4] D. Fang, Y. Qian and R. Q. Hu, "Security for 5G Mobile Wireless Networks," in *IEEE Access*, vol. 6, pp. 4850-4874, 2018.

[5] T. Breussegem and M. Steyaert, *CMOS Integrated Capacitive DC-DC Converters*. New York, NY: Springer, 2013.

[6] G. Palumbo and D. Pappalardo, "Charge Pump Circuits: An Overview on Design Strategies and Topologies," in *IEEE Circuits and Systems Magazine*, vol. 10, no. 1, pp. 31-45, First Quarter 2010.

[7] A. Cervera and M. M. Peretz, "Resonant switched-capacitor voltage regulator with ideal transient response," *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, Fort Worth, TX, 2014, pp. 867-872.

[8] C. Schaef and J. T. Stauth, "A 3-Phase Resonant Switched Capacitor Converter Delivering 7.7 W at 85% Efficiency Using 1.1 nH PCB Trace Inductors," in *IEEE Journal of Solid-State Circuits*, vol. 50, no. 12, pp. 2861-2869, Dec. 2015.

[9] C. Schaef, E. Din and J. T. Stauth, "A Hybrid Switched-Capacitor Battery Management IC With Embedded Diagnostics for Series-Stacked Li–Ion Arrays," in *IEEE Journal of Solid-State Circuits*, vol. 52, no. 12, pp. 3142-3154, Dec. 2017.

[10] M. D. Seeman and S. R. Sanders, "Analysis and Optimization of Switched-Capacitor DC–DC Converters," in *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 841-851, March 2008.

[11] Michael Douglas Seeman. *A Design Methodology for Switched-Capacitor DC-DC Converters*. PhD thesis. EECS Department, University of California, Berkeley, May 2009.

[12] S. Pasternak, C. Schaef and J. Stauth, "Equivalent resistance approach to optimization, analysis and comparison of hybrid/resonant switched-capacitor converters," *2016*

IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL), Trondheim, 2016, pp. 1-8.

[13] T. M. Van Breussegem and M. S. J. Steyaert, "Monolithic Capacitive DC-DC Converter with Single Boundary–Multiphase Control and Voltage Domain Stacking in 90 nm CMOS," in *IEEE Journal of Solid-State Circuits*, vol. 46, no. 7, pp. 1715-1727, July 2011.

[14] M. S. Makowski and D. Maksimovic, "Performance limits of switched-capacitor DC-DC converters," *Proceedings of PESC '95 - Power Electronics Specialist Conference*, Atlanta, GA, USA, 1995, pp. 1215-1221 vol.2.

[15] R. Karadi, "Synthesis of switched-capacitor power converters: An iterative algorithm," *2015 IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Vancouver, BC, 2015, pp. 1-4.

[16] Y. Mahnashi and F. Z. Peng, "Systematic approach to optimal SC converter synthesis for multi voltage-gain-ratio applications," *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Stanford, CA, 2017, pp. 1-5.

[17] N. Butzen and M. Steyaert, "Proof of General Switched-Capacitor DC-DC Converter Law using Voltage-Domain Analysis," *2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Padua, 2018, pp. 1-6.

[18] D. Maksimovic and S. Dhar, "Switched-capacitor DC-DC converters for low-power on-chip applications", *30th Annual IEEE Power Electronics Specialists Conference*. Record.

[19] Carl Adam Petri. *Kommunikation mit automaten (Communicating with automata)*. PhD thesis, University of Bonn, 1962.

[20] L. Rosenblum and A. Yakovlev, "Signal Graphs: From Self-Timed to Timed Ones", *Proceeding International Workshop on Timed Petri Nets*, pp. 199-206, 1985.

[21] P. Merlin, "A Methodology for the Design and Implementation of Communication Protocols", *IEEE Transactions on Communications*, vol. 24, no. 6, pp. 614-621, 1976.

[22] Molloy, "Performance Analysis Using Stochastic Petri Nets," in *IEEE Transactions on Computers*, vol. C-31, no. 9, pp. 913-917, Sept. 1982.

[23] F. Vallejo, J. A. Gregorio, M. Gonzalez Harbour and J. M. Drake, "Shared memory multi-microprocessor operating system with an extended Petri net model," in *IEEE Transactions on Parallel and Distributed Systems*, vol. 5, no. 7, pp. 749-762, July 1994.

[24] D. Sokolov and A. Yakovlev, "GALS Partitioning by Behavioural Decoupling Expressed in Petri Nets," *2014 20th IEEE International Symposium on Asynchronous Circuits and Systems*, Potsdam, 2014, pp. 17-26.

[25] T. Chu, *Synthesis of self-timed VLSI circuits from graph-theoretic specifications*, PhD thesis, MIT, 1987.

[26] D. Sokolov, V. Dubikhin, V. Khomenko, D. Lloyd, A. Mokhov and A. Yakovlev, "Benefits of asynchronous control for analogue electronics: Multiphase buck case study," *Design, Automation & Test in Europe Conference & Exhibition (DATE), 2017*, Lausanne, 2017, pp. 1751-1756.

[27] V. Dubikhin, D. Sokolov, A. Yakovlev and C. J. Myers, "Design of Mixed-Signal Systems with Asynchronous Control," in *IEEE Design & Test*, vol. 33, no. 5, pp. 44-55, Oct. 2016.

[28] V. Dubikhin, C. Myers, D. Sokolov, I. Syranidis and A. Yakovlev, "Invited: Advances in formal methods for the design of analog/mixed-signal systems," *2017 54th ACM/EDAC/IEEE Design Automation Conference (DAC)*, Austin, TX, 2017, pp. 1-6.

[29] S. Mileiko, A. Kushnerov, D. Sokolov and A. Yakovlev, "Self-timed control of two-phase switched capacitor converters," *2016 IEEE International Conference on the Science of Electrical Engineering (ICSEE)*, Eilat, 2016, pp. 1-4.

[30] S. Mileiko, A. Kushnerov, D. Sokolov and A. Yakovlev, "Self-timed control of multiphase switched capacitor converters," *2017 European Conference on Circuit Theory and Design (ECCTD)*, Catania, 2017, pp. 1-4.

[31] R. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. New York: Springer, 2012.

[32] M. Wens and M. Steyaert, *Design and implementation of fully-integrated inductive DC-DC converters in standard CMOS*. Dordrecht: Springer, 2011.

[33] M. D. Seeman and S. R. Sanders, “Analysis and optimization of switched-capacitor dc-dc power converters,” *IEEE Computers in Power Electronics Workshop*, pp. 216–224, July 2006.

[34] M. Makowski, "Realizability conditions and bounds on synthesis of switched-capacitor DC-DC voltage multiplier circuits", *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 44, no. 8, pp. 684-691, 1997.

[35] T. Tanzawa, *On-chip High-Voltage Generator Design*. Cham: Springer International Publishing, 2016.

[36] H. Marien *et al*., "An organic integrated capacitive DC-DC up-converter," *2010 Proceedings of ESSCIRC*, Seville, 2010, pp. 510-513.

[37] S. Pongswatd, K. Smerpituk, P. Julsereewong, K. Eguchi and H. Sasaki, "Design of fractional conversion ratio SC DC-DC converters," *2013 10th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology*, Krabi, 2013, pp. 1-4.

[38] L. G. Salem and P. P. Mercier, "A 45-ratio recursively sliced series-parallel switched-capacitor DC-DC converter achieving 86% efficiency," *Proceedings of the IEEE 2014 Custom Integrated Circuits Conference*, San Jose, CA, 2014, pp. 1-4.

[39] L. Su and D. Ma, "Design and optimization of integrated low-voltage low-power monolithic CMOS charge pumps," *2008 International Symposium on Power Electronics, Electrical Drives, Automation and Motion*, Ischia, 2008, pp. 43-48.

[40] J. Kim, Y. Jun and B. Kong, "CMOS Charge Pump With Transfer Blocking Technique for No Reversion Loss and Relaxed Clock Timing Restriction," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 56, no. 1, pp. 11-15, Jan. 2009.

[41] J. Kim, S. Park, K. Kwon, B. Kong, J. Choi and Y. Jun, "CMOS Charge Pump With No Reversion Loss and Enhanced Drivability," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 22, no. 6, pp. 1441-1445, June 2014.

[42] P. Ngo and D. Ma, "Integrated switched-capacitor voltage doubler with clock transition periods boosting and transfer blocking techniques," *2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Palm Springs, CA, 2010, pp. 813-817.

[43] C. Falconi, G. Savone and A. D'Amico, "High light-load efficiency charge pumps," *2005 IEEE International Symposium on Circuits and Systems*, Kobe, 2005, pp. 1887-1890 Vol. 2.

[44] F. Su, W.-H. Ki, and C.-Y. Tsui, “High efficiency cross-coupled doubler with no reversion loss,” in *Proc. IEEE Int. Symp. Circuits Syst*., 2006, pp. 2761–2764.

[45] Hoi Lee and P. K. T. Mok, "Switching noise and shoot-through current reduction techniques for switched-capacitor voltage doubler," in *IEEE Journal of Solid-State Circuits*, vol. 40, no. 5, pp. 1136-1146, May 2005.

[46] B. Shen and M. L. Johnston, "Zero Reversion Loss, High-Efficiency Charge Pump for Wide Output Current Load Range," *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, 2018, pp. 1-5.

[47] X. Yu, K. Moez, I. Wey, M. Sawan and J. Chen, "A Fully Integrated Multistage Cross-Coupled Voltage Multiplier With No Reversion Power Loss in a Standard CMOS Process," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, no. 7, pp. 737-741, July 2017.

[48] Z. Luo, M. Ker, W. Cheng and T. Yen, "Regulated Charge Pump With New Clocking Scheme for Smoothing the Charging Current in Low Voltage CMOS Process," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 3, pp. 528-536, March 2017.

[49] Y. Allasasmeh and S. Gregori, "Switch bootstrapping technique for voltage doublers and double charge pumps," *2011 IEEE International Symposium of Circuits and Systems (ISCAS)*, Rio de Janeiro, 2011, pp. 494-497.

[50] T. W. Mui, M. Ho, K. H. Mak, J. Guo, H. Chen and K. N. Leung, "An Area-Efficient 96.5%-Peak-Efficiency Cross-Coupled Voltage Doubler With Minimum Supply of 0.8 V," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 61, no. 9, pp. 656-660, Sept. 2014.

[51] H. Hwang, J. Chun and K. Kwon, "A low power cross-coupled charge pump with charge recycling scheme," *2009 3rd International Conference on Signals, Circuits and Systems (SCS)*, Medenine, 2009, pp. 1-5.

[52] X. Jiang, X. Yu, K. Moez, D. G. Elliott and J. Chen, "High-Efficiency Charge Pumps for Low-Power On-Chip Applications," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 65, no. 3, pp. 1143-1153, March 2018.

[53] P. Favrat, P. Deval and M. J. Declercq, "A high-efficiency CMOS voltage doubler," in *IEEE Journal of Solid-State Circuits*, vol. 33, no. 3, pp. 410-416, March 1998.

[54] E. Joffe and K. Lock, Grounds for Grounding. Hoboken: Wiley, 2010.

[55] Seung-Jae Choi, Y. Jun and B. Kong, "CMOS charge pump with separated charge sharing for improved boosting ratio and relaxed timing restriction," *2011 9th IEEE International Conference on ASIC*, Xiamen, 2011, pp. 133-136.

[56] K. Yu, S. Li, G. Zhang, Z. Zhang, Q. Tong and X. Zou, "Design Considerations of Charge Pump for Antenna Switch Controller With SOI CMOS Technology," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, no. 3, pp. 229-233, March 2017.

[57] B. Cen, Y. Jiang, K. Ng, M. Law, P. Mak and R. P. Martins, "A wide range high efficiency fully integrated switched-capacitor DC-DC converter with fixed output

spectrum modulation," *2017 International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, Hsinchu, 2017, pp. 1-2.

[58] F. Su and W. Ki, "An integrated reconfigurable SC Power converter with hybrid gate control scheme for mobile display driver applications," *2008 IEEE Asian Solid-State Circuits Conference*, Fukuoka, 2008, pp. 169-172.

[59] Y. Tsividis, "Principles of operation and analysis of switched-capacitor circuits," in *Proceedings of the IEEE*, vol. 71, no. 8, pp. 926-940, Aug. 1983.

[60] J. Peterson, *Petri net theory and the modeling of systems*, 1981.

[61] T. Murata, "Petri nets: Properties, analysis and applications," in *Proceedings of the IEEE*, vol. 77, no. 4, pp. 541-580, April 1989.

[62] I. Poliakov, A. Mokhov, A. Rafiev, D. Sokolov and A. Yakovlev, "Automated Verification of Asynchronous Circuits Using Circuit Petri Nets," *2008 14th IEEE International Symposium on Asynchronous Circuits and Systems*, Newcastle upon Tyne, 2008, pp. 161-170.

[63] M. Uzam and M. Zhou, "An Iterative Synthesis Approach to Petri Net-Based Deadlock Prevention Policy for Flexible Manufacturing Systems," in *IEEE Transactions on Systems, Man, and Cybernetics - Part A: Systems and Humans*, vol. 37, no. 3, pp. 362-371, May 2007.

[64] Z. Li, M. Zhou and N. Wu, "A Survey and Comparison of Petri Net-Based Deadlock Prevention Policies for Flexible Manufacturing Systems," in *IEEE Transactions on Systems, Man, and Cybernetics, Part C (Applications and Reviews)*, vol. 38, no. 2, pp. 173-188, March 2008.

[65] C. Myers, *Asynchronous Circuit Design*. Hoboken: John Wiley & Sons, 2004.

[66] V. Varshavskiĭ, *Self-Timed Control of Concurrent Processes*. Dordrecht: Springer Netherlands, 1990.

[67] K. Van Berkel, R. Burgess, J. Kessels, M. Roncken, F. Schalij and A. Peeters, "Asynchronous circuits for low power: a DCC error corrector," in *IEEE Design & Test of Computers*, vol. 11, no. 2, pp. 22-32, Summer 1994.

[68] T. E. Williams and M. A. Horowitz, "A Zero-overhead Self-timed 160ns 54b CMOS Divider," *1991 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, San Francisco, CA, USA, 1991, pp. 98-296.

[69] N. C. Paver, P. Day, C. Farnsworth, D. L. Jackson, W. A. Lien and J. Liu, "A low-power, low noise, configurable self-timed DSP," *Proceedings Fourth International*

Symposium on Advanced Research in Asynchronous Circuits and Systems, San Diego, CA, USA, 1998, pp. 32-42.

[70] C. Niessen, C. H. van Berkel, M. Rem and R. W. J. J. Saeijs, "VLSI programming and silicon compilation-a novel approach from Philips research," *Proceedings 1988 IEEE International Conference on Computer Design: VLSI*, Rye Brook, NY, USA, 1988, pp. 150-151.

[71] WORKCRAFT homepage: http://workcraft.org/.

[72] J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno, and A. Yakovlev. Petrify: a tool for manipulating concurrent specifications and synthesis of asynchronous controllers. *IEICE Transactions on Information and Systems*, 1997, E80-D(3):315–325.

[73] Unfolding tools homepage: http://homepages.cs.ncl.ac.uk/victor.khomenko/tools

[74] CPN tools homepage: http://cpntools.org/

[75] EPNK homepage: http://www.imm.dtu.dk/

[76] N. Dingle, W. Knottenbelt and T. Suto, "PIPE2", *ACM SIGMETRICS Performance Evaluation Review*, vol. 36, no. 4, pp. 34-39, 2009.

[77] ORIS homepage: https://www.oris-tool.org/

[78] CLP homepage: http://homepages.cs.ncl.ac.uk/victor.khomenko/tools

[79] X. Zhang, D. Shang, F. Xia, H. Low and A. Yakovlev, "A hybrid power delivery method for asynchronous loads in energy harvesting systems", *10th IEEE International NEWCAS Conference*, 2012.

[80] W. Jung, S. Oh, S. Bang, Y. Lee, Z. Foo, G. Kim, Y. Zhang, D. Sylvester and D. Blaauw, "An Ultra-Low Power Fully Integrated Energy Harvester Based on Self-Oscillating Switched-Capacitor Voltage Doubler", *IEEE Journal of Solid-State Circuits*, vol. 49, no. 12, pp. 2800-2811, 2014.

[81] N. Butzen and M. S. J. Steyaert, "Scalable Parasitic Charge Redistribution: Design of High-Efficiency Fully Integrated Switched-Capacitor DC–DC Converters," in *IEEE Journal of Solid-State Circuits*, vol. 51, no. 12, pp. 2843-2853, Dec. 2016.

[82] N. Butzen and M. S. J. Steyaert, "Design of Soft-Charging Switched-Capacitor DC–DC Converters Using Stage Outphasing and Multiphase Soft-Charging," in *IEEE Journal of Solid-State Circuits*, vol. 52, no. 12, pp. 3132-3141, Dec. 2017.

[83] J. Kim, P. K. T. Mok and C. Kim, "A 0.15 V Input Energy Harvesting Charge Pump With Dynamic Body Biasing and Adaptive Dead-Time for Efficiency Improvement," in *IEEE Journal of Solid-State Circuits*, vol. 50, no. 2, pp. 414-425, Feb. 2015.

[84] D. Kilani, M. Alhawari, B. Mohammad, H. Saleh and M. Ismail, "An Efficient Switched-Capacitor DC-DC Buck Converter for Self-Powered Wearable Electronics," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 10, pp. 1557-1566, Oct. 2016.

[85] S. S. Kudva and R. Harjani, "Fully Integrated Capacitive DC–DC Converter With All-Digital Ripple Mitigation Technique," in *IEEE Journal of Solid-State Circuits*, vol. 48, no. 8, pp. 1910-1920, Aug. 2013.

[86] T. Ozaki, T. Hirose, H. Asano, N. Kuroki and M. Numa, "A fully-integrated, high-conversion-ratio and dual-output voltage boost converter with MPPT for low-voltage energy harvesting," *2015 IEEE Asian Solid-State Circuits Conference (A-SSCDDC)*, Xiamen, 2015, pp. 1-4.

[87] D. Somasekhar *et al*., "Multi-phase 1GHz voltage doubler charge-pump in 32nm logic process," *2009 Symposium on VLSI Circuits*, Kyoto, Japan, 2009, pp. 196-197.

[88] L. G. Salem, J. G. Louie and P. P. Mercier, "Flying-Domain DC–DC Power Conversion," in *IEEE Journal of Solid-State Circuits*, vol. 51, no. 12, pp. 2830-2842, Dec. 2016.

[89] H. Le, S. R. Sanders and E. Alon, "Design Techniques for Fully Integrated Switched-Capacitor DC-DC Converters," in *IEEE Journal of Solid-State Circuits*, vol. 46, no. 9, pp. 2120-2131, Sept. 2011.

[90] Y. K. Ramadass, A. P. Chandrakasan, "Voltage scalable switched capacitor DC-DC converter for ultra-low-power on-chip applications", *Proc. 2007 IEEE Power Electronics Specialists Conf. (PESC)*, pp. 2353-2359, 2007.

[91] T. Van Breussegem, M. Steyaert, "A 82% efficiency 0.5% ripple 16-phase fully integrated capacitive voltage doubler", *2009 IEEE Symp. VLSI Circuits Dig.*, pp. 198-199, 2009.

[92] D. Somasekhar, B. Srinivasan, G. Pandya, F. Hamzaoglu, M. Khellah, T. Karnik, K. Zhang, "Multiphase 1 GHz voltage doubler charge-pump in 32 nm logic process", *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 751-758, Apr. 2010.

[93] Y. Ramadass, A. Fayed, A. Chandrakasan, "A fully-integrated switched-capacitor step-down DC-DC converter with digital capacitance modulation in 45 nm CMOS", *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2557-2565, Dec. 2010.

[94] D. Li, D. Shang, F. Xia and A. Yakovlev, "Modelling Switched-Capacitor DC-DC Converters with Signal Transition Graphs," 2018 15th International Conference on

Synthesis, Modelling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), Prague.

[95] D. Li, F. Xia, J. Luo and A. Yakovlev, " Modelling Reversion Loss and Shoot-through Current in Switched-Capacitor DC-DC Converters with Petri Net," 2019 29th International Workshop on Power and Timing Modelling, Optimisation and Simulation (PATMOS), Rhodes.

[96] Danil Sokolov. *Automated synthesis of asynchronous circuits using direct mapping for control and data paths*. PhD thesis. University of Newcastle University, Newcastle, January 2006.