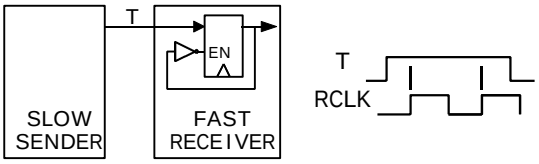
## What's Wrong with this? Some questions and a sum

- with acknowledgements to Ran Ginosar



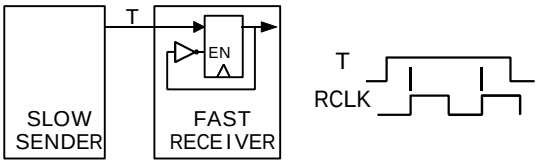
## Slow-to-Fast Synchronizer




- How does it work?
  - ***T*** is set for one cycle
  - Receiver has at least 2 chances to read ***T***
- What can go wrong?



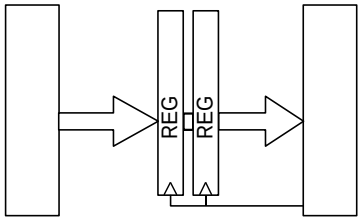
## Slow-to-Fast Synchronizer




- In a next generation chip, the sender is faster
- Reuse limitation



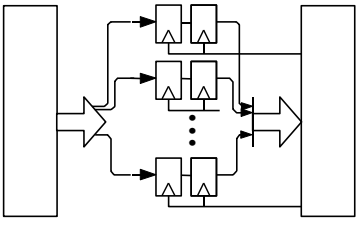
## Parallel Synchronizer




- Used in Multi-Sync cases
- New data sent every cycle
- This one is extremely dangerous (MTBF=0) !
- Why?



## Parallel Synchronizer



- Some bits may go metastable
- Some will resolve to 0, others to 1
- Guaranteed to fail…



## A Two-Latch Synchronizer

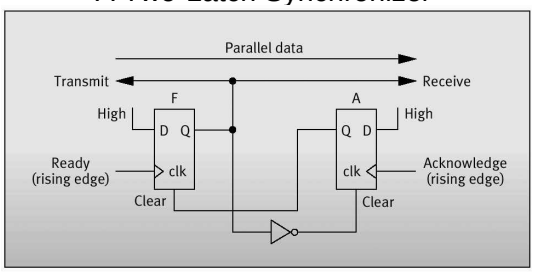



Figure 1: Parallel passing is normally used as the traditional method to generate a flag.

- What's wrong with this one?

## A Two-Latch Synchronizer

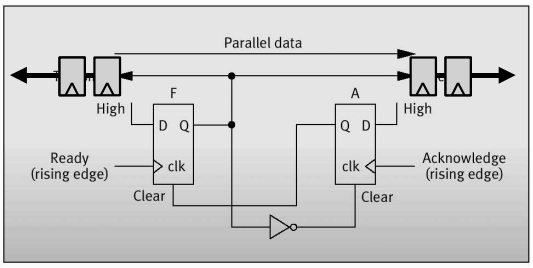
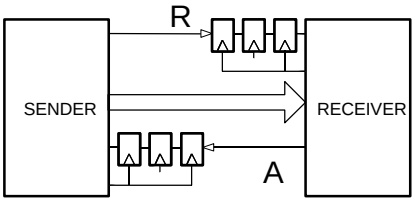



Figure 1: Parallel passing is normally used as the traditional method to generate a flag.

- The synchronizers were left out...



## Conservative Synchronizer




- FC = 200MHz
- FD = FC
- $T_W$ = 50 psec (0.18μ)
- τ = 10 psec

- What's the MTBF for
  - Two-FF sync ?
  - Three-FF sync ?
  - Eight-FF sync ?



## Conservative Synchronizer

- $F_C$ = 200MHz
- $F_D = F_C$
- $T_W$ = 50 psec (0.18μ)
- τ = 10 psec

*The universe is only $10^{10}$ years old..*

*Now I am **really** safe!*

$$MTBF(T) = \frac{e^{T/\tau}}{T_W \cdot F_C \cdot F_D} = \frac{e^{T/\tau}}{50\,p\sec \cdot 200MHz \cdot 200MHz}$$

$$= \frac{e^{\frac{1000}{2}}}{2\times10^{6}} = 10^{203}\ years$$

$$MTBF(2T) = \frac{e^{10nsec/10psec}}{50\,p\sec \cdot 200MHz \cdot 200MHz} = \frac{e^{1000}}{2\times10^{6}} = 10^{420}\ years$$



## Conservative Synchronizer

- What's wrong with being conservative ?
  - This guy doesn't know what he's doing…
  - So I am worried about OTHER synchronizers that he has done!



## What would the latency be if…?

- Imagine a future GALS SoC with 100 independent unpredictable clock zones, $f_c = f_d$ = 5GHz, $T_w = \tau$ = 10ps.
- How much time do 100 simple synchronizers need to get an overall reliability of 1 year? How many clock cycles? (40τ, or 2 cycles)
- How long does it take to transmit data from one side of the chip to the other? (across 9 boundaries) (9x 400 ps, or 1.8ns)